13W 802.3af PoE PD Interface with Fly-back DC/DC Converter

Features

- Compatible with 802.3af Specifications
- 100V, 0.6Ω Integrated Pass Switch
- 150mA DC Input Current Limit
- 450mA PD Operation Current Limit
- Cycle-by-cycle Switch-current Limits
- Integrated 160V 0.8Ω Power Switching
- Integrated 100V Start-Up Circuit
- Programmable Switching Frequency
- Internal Slope Compensation OCP, SCP, and OTP
- Auto-Restart for Opened/Shorted Output
- Duty Cycle Limiting with Line Feed Forward
- Line Over Voltage Protection
- Built-in soft start

Application

- Security Camera
- VoIP Phones
- WLAN Access Points
- IP Cameras

Description

The TMI7325B is an integrated IEEE 802.3af PoE compliant Powered Device (PD) power supply solution. It includes a PD interface and an isolated/non-isolated fly-back.

The PD interface includes detection and classification modes as well as a 100V output pass device. An inrush current limit is included to charge the input capacitor slowly without interruption due to die heating.

The DC-DC converter integrates a 160V power switch, which can convert the energy of PD with lower loss. Further it has the functions of internal soft-start and automatic retry. Besides, it has Over Current Protection (OCP), output short-circuit, Over Voltage Protection (OVP) and thermal shutdown protection, and can keep no-load operation through skip cycle. The DC-DC switching frequency supports external resistance setting and external clock synchronization.

The TMI7325B features power good output with inrush completion delay and is available in a thermally enhanced 4mm x 6mm DFN-20 package.

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Typical Application

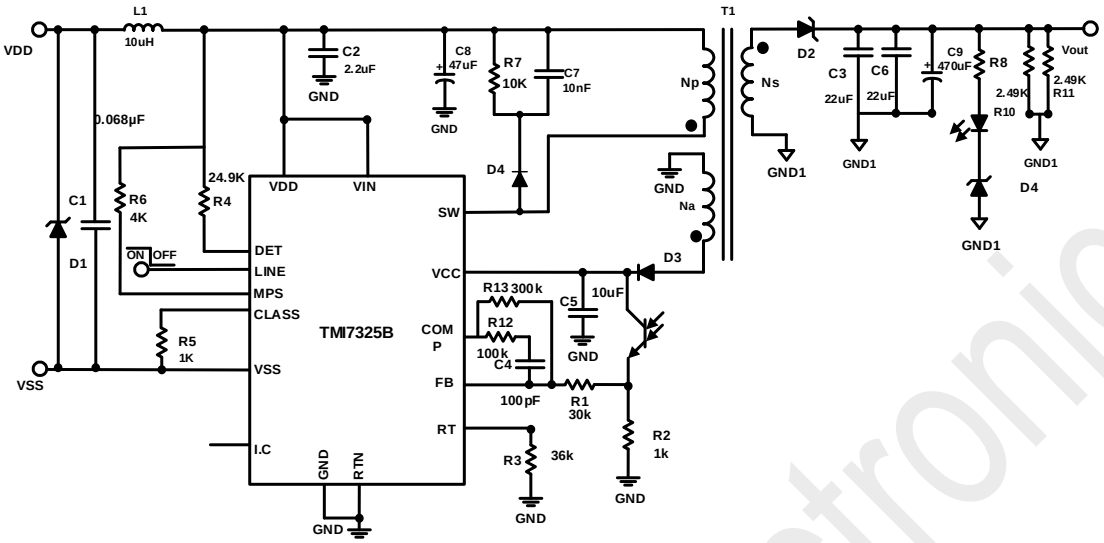

Figure 1 TMI7325B Typical Application Circuit

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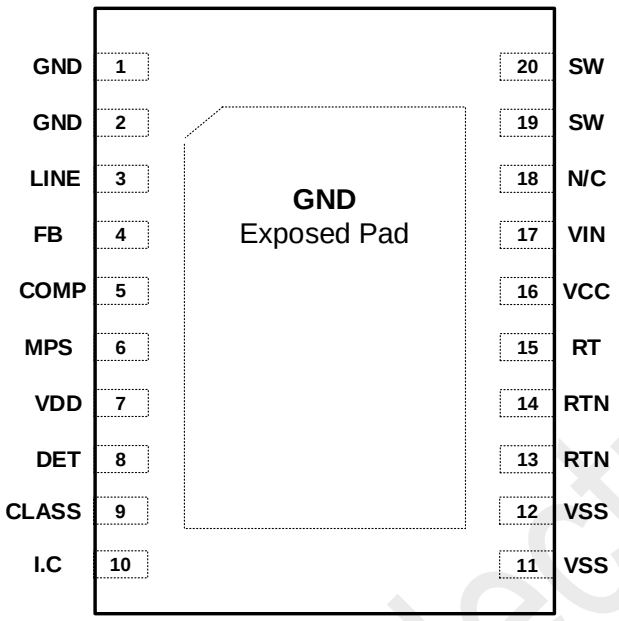
Package



Top View

DFN4x6-20

Top Marking: T7325B/XXXXX (T7325B: Device Code, XXXXX: Inside Code)

Order Information

Part Number	Package	Top Marking
TMI7325B	DFN4x6-20	T7325B XXXXX

TMI7325B devices are Pb-free and RoHS compliant.

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Pin Functions

Pin	Name	Function
1,2	GND	Ground Pin. DC-DC converter power return and reference node. Internally connected to RTN.
3	LINE	Input UV/LV set point. Short to ground to turn the controller off.
4	FB	Regulation Feedback Input. Inverting input of the error amplifier. The noninverting is internally connected to 1.21V
5	COMP	Error Amplifier Output
6	MPS	Open drain output. Keep Pin 10 I.C floating: pin6 work as MPS switch to generate current pulses by connecting a resistor between MPS and VDD.
7	VDD	Positive Power Supply Terminal. Connect a 68nF bypass capacitor between VDD and VSS.
8	DET	Detection Resistor Input. Connect a signature resistor (RDET = 24.9k) from DET to VDD.
9	CLASS	Classification Resistor Input. Connect a resistor (RCLS) from CLS to VSS to set the desired classification current.
10	I.C	Internally pulled up to internal 5V. The state of pin10 determines the function of pin6. Keep Pin10 floating, pin6 works as MPS switch;
11,12	VSS	Negative Supply Input. VSS connects to the source of the integrated isolation n-channel power MOSFET.
13,14	RTN	Drain of PD pass MOSFET. Internally connected to GND pin. Connect RTN to the downstream DC-DC converter ground as shown in the Typical Application Circuit.
15	RT	Oscillator Resistor and Synchronous Clock Pin. Connect an external resistor to GND for oscillator frequency setting. It can be used as a synchronous input from external oscillator clock.
16	VCC	Supply Bias Voltage for DC converter. A capacitor no less than 1uF is recommended to connect between this pin and GND.
17	VIN	DCDC converter High Voltage Startup Circuit Supply.
18	NC	No connection.
19/20	SW	Output Switching Node. High voltage power N-Channel MOSFET drain output.

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Absolute Maximum Ratings (Note 1)

Parameter	Min	Max	Unit
VDD, RTN, DET, MPS, GND, to VSS	-0.5	100	V
CLASS to VSS	-0.3	5.5	V
SW to GND	-0.3	160	V
All other pins voltage	-0.3	5.5	V
Continuous Power Dissipation (T_A=+25°C), PD	Internally Limited		
Junction Temperature	-40	150	°C
Lead Temperature		260	°C
Storage Temperature	-55	150	°C

ESD Rating (Note4)

Items	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2017 Classification, Class: 2	±2000	V
$V_{(ESD-CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2018 Classification, Class: C3	±1000	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±200	mA

JEDEC specification JS-001

Recommended Operating Conditions

Parameter	Min	TYP	Max	Unit
Supply Voltage V_{DD},V_{IN}	0		57	V
Switching Voltage V_{SW}	-0.5		160	V
Supply Voltage VCC	4		5	V
Operating Junction Temperature, T_J	-40		85	°C

Thermal Resistance (Note3)

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	37.5	°C/W
θ_{JC}	Junction-to-case(top) thermal resistance	22.8	°C/W
θ_{JB}	Junction-to-board thermal resistance	12.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.5	°C/W

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Electrical Characteristics

(Unless otherwise specified, the reference ground of VDD, CLASS, DET, and RTN is VSS; other pins are referenced to GND. VDD=48V, R_{DET}=24.9kΩ, RTN AND MPS floating, VCC=5V, V_{LINE}=1.8V, RT=20kΩ, TA=25°C)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Detection							
V_{DET_ON}	Detection on	V_{VDD}=V_{RTN}=V_{PG}=1.9V			1.4		V
V_{DET_OFF}	Detection off	V_{VDD}=V_{RTN}=V_{PG}=12V		11.3	12	12.7	V
V_{DET_LK}	DET Leakage Current	V_{DET}=V_{VDD}=57V, Measure IDET			0.1	5	μA
V_{DET_H}	Detection on/off Hysteresis	Falling below 12V on Threshold			1		V
I_{DET}	Detection Current	V_{VDD}=V_{RTN}, RDET=24.9kΩ, Measure I_{VDD}+I_{RTN}+I_{DET}	V_{DD}=1.4V	55.1	56	56.9	μA
			V_{DD}=10.1V	400	408	416	μA
Classification							
V_{CLASS}	VCLASS Output Voltage	13V<V_{DD}< 21V 1mA<I_{CLASS}< 30mA			1.22		V
I_{CLASS}	Classification Current	13≤V_{VDD}≤21V, Guaranteed by V_{CLASS}					
		RCLASS=509Ω, 13≤VVDD≤21V		2.2	2.4	2.8	mA
		RCLASS=115Ω, 13≤VVDD≤21V		10.3	10.6	11.3	
		RCLASS=66.7Ω, 13≤VVDD≤21V		17.7	18.3	19.5	
		RCLASS=43.6Ω, 13≤VVDD≤21V		27.1	28	29.5	
V_{CL_ON}	Classification Lower Threshold	Regulator Turns on, V_{VDD} Rising		11	12	13	V
V_{CU_OFF}	Classification Upper Threshold	Regulator Turns off, V_{VDD} Rising		21	22	23	V
V_{CL_HYS}	Classification Hysteresis	Low side Hysteresis			0.77		V
I_{IN_CLASS}	IC Supply Current during Classification	V_{DD} =17.5V, CLASS Floating		100	150	200	μA
$I_{LEAKAGE}$	Leakage Current	V_{CLASS} =0 V, V_{VDD} =57V				1	μA
PD UVLO							
$V_{DD\text{-}VSS\text{-}R}$	VDD Turn on Threshold	VDD Rising		37.5	38.6	40	V
$V_{DD\text{-}VSS\text{-}F}$	VDD Turn off Threshold	VDD Falling			31		V
I_{IN}	IC Supply Current during Operation	V_{VDD} = 48V, Pins 5, 6 Floating Measure I_{VDD}			240	450	μA
Pass Device and Current Limit							
$R_{ON\text{-}RTN}$	On Resistance	I_{RTN}=300mA			0.6		Ω
$I_{RTN\text{-}LK}$	Leakage Current	V_{DD}=VRTN=57V			1	15	μA
I_{LIMIT}	Current Limit	V_{RTN}=1V		400	450	500	mA

Electrical Characteristics

(Unless otherwise specified, the reference ground of VDD, CLASS, DET, and RTN is VSS; other pins are referenced to GND. VDD=48V, R_{DET}=24.9kΩ, RTN AND MPS floating, VCC=5V, V_{LINE}=1.8V, RT=20kΩ, TA=25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LIMIT}	Inrush Current Limit	V_{RTN}=2V	120	150	200	mA
t_{DELAY}	Inrush to Operation Mode Delay	T_{DELAY} = minimum PG current pulse width after entering into power mode	80	94	110	ms
V_{FOLD}	Current Fold-back Threshold	V_{RTN} Rising	9.5	10	105	V
t_{FOLD}	Fold-back Deglitch Time	V_{RTN} Rising to Inrush Current Fold-back		345		μs
MPS						
I_{MPS_TH}	Automatic MPS falling current threshold	Startup has completed, IRTN falling threshold to generate MPS pulses		35		mA
I_{MPS_HYS}	HYS	Hysteresis on RTN current		3		mA
D_{MPS}	MPS pulsed mode duty cycle	MPS pulsed current ON time		75		ms
		MPS pulsed current OFF time		225		ms
		MPS pulsed current duty cycle	24.7%	25%	25.3%	
PD Thermal Shutdown						
T_{PD-SD}	Thermal Shut down Temperature(5)		140	152	160	°C
T_{PD-HYS}	Thermal Shut down Hysteresis(5)			20		°C
Converter Power Supply and UVLO						
V_{CC}	V_{CC} Upper Threshold Voltage			5		V
	V_{CC} Lower Threshold Voltage			4		V
	V_{CC} Over Voltage Threshold Voltage			5.5		V
I_{ST}	Startup Current	V_{IN} = 12V, V_{CC} = 4.0V		4		mA
	Startup Current	V_{IN} = 20V, V_{CC} = 4.0V		5		mA
Icc	Quiescent Current	1.2V < V_{LINE} < 3.2V, VFB = 1.3V		0.55		mA
Line	Line OV Threshold Voltage			2.7		V
	Line OV Hysteresis			300		mV
	Line UV Threshold Voltage	V_{CC} = 5.0V		1.2		V
	Line UV Hysteresis	V_{CC} = 5.0V		100		mV

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Electrical Characteristics

(Unless otherwise specified, the reference ground of VDD, CLASS, DET, and RTN is VSS; other pins are referenced to GND. VDD=48V, R_{DET}=24.9kΩ, RTN AND PG floating, VCC=5V, V_{LINE}=1.8V, RT=20kΩ, TA=25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Voltage Feedback						
V_{FB}	Feedback Voltage			1.21		V
I_{FB}	Feedback Input Current	VFB = 1.2V		1		nA
GBW	Error Amplifier Gain Bandwidth			2		MHz
AV	Error Amplifier DC Gain		60			dB
I_{OH}	Comp Output Source Current	V_{FB}= 1.0V, V_{COMP} = 0.5V		11		mA
I_{OL}	Comp Output Sink Current	V_{FB}= 1.4V, V_{COMP} = 2.5V		5		mA
PWM (DC-DC)						
F_{MIN}	Minimum Oscillating Frequency	RT = 100k		60		kHz
F_{MAX}	Maximum Oscillating Frequency	RT = 10k		550		kHz
Switching Power Device						
R_{ON-SW}	On Resistance	V_{SW} = 0.1V		0.8		Ω
I_{LK}	Switch Leakage Current	V_{SW} = 150V		1		uA
Current Sense						
I_{LIMIT}	Switching Current Limit			2		A
DCDC Converter Thermal Shutdown						
T_{SD}	Thermal Shutdown Temperature(5)			155		°C
T_{HYS}	Thermal Shutdown Hysteresis(5)			30		°C

Notes 1: Exceeding these ratings may damage the device.

Notes 2: GND and AGND must be connected to RTN

Notes 3: Refer to the “Converter Output Voltage Setting” section.

Notes 4: VCC voltage can be pulled higher than this rating, but the external pull-up current should be limited. Refer to “VCC sinking current” rating and “VCC Power Supply Setting” section.

Notes 5: The maximum allowable power dissipation is a function of the maximum junction temperature TJ (MAX), the junction-to-ambient thermal resistance θJA, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (TJ (MAX)-TA)/θJA. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Notes 6: The device is not guaranteed to function outside of its operating conditions.

Notes 7: Measured on JESD51-7, 4-layer PCB.

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Notes 8: Guaranteed by characterization, not tested in production.

Notes 9: The maximum VCC UVLO rising threshold is higher than the minimum VCC regulation in the EC table due to production distribution. However, for one unit, VCC regulation is higher than the VCC UVLO rising threshold. The VCC UVLO rising threshold is about 87 percent of the VCC regulation voltage, and the VCC UVLO falling threshold is about 83 percent of the VCC regulation voltage in one unit.

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Block Diagram

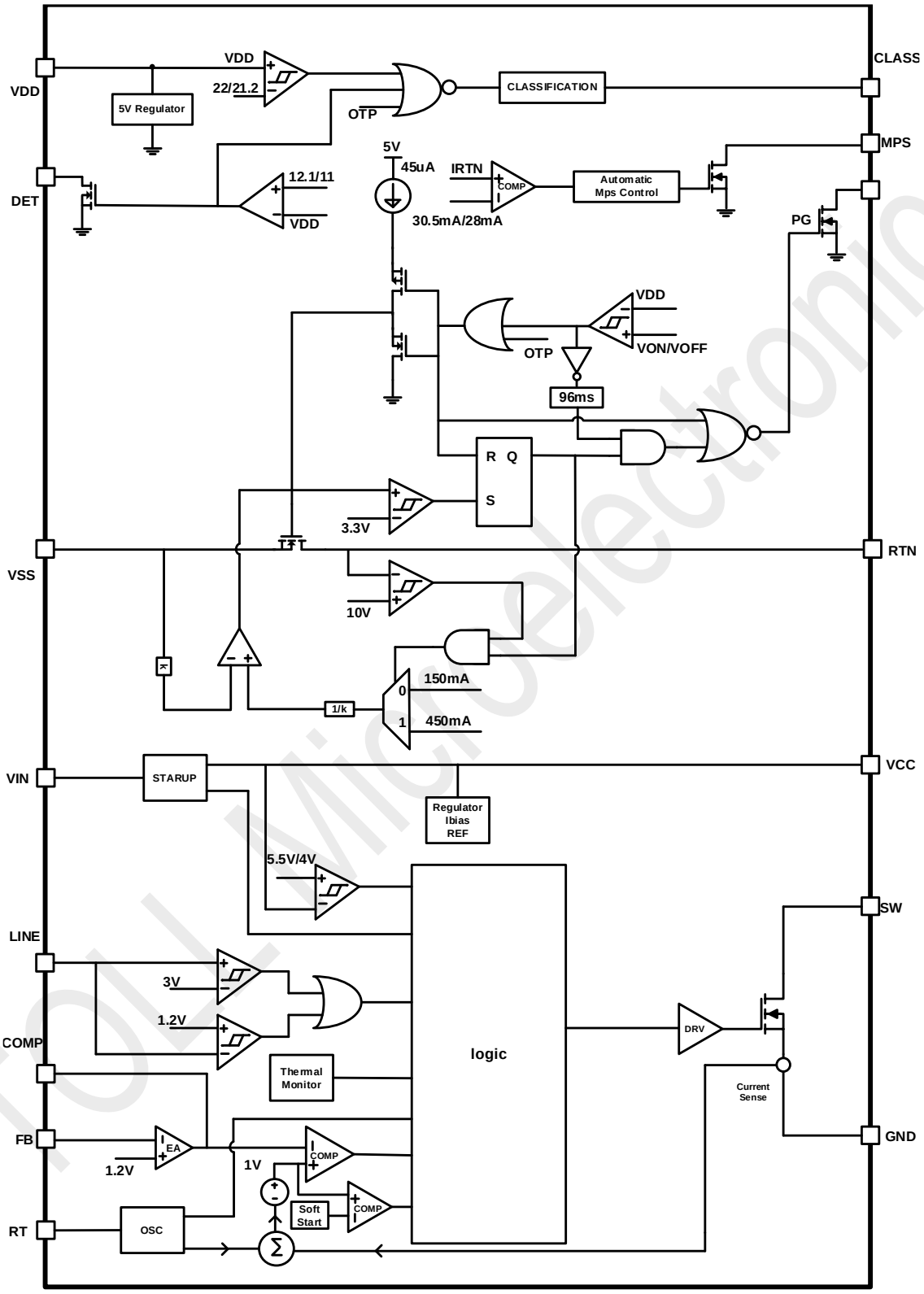

Figure 1. TMI7325B Block Diagram

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Operation Description

Overview

TMI7325B has 3 different operating modes based on input voltage VDD: PD detection, PD classification and PD power mode. TMI7325B entered PD detection mode when the input voltage ranges 1.4V to 10.1V. TMI7325B entered PD classification mode when the input voltage ranges 12.6V to 20V. Once the input voltage exceeds V_{ON}, the device will move into PD power mode.

Detection

In the detection mode, PSE supplies VDD two voltages within 1.4V to 10.1V, and two current measurements of above two voltages should be recorded. PSE then calculates ΔV/ΔI to ensure that 24.9kΩ characteristic resistor is connected. Connect a characteristic resistor (R_{DET}) between VDD and DET for ensuring proper feature detection. During the detection phase, TMI7325B pulls down DET. When the input voltage is higher than 12.7V, DET becomes high impedance state. In the detection mode, most internal circuits of TMI7325B in off-state, which offset current is less than 10μA. Please install the protection diode on the input port in order to avoid damaging the interior of TMI7325B if PD voltage is reversed. Because the fact that PSE uses gradient (ΔV/ΔI) to calculate characteristic resistance, the DC bias caused by diodes cannot be considered, and the detection progress will not be affected.

Classification

In the classification mode, PSE classifies PD based on the required power dissipation, and PSE can manage power distribution efficiently. An external resistor needs to be connected between CLS and VSS for setting the classification current. PSE ensures the class of PD through applying voltage to PD and measuring PSE output current. When the applying voltage by PSE ranges between 12.6V and 20V, the TMI7325B current characteristics are shown as the follow illustration. PSE uses classification current to classify PD required power. Classification current includes the current absorbed by RCLS and the supply current of TMI7325B, so the total current absorbed by PD is within the index range of IEEE802.3af/at. Close the classification current when the device is in power mode.

Power Mode

When VDD rises above the undervoltage lockout threshold (V_{ON}), the TMI7325B moves into power mode. When VDD rises to V_{ON}, TMI7325B turns on internal n-channel isolation MOSFET, and connects VSS to RTN. Then internal inrush current limit sets 150mA (Typical). When the voltage of RTN is closed to the voltage of VSS and the inrush current decreases below the inrush threshold, isolation MOSFET is fully turned on. Once that, TMI7325B will change the current limits to 450mA. Before power MOSFET is fully turned on, in order to ban the subsequent DC-DC converter during inrush, Power Good open-drain output keeps low, and the duration is t_{DELAY} at least.

Undervoltage Lockout

The operating voltage of TMI7325B is up to 60V, and the UVLO threshold (V_{ON}) of the circuit is 38.6V; the UVLO threshold (V_{OFF}) of the circuit is 31V. When the input voltage is higher than V_{ON}, TMI7325B moves into power mode and internal MOSFET turns on. When the time of the input voltage which is less than V_{OFF} exceeds t_{OFF_DLY}, MOSFET turns off.

Power Good Output

PG is an active low output that is pulled to VSS when the device is in the steady-state power mode. It remains in a high impedance state at all other times.

Thermal Shutdown Protection

TMI7325B has the function of thermal shutdown protection to avoid overheat. If the junction temperature exceeds thermal shutdown threshold of +152°C, TMI7325B will turn off internal power MOSFET . When the junction temperature decreases less than +132°C, the device moves into inrush mode, and then returns to power mode. Inrush mode can ensure that closes subsequent DC-DC converter before the internal power MOSFET turns on.

DCDC Converter Startup and Power Supply

After the PD conduction tube is turned on, the power supply between VIN and GND starts to supply power, and the VCC pin to the capacitor starts to charge through the VIN pin. When the VCC pin voltage is charged to 5V, the converter starts. Then, the path between the VCC pin and VIN is disconnected, and the voltage of the VCC pin is discharged through the operating current of the controller. When the VCC voltage is lower than 4V, the path between VCC and VIN is reconnected, and VIN charges VCC again. The voltage on the VCC pin is between 4V and 5V, repeating this ramp cycle. For the controller to work stably, it is recommended to connect a capacitor of no less than 1uF to the VCC pin. The VCC pin can provide no less than 4V power through the auxiliary winding to reduce the
loss of the startup circuit. In order to prevent the DCDC converter from starting before the PD conduction tube is fully turned on, the LINE pin can be used to control the enable/disable of the DC-DC converter. The LINE pin signal can be controlled by the PG to prevent the DC-DC from starting during the period when the PD charges the capacitor and generates an inrush current.

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Error Amplifier

The DC-DC converter has a built-in error amplifier. The positive phase terminal of the amplifier is connected to the 1.21V reference voltage, and the reverse phase terminal is connected to the feedback voltage. The output voltage divider is connected to the FB pin through a resistor feedback network or an opto-coupler. The following figure shows the common error amplifier design.

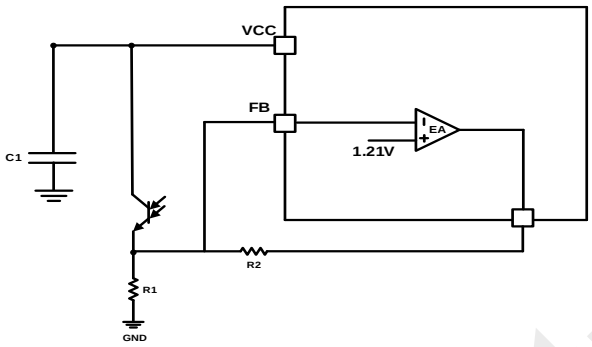

Figure 2 Error Amplifier Design

Undervoltage and Overvoltage Detection

The DC converter has a bus voltage monitoring circuit. Two external resistors divide the voltage from VIN to GND, and the voltage dividing point is connected to the LINE pin. When the voltage on the LINE pin is between 1.21V and 3V, the controller works normally; when the voltage on the LINE pin exceeds this range. The controller shuts down and enters the standby state. The LINE pin can also be used as a remote enable. Ground the LINE pin when the controller is disabled.

Maximum Duty Cycle Limit

When the LINE voltage is equal to 1.3V, the converter's maximum duty cycle D_{MAX} is limited to 67.5%. The relationship between the maximum duty cycle and the LINE voltage is as follows. As the V_{LINE} voltage increases, D_{MAX} decreases.

$$D_{MAX} = \left[\frac{2.7V}{2.7V + V_{LINE}} \right] \times 100\%$$

The Converter Restarts Automatically

When the auxiliary winding is biased to VCC and feedback occurs in an open loop, the voltage on the VCC pin charges to 5.5V. When the VCC voltage exceeds this threshold voltage, the automatic restart circuit turns off the power switch, the converter is in standby mode, and the VCC pin discharges. When VCC drops to 4V, the startup circuit turns on, charges VCC, and the voltage rises again. When VCC exceeds 5.0V, the charging switch is turned off, and the VCC pin discharges back to 4V through the standby current. After 15 cycles of the VCC voltage ramp between the two threshold voltages, the auto-restart circuit of the converter is disabled, and then the converter starts soft-start again.

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Overcurrent Protection

The converter has a cycle-by-cycle switching current limit function. When the peak current value exceeds the set limit current threshold, the output voltage begins to fall until the FB voltage is below the undervoltage threshold (33% of normal FB voltage). When the FB voltage is lower than the undervoltage threshold, the undervoltage protection triggers, and the DC-DC converter enters hiccup mode (the converter is turned off until the VCC voltage ramp repeats 15 consecutive times between 4V and 5V), and the converter is restarted periodically. This protection mode is particularly effective when the output is short-circuited to ground, and the converter input current can be greatly reduced in the output short-circuit state, alleviating the heat dissipation problem. Once the overcurrent condition is eliminated, the converter can exit hiccup mode.

Thermal Shutdown Protection

The temperature monitoring circuit of TMI7325B, when the converter temperature exceeds the protection threshold, the protection circuit will shut down the controller, when the temperature is lower than the lower threshold, the controller exits the protection state.

PC Board Layout Consideration

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines for reference.

1. Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
2. Bypass ceramic capacitors are suggested to be put close to the VIN Pin.
3. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4. VOUT, SW away from sensitive analog areas such as FB.
5. Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

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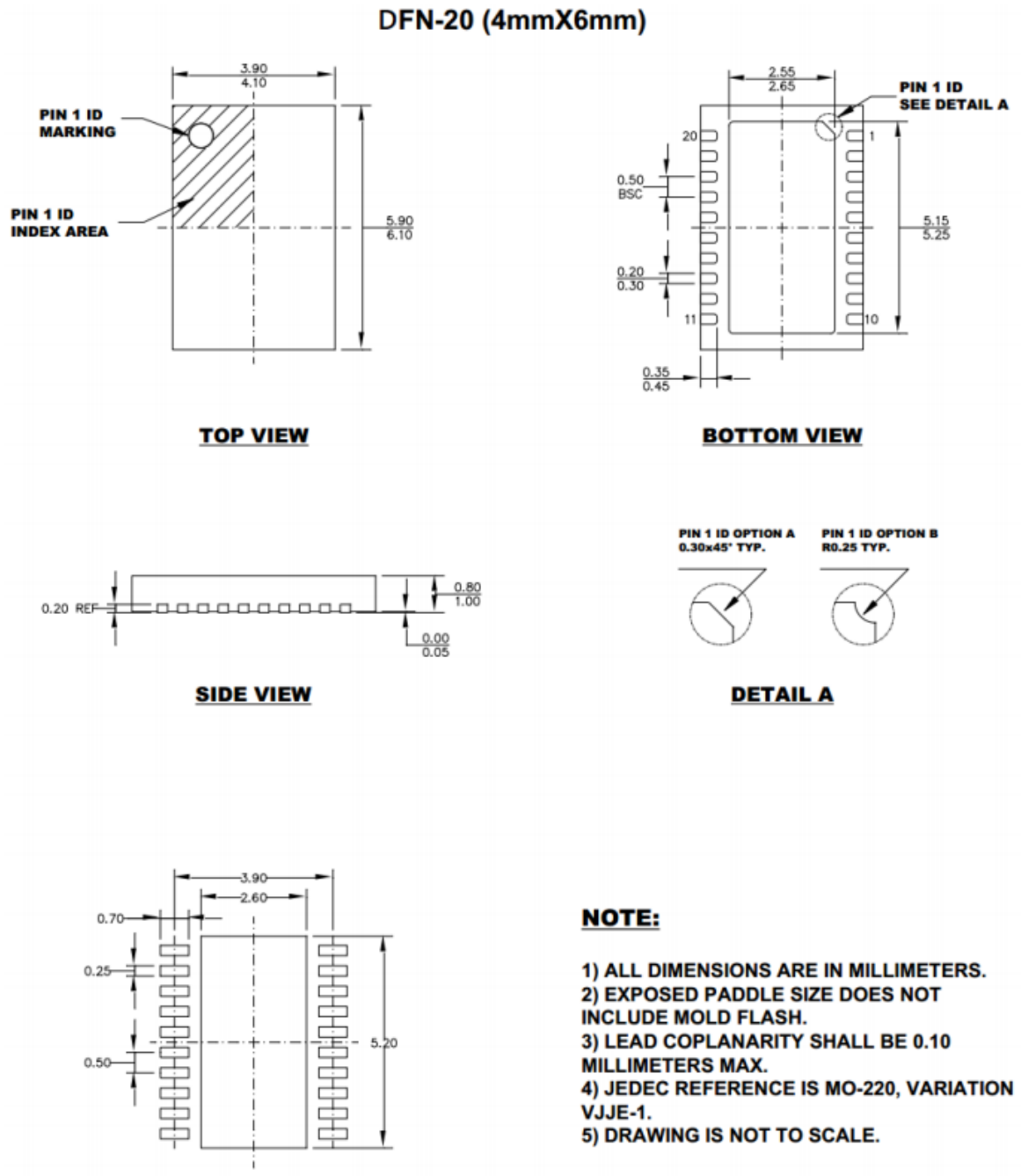
Package Information



Note:

1) All dimensions are in millimeters.

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