

8 nV/√Hz Noise, Precision Instrumentation Amplifier

Features

- Gain Set with One External Resistor (Gain range 1 to 10,000)
- High CMRR: 93 dB min (G = 10)
- Low Input Offset Voltage: 125 μV max
- Low Input Offset Drift: 0.3 μV/°C
- Low Input Bias Current: 0.5 nA max
- Low Noise: 8 nV/√Hz
- 2 μV_{P-P} Input Noise (0.1 Hz to 10 Hz, G = 1)
- Bandwidth: 625 kHz (G = 10)
- Supply Current: 3.3 mA
- Supply Voltage: ±2.4 V to ±18 V
- Specified Temperature Range: -40 °C to +85 °C

Applications

- Precision Data Acquisition
- Instrumentation
- Sensor Signal Conditioning
- Industrial Control
- Communication Systems

General Description

The ZJA3622/ZJA3628 are precision, low-noise instrumentation amplifiers that can be used to set the gain range from 1 to 10,000 with a single external resistor.

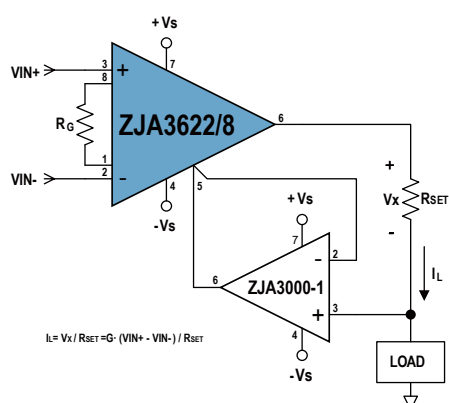
The ZJA3622/ZJA3628 are based on classic three-op-amp structure to provide high common-mode rejection ratio (CMRR) over 93 dB at a gain of 10. This allows it to accurately amplify useful signals in the presence of large external interference, which is a common situation in precision data acquisition, bridge sensor interface, thermocouples, and medical signal acquisition (such as ECG, EEG, etc.).

The ZJA3622/ZJA3628 have excellent dc and ac performances. They have low offset voltage of 125 μV max, offset drift of 0.3 μV/°C, and the bias current is 0.5 nA max, to lower the system calibration cost. The ZJA3622/ZJA3628 work well as a preamplifier due to its low input voltage noise of 8 nV/√Hz at 1 kHz, 2 μV_{P-P} in the 0.1 Hz to 10 Hz band at the gain of 1. Also, the ZJA3622/ZJA3628 are well suited for multiplexed applications with its settling time of 6.3 μs to 0.01 %, slew rate of 2 V/μs and bandwidth of 625 kHz at the gain of 10.

The ZJA3622 gain equation is $G = 1 + 49.4 \text{ k}\Omega/R_G$, while the ZJA3628 is $G = 1 + 50 \text{ k}\Omega/R_G$.

The ZJA3622/ZJA3628 performances are specified over temperature range of -40 °C to +85 °C. Its supply voltage is from ±2.4 V to ±18 V. The ZJA3622/ZJA3628 are available in 8-lead SOIC package.

Application Examples



Typical Performance Characteristics

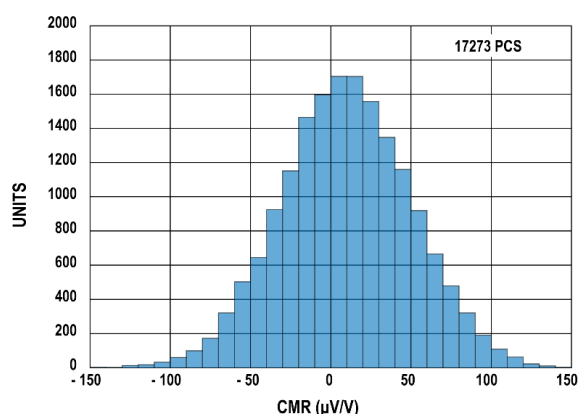


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Version (Release B)¹

Revision History

Nov 2024——Release B

English version

Updated Outline Dimensions, Orderable Device Explanation, Related Parts

August 2023

Format updating

Delete Figure 2 and 5 in Release A

Updated Figure 4, Figure 6, Figure 13, Figure 21, Figure 23 and Figure 35

August 2023 – Release A

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Pin Configurations and Function Descriptions

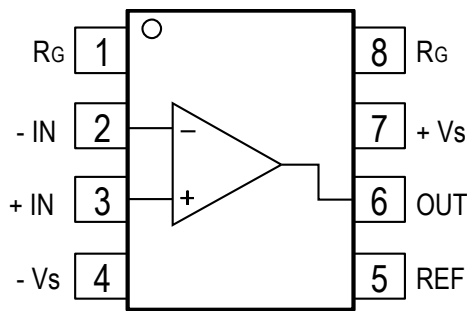


Figure 1. ZJA3622/ZJA3628 Pin Configuration (8-lead SOIC)

Mnemonic	Pin No.	I/O ¹	Description
R _G	1	AI	Gain setting pin. Place a gain resistor between pin 1 and pin 8
-IN	2	AI	Inverting input
+IN	3	AI	Non-inverting input
-V _S	4	P	Negative power supply
REF	5	AI	Reference input. This pin must be driven by a low impedance source
OUT	6	AO	Output
+V _S	7	P	Positive power supply
R _G	8	AI	Gain setting pin. Place a gain resistor between pin 1 and pin 8

¹ AI: Analog Input; P: Power; AO: Analog Output.

Absolute Maximum Ratings ¹

Parameter	Rating
Supply Voltage	±20 V
Input Voltage	±Vs
Input Current ²	±10 mA
Differential Input Voltage (G = 1 to10)	(+Vs) - (-Vs)
Output Short-Circuit Duration to GND ³	Continuous
Operating Temperature Range	-40 °C to 125 °C
Storage Temperature Range	-65 °C to 150 °C
Maximum Reflow Temperature ⁴	150 °C
Lead Temperature, Soldering (10 sec)	260 °C
Electrostatic Discharge (ESD) ⁵	
Human Body Model (HBM) ⁶	3 kV
Charged Device Model (CDM) ⁷	2 kV

Thermal Resistance ⁸

Package Type	θ _{JA}	θ _{JC}	Unit
SOIC-8	158	43	°C/W

¹ These ratings apply at 25 °C, unless otherwise noted. Note that stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

² There are clamping diodes between the input pins and the power pins, and also between each other. When the input signal exceeds the supply rail by 0.3 V, the input current is limited to 10 mA.

³ Limited by Over Temperature Protection (OTP).

⁴ IPC/JEDEC J-STD-020 Compliant

⁵ Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

⁶ ANSI/ESDA/JEDEC JS-001 Compliant

⁷ ANSI/ESDA/JEDEC JS-002 Compliant

⁸ θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the specification which apply over the specified temperature range (- 40 °C to 85 °C), otherwise specifications are at $V_S = \pm 15\text{ V}$, $V_{REF} = 0\text{ V}$, $G = 1$, $R_L = 2\text{ k}\Omega$, $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
GAIN		ZJA3622: $G = 1 + (49.4\text{ k}\Omega/R_G)$ ZJA3628: $G = 1 + (50\text{ k}\Omega/R_G)$					
Gain Range				1		10,000	
Gain Error	GE	$V_{OUT} = \pm 10\text{ V}$					
G = 1				-0.10		0.10	%
G = 10				-0.30		0.30	%
G = 100				-0.30		0.30	%
G = 1,000				-0.70		0.70	%
Gain Nonlinearity		G = 1-100, $V_{OUT} = -10\text{ V to } +10\text{ V}$					
		$R_L = 10\text{ k}\Omega$			10	50	ppm
		$R_L = 2\text{ k}\Omega$			10	95	ppm
Gain vs Temperature		G = 1	●			10	ppm/°C
		G > 1 ¹	●	-50		50	ppm/°C
OFFSET VOLTAGE	V_{OS}	Total Error RTI ($V_{OS,RTI}$) = $V_{OSI} + \frac{V_{OSO}}{G}$					
Input Offset Voltage	V_{OSI}	$V_S = \pm 4.5\text{ V to } \pm 16.5\text{ V}$		-125		125	μV
Average TC	TCV_{OSI}	$V_S = \pm 4.5\text{ V to } \pm 16.5\text{ V}$	●		0.3	1.0	μV/°C
Output Offset Voltage	V_{OSO}	$V_S = \pm 4.5\text{ V to } \pm 16.5\text{ V}$		-1000	200	1000	μV
Average TC	TCV_{OSO}	$V_S = \pm 4.5\text{ V to } \pm 16.5\text{ V}$	●		5	15	μV/°C
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 2.3\text{ V to } \pm 18\text{ V}$					
G = 1				80	100		dB
G = 10				95	120		dB
G = 100				110	140		dB
G = 1,000				110	140		dB
INPUT BIAS CURRENT		$V_S = \pm 16.5\text{ V}$					
Input Bias Current	I_B				0.1	0.5	nA
Average TC			●		3		pA/°C
Input Offset Current	I_{OS}			-0.25		0.25	nA
INPUT CHARACTERISTICS							
Input Impedance	R_{IN}/C_{IN}	Differential Mode			100/2		GΩ/pF
		Common Mode			100/2		GΩ/pF
Input Operating Voltage Range ²	IVR	$V_S = \pm 2.4\text{ V to } \pm 15\text{ V}$		$-V_S + 0.5$		$+V_S - 1.2$	V
Common-ode Rejection Ratio	CMRR						

¹ The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G .

² One input is connected to ground.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
G = 1				73	90		dB
G = 10				93	110		dB
G = 100				110	130		dB
G = 1,000				110	130		dB
OUTPUT CHARACTERISTICS							
Output Swing		V _S = ±2.4 V to ±15 V, R _L = 10 kΩ		-V _S +0.3		+V _S -0.3	V
Short-Circuit Current	I _{SC}	source			90		mA
		sink			50		mA
DYNAMIC PERFORMANCE							
Small Signal Bandwidth, -3 dB		G = 1			3200		kHz
		G = 10			625		kHz
		G = 100			70		kHz
		G = 1,000			9		kHz
Slew Rate	SR			0.75	2		V/μs
Settling Time (to 0.01 %)	t _s	G = 1 to 10, 0 to 10 V step			6.5		μs
		G = 100, 0 to 10 V step			23		μs
		G = 1,000, 0 to 10 V step			213		μs
NOISE PERFORMANCE							
		Referred-To-Input (RTI)= $\sqrt{e_{ni}^2+(e_{no}/G)}$					
Voltage Noise		f = 1 kHz					
Input Voltage Noise	e _{ni}				8		nV/√Hz
Output Voltage Noise	e _{no}				75		nV/√Hz
RTI		f = 0.1 Hz to 10 Hz					
		G = 1			2		μV _{P-P}
		G = 10			0.9		μV _{P-P}
		G = 100			0.9		μV _{P-P}
Input Current Noise		f = 1 kHz			0.8		fA /√Hz
		0.1 Hz to 10 Hz			6		pA _{P-P}
REFERENCE INPUT							
R _{IN}					20		kΩ
I _{IN}		V _S = ±16.5 V			0.03	0.3	μA
Voltage Range				-V _S +0.5		+V _S -1.2	V
Reference Gain to Output					1±0.0001		V/V
POWER SUPPLY							
Operating Range				±2.4		±18	V
Quiescent Current	I _{SY}				3.3	3.8	mA
TEMPERATURE RANGE							
		Specified Temperature Range		-40		85	°C

Typical Performance Characteristics

Unless otherwise stated, $V_S = \pm 15.0\text{ V}$, $I_{\text{LOAD}} = 0$, $C_L = 0.1\text{ }\mu\text{F}$, $T_A = 25\text{ }^\circ\text{C}$.

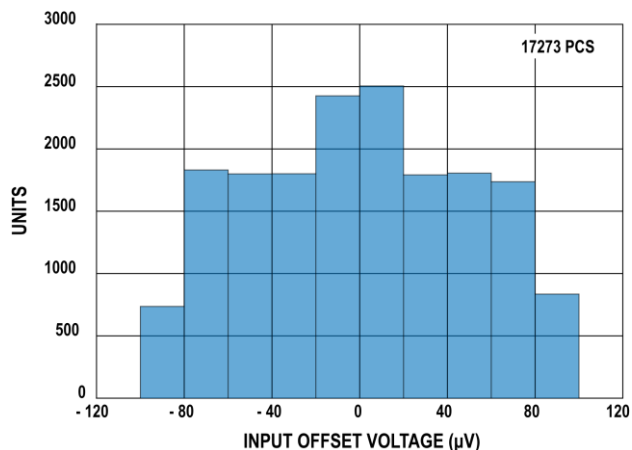


Figure 2. Typical Distribution of Input Offset Voltage V_{OSI}

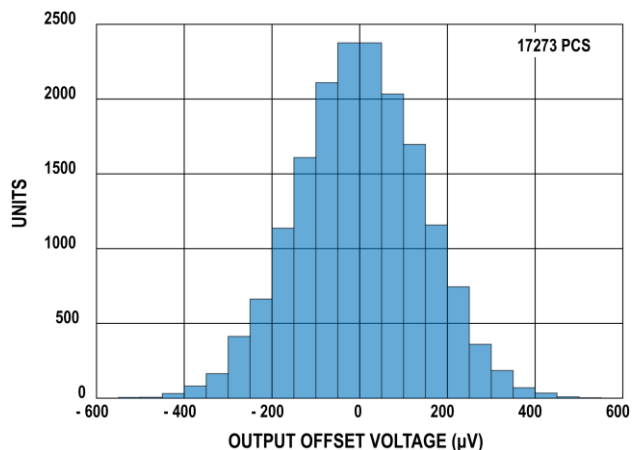


Figure 3. Typical Distribution of Output Offset Voltage V_{OSO}

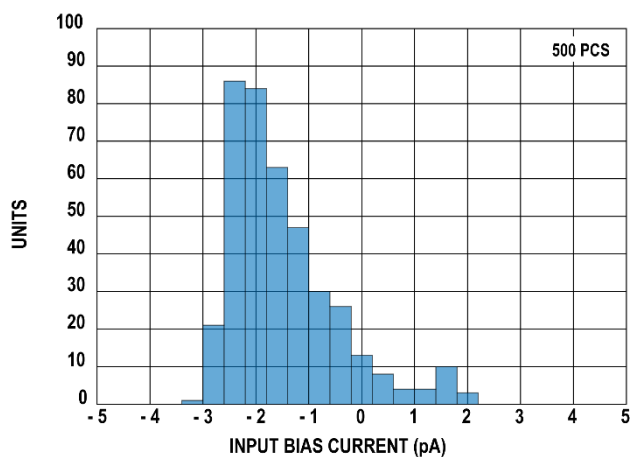


Figure 4. Typical Distribution of Input Bias Current I_{BIAS}

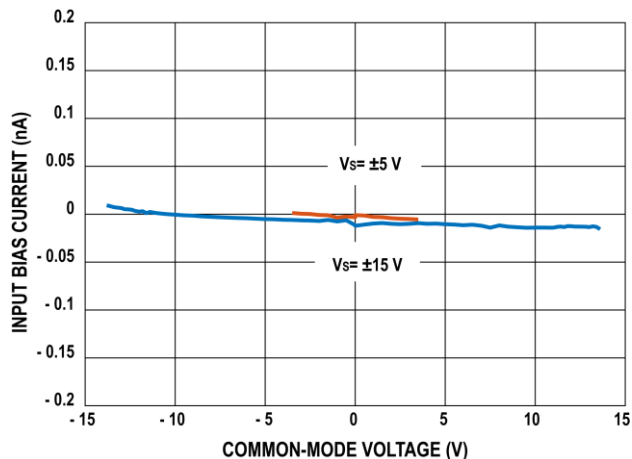


Figure 5. Input Bias Current vs. Common-Mode Voltage

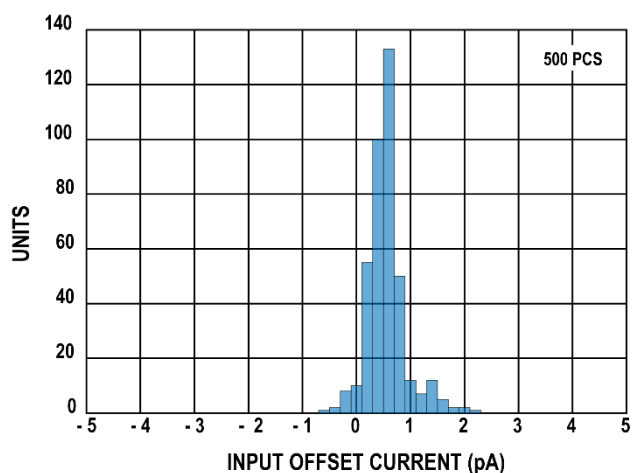


Figure 6. Typical Distribution of Input Offset Current

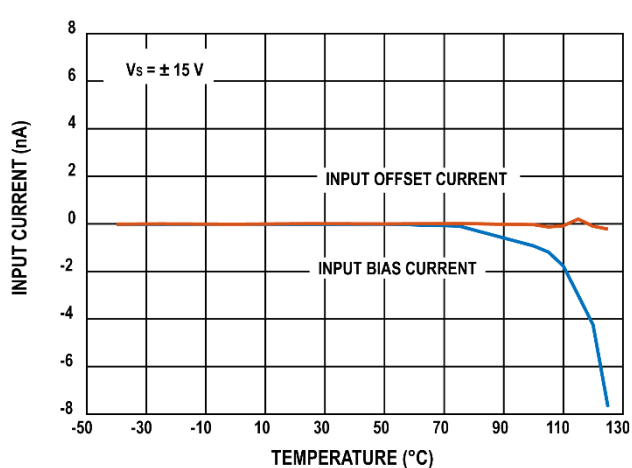


Figure 7. Input Bias Current & Offset Current vs. Temperature

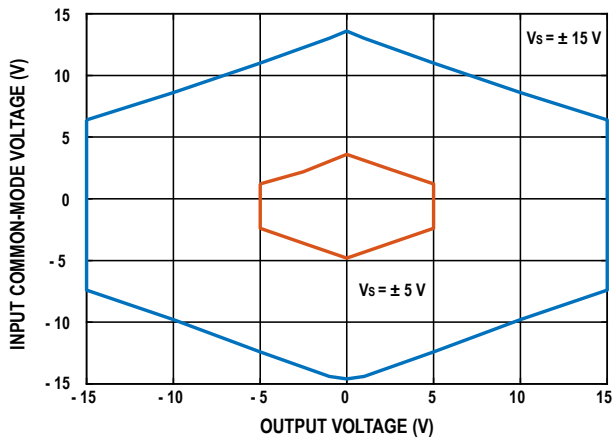


Figure 8. Input Common-Mode Voltage vs. Output Voltage ($G = 1$)

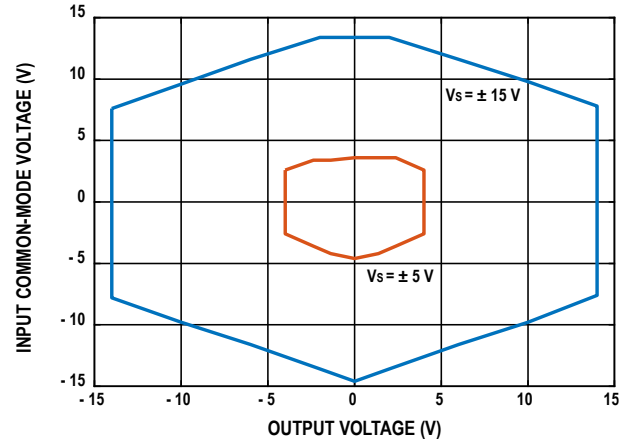


Figure 9. Input Common-Mode Voltage vs. Output Voltage ($G = 100$)

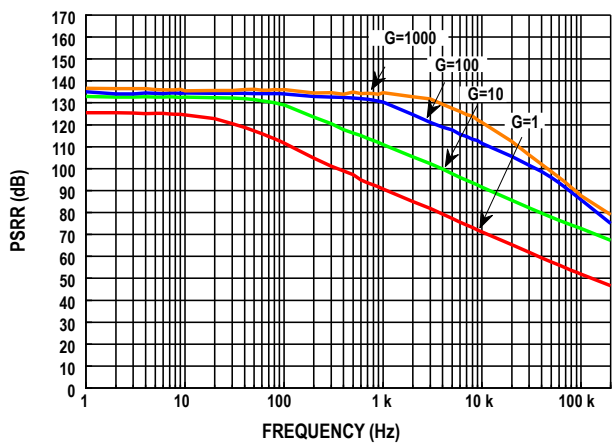


Figure 10. Positive Power Supply Rejection Ratio (PSRR) vs. Frequency, RTI ($G = 1$ to 1000)

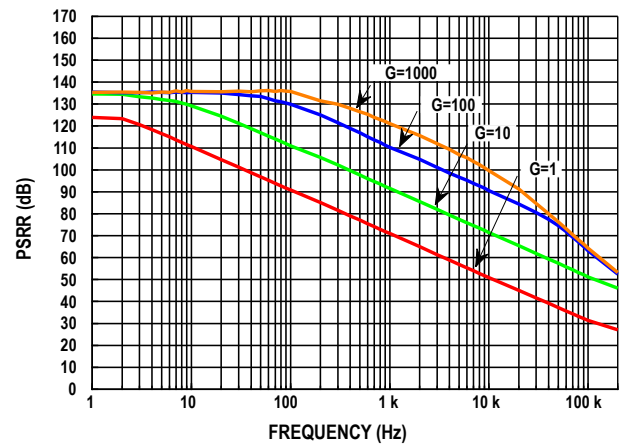


Figure 11. Negative Power Supply Rejection Ratio (PSRR) vs. Frequency, RTI ($G = 1$ to 1000)

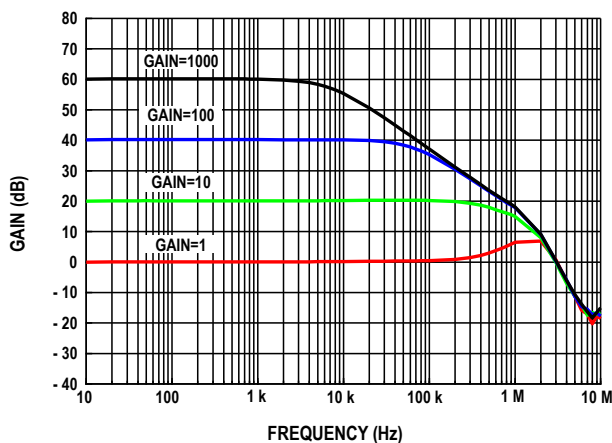


Figure 12. Gain vs. Frequency (RTI)

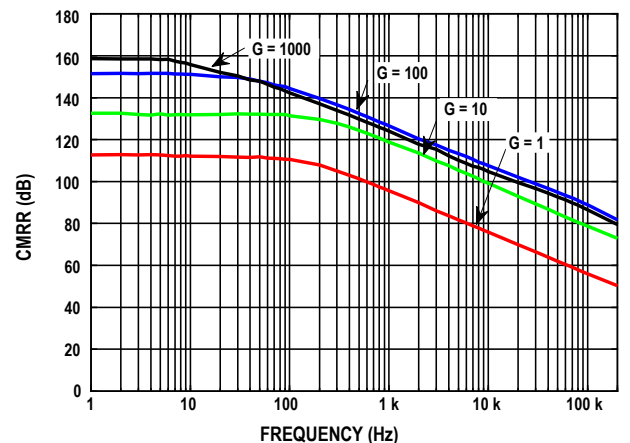


Figure 13. Common Mode Rejection Ratio (CMRR) vs. Frequency (RTI)

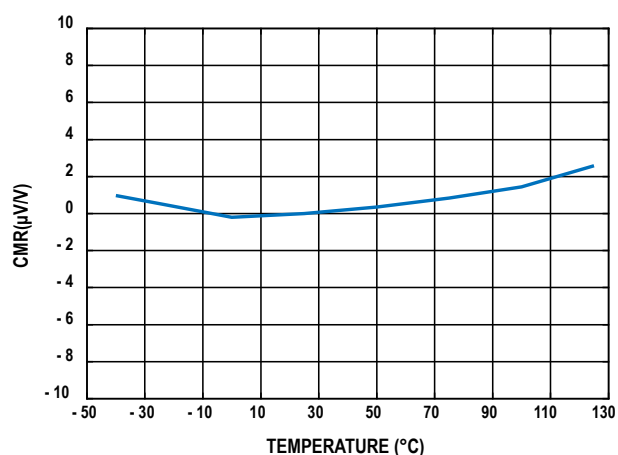


Figure 14. Common Mode Rejection Ratio (CMRR) vs. Temperature

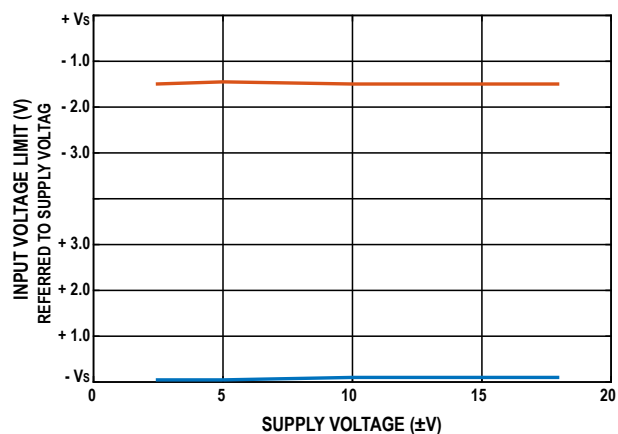


Figure 15. Input Voltage Limit vs. Supply Voltage (G = 1)

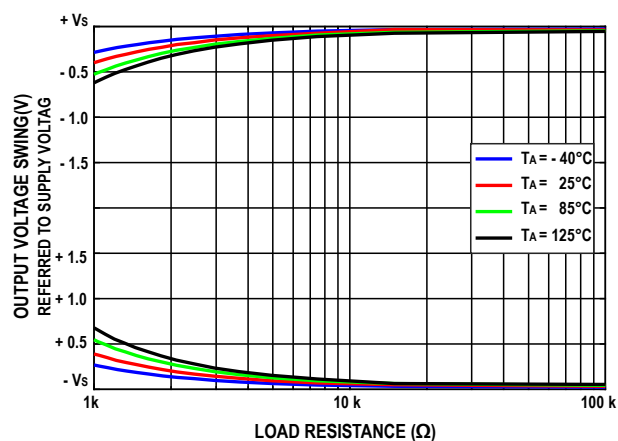


Figure 16. Output Voltage Swing vs. Load Resistance

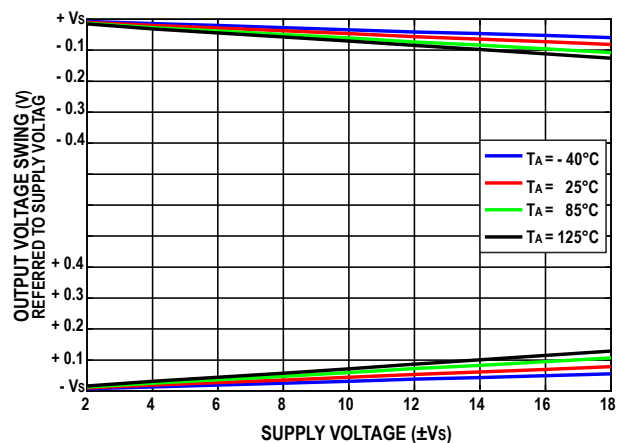
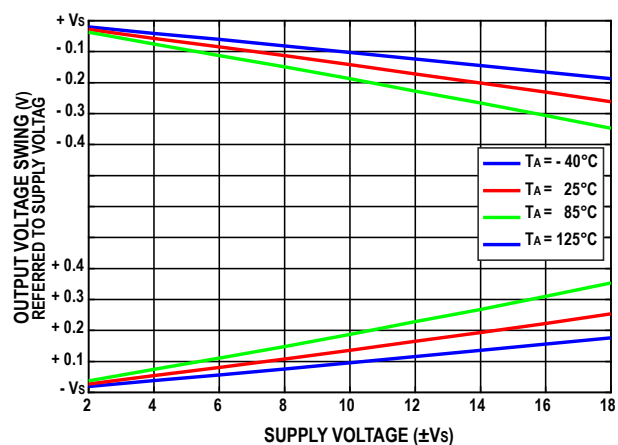
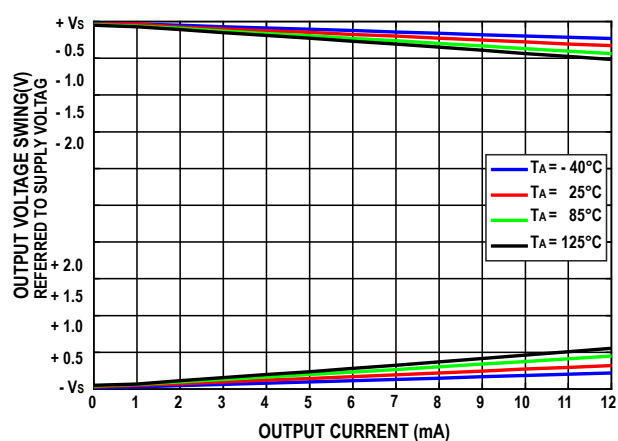
Figure 17. Output Voltage Swing vs. Supply Voltage (G = 1, $R_L = 10\text{ k}\Omega$)Figure 18. Output Voltage Swing vs. Supply Voltage (G = 1, $R_L = 2\text{ k}\Omega$)

Figure 19. Output Voltage Swing vs. Output Current (G = 1)

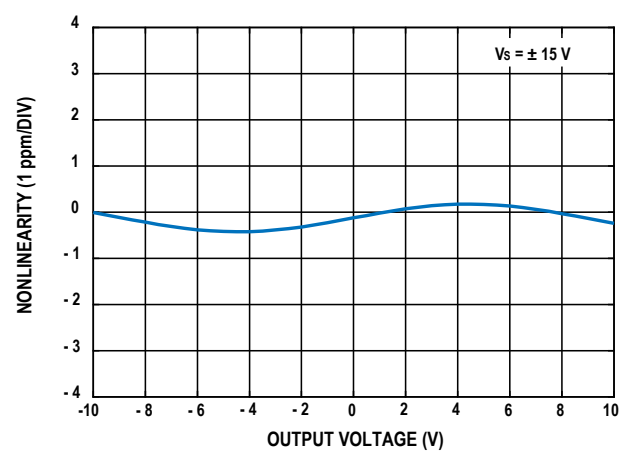


Figure 20. Gain Nonlinearity ($G = 1$, $R_L = 10\text{ k}\Omega$)

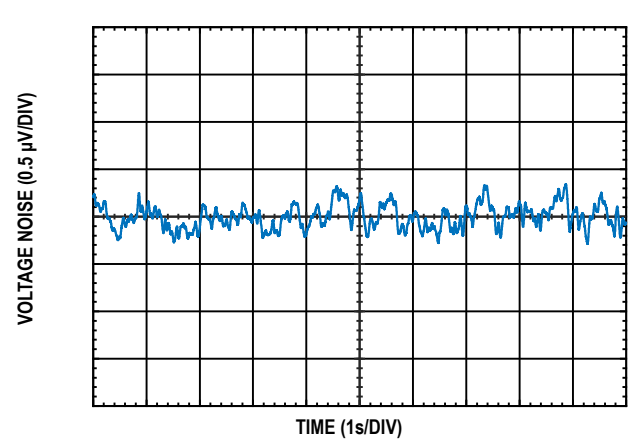


Figure 21. 0.1 Hz to 10 Hz RTI Voltage Noise ($G = 100$)

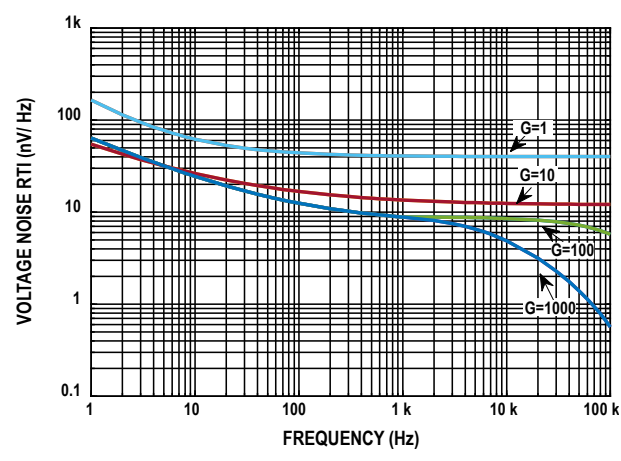


Figure 22. RTI Voltage Noise Spectral Density vs. Frequency ($G = 1$ to 1000)

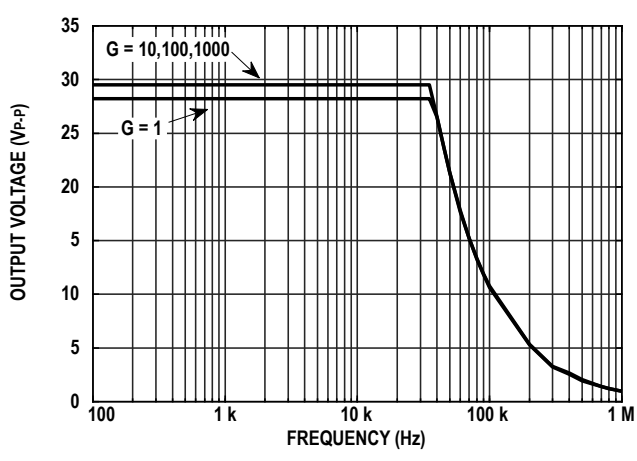


Figure 23. Large Signal Frequency Response

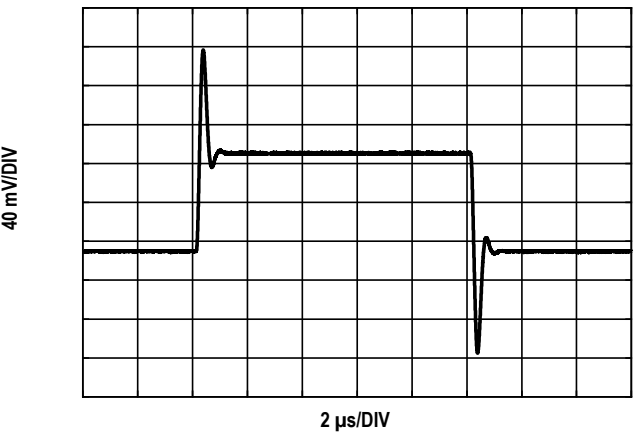


Figure 24. Small Signal Pulse Response ($G = 1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$)

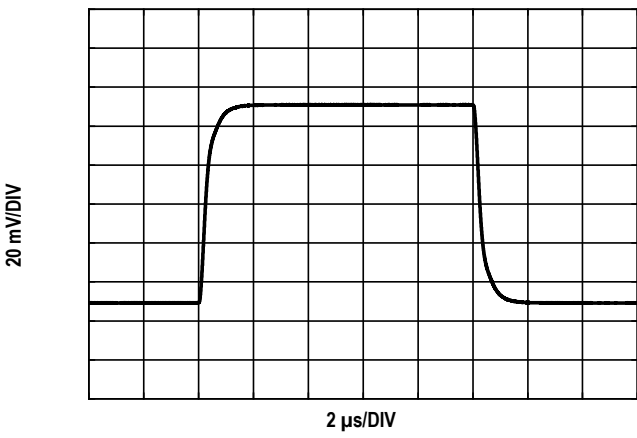
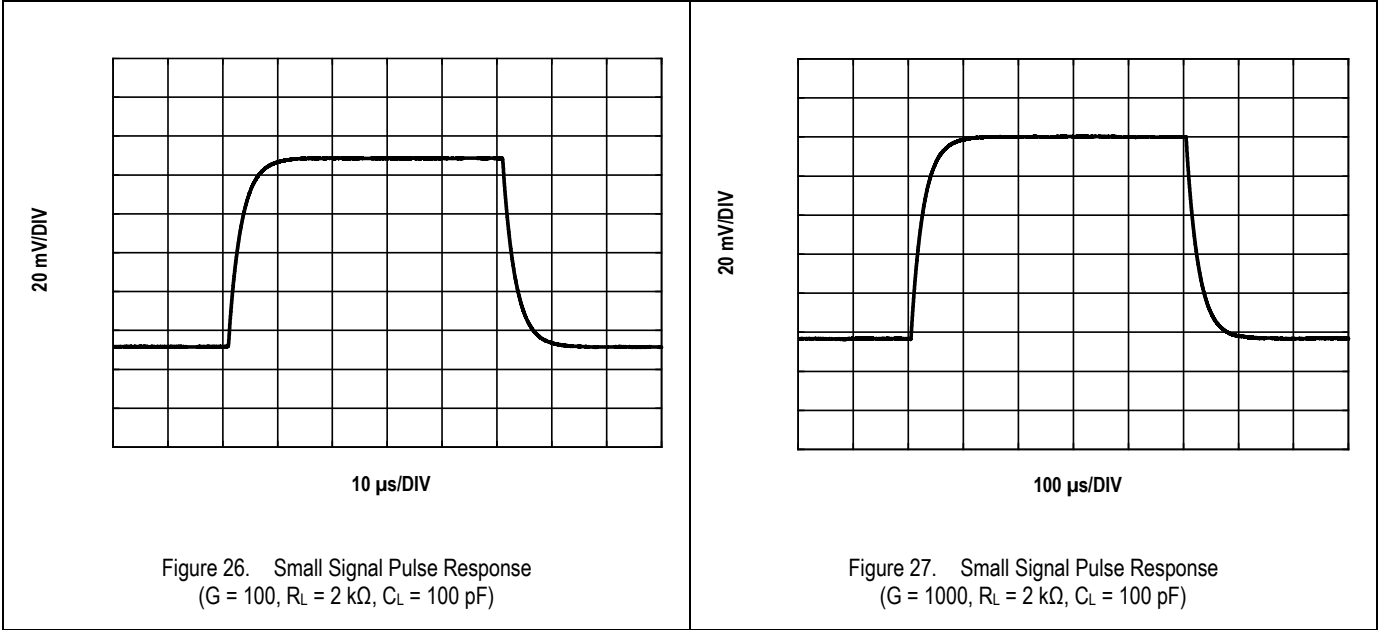


Figure 25. Small Signal Pulse Response ($G = 10$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$)



Theory of Operation

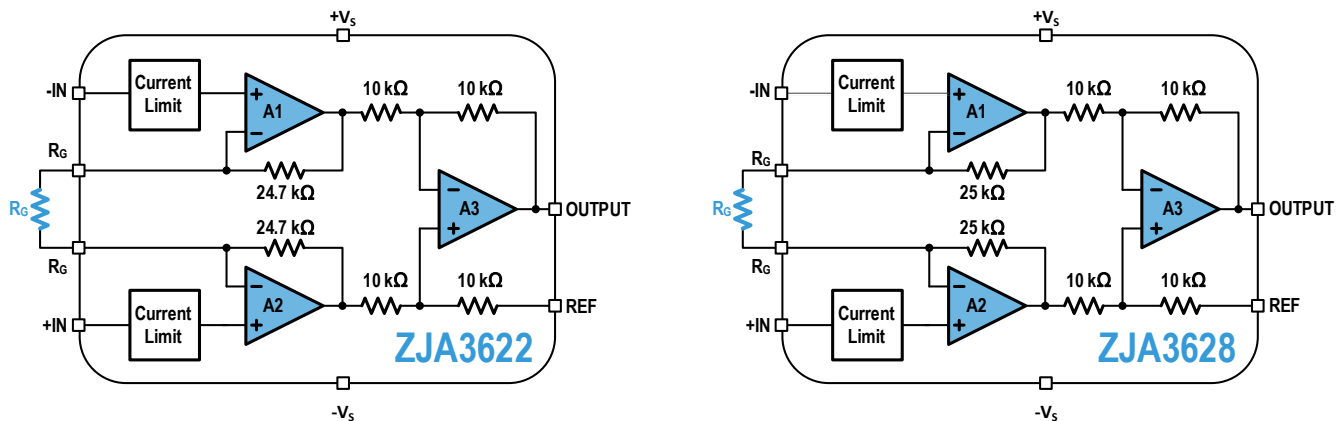


Figure 28. Simplified Schematic of ZJA3622 and ZJA3628

The ZJA3622 and ZJA3628 is a monolithic instrumentation amplifier based on the classic 3-op-amp topology. The input stage consists of amplifiers A1 and A2. The internal gain resistors close to A1 and A2 are trimmed to an absolute value of 24.7 kΩ for ZJA3622 and 25 kΩ for ZJA3628. They are used along with an external resistor R_G to set the gain. The amplified differential and common-mode signals are applied to a difference amplifier that rejects the common-mode voltage but amplifies the differential voltage. The difference amplifier employs innovations that result in low output offset voltage as well as low output offset voltage drift. The proprietary ZHIJINGTRIM® is used to trim these resistors and amplifiers, achieving a highly accurate instrumentation amplifier with gain error less than 0.1 % and CMRR exceeding 93 dB ($G = 10$).

The ZJA3622 and ZJA3628 offers extremely high input impedance, low I_B (below 500 pA at room temperature and symmetrical for +IN and -IN), low I_B drift, low I_{OS} (lower than 1 nA from -40 °C to 85 °C), low input bias current noise, and extremely low voltage noise of 8 nV/ $\sqrt{\text{Hz}}$.

The gain equation of the ZJA3622 is

$$G = 1 + \frac{49.4 \text{ k}\Omega}{R_G}$$

The gain equation of the ZJA3628 is

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G}$$

Users can easily and accurately set the gain using a single standard resistor.

Gain Selection

Placing a resistor across the R_G terminals set the gain of ZJA3622, which can be calculated by referring to Table 1 or by using the gain equation:

$$R_G = \frac{49.4 \text{ k}\Omega}{G - 1}$$

1 % Standard Table Value of R_G (Ω)	Calculated Gain
49.9 k	1.990
12.4 k	4.984
5.49 k	9.998
2.61 k	19.93
1.00 k	50.40
499	100.0
249	199.4
100	495.0
49.9	991.0

0.1 % Standard Table Value of R_G (Ω)	Calculated Gain
49.3 k	2.002
12.4 k	4.984
5.49 k	9.998
2.61 k	19.93
1.01 k	49.91
499	100.0
249	199.4
98.8	501.0
49.3	1003

Table 1. ZJA3622 Commonly-Used Gains and Resistor Values

The ZJA3622 defaults to $G = 1$ when no gain resistor is used.

Same as the ZJA3622, placing a resistor across the R_G terminals set the gain of ZJA3628, which can be calculated by referring to Table 2 or by using the gain equation:

$$R_G = \frac{50 \text{ k}\Omega}{G - 1}$$

1 % Standard Table Value of R_G (Ω)	Calculated Gain
49.9 k	2.002
12.4 k	5.032
5.62 k	9.897
2.61 k	20.16
1.02 k	50.02
511	98.85
249	201.8
100	501.0
49.9	1003

0.1 % Standard Table Value of R_G (Ω)	Calculated Gain
49.9 k	2.002
12.4 k	5.032
5.56 k	9.993
2.64 k	19.94
1.02 k	50.02
505	100.0
252	199.4
100	501.0
49.9	1003

Table 2. ZJA3628 Commonly-Used Gains and Resistor Values

The ZJA3628 defaults to $G = 1$ when no gain resistor is used.

For the ZJA3622/ZJA3628 gain accuracy is determined by the absolute tolerance of R_G . The TC of the external gain resistor increases the gain drift of the instrumentation amplifier. To minimize gain error, avoid high parasitic resistance in series with R_G ; to minimize gain drift, R_G should have a low TC—less than 10 ppm/°C—for the best performance. Gain error and gain drift are kept to a minimum when the gain resistor is not used.

Offset Voltage

The offset voltage of the ZJA3622/ZJA3628 is attributed to two sources, input offset voltage V_{OSI} and output offset voltage V_{OSO} . The V_{OSO} is divided by G when referred to the input. In practice, the V_{OSI} dominates at high gains, and the V_{OSO} dominates at low gains. V_{OSI} includes the offset voltage generated by input amplifiers A1 and A2; V_{OSO} is the offset voltage of amplifier A3. The total V_{OS} for a given gain is calculated as

$$\text{Total Error RTI } (V_{OS,RTI}) = V_{OSI} + \frac{V_{OSO}}{G}$$

$$\text{Total Error RTO } (V_{OS,RTO}) = G * V_{OSI} + V_{OSO}$$

Reference Terminal

The reference terminal REF defines the zero-output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It can interface with pseudo-differential input ADCs easily, for example, ZJC2002 (pseudo-differential unipolar) and ZJC2003 (pseudo-differential bipolar).

The REF pin should not exceed either $+V_S$ or $-V_S$ by more than 1.2 V. And as shown in Figure 28, it connects to one terminal of the trimmed 10 k Ω resistor. For best performance, source impedance to the REF terminal should be kept low, because parasitic resistance can adversely affect CMRR and gain accuracy. If the REF terminal is not connected to a clean and low-impedance system ground, it is generally recommended to add a precision op-amp buffer, such as ZJA3000-1, between the REF terminal and the signal source to obtain the best performance. This is how the typical applications in Figure 33 is handled.

Input Protection

Instrumentation amplifiers like ZJA3622/ZJA3628 are normally put in the very front of the system, thus its input protection is critical. The ZJA3622/ZJA3628 features 3 kV HBM ESD. For input overloads beyond the supplies, clamping the inputs to the supplies (using a low leakage diode such as an BAV99) will reduce the required resistance, yielding lower noise. Make sure short routing distance between the diodes and the input pins.

Input Bias Current Return Path

The input bias current of the ZJA3622/ZJA3628 must have a return path to common. When the source, such as a thermocouple, cannot provide a return current path, one should be created, as shown in Figure 29 and Figure 30.

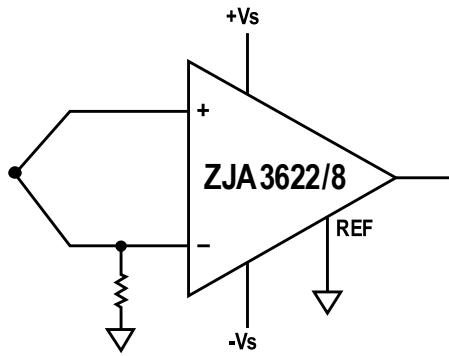


Figure 29. ZJA3622/3628 Interfaces with Thermocouple

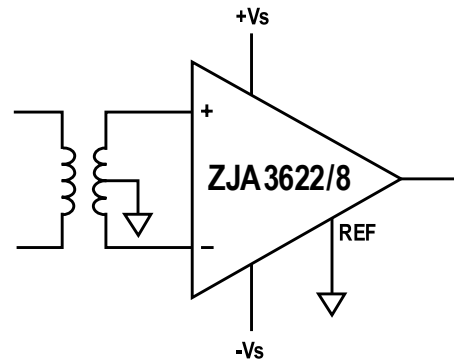


Figure 30. ZJA3622/3628 Interfaces with Transformer

When using ZJA3622 and ZJA3628 for AC coupling, it is important to provide a return path to the input AC coupling capacitors. Otherwise, the input offset voltage will accumulate due to parasitic leakage and input currents, potentially causing the output to lock to a fixed voltage near the power rail. Figure 31 shows the correct connection for AC coupling, which utilizes a high-pass filter with a cutoff frequency determined by RC. And due to the differential inputs, the matching of R and C is crucial.

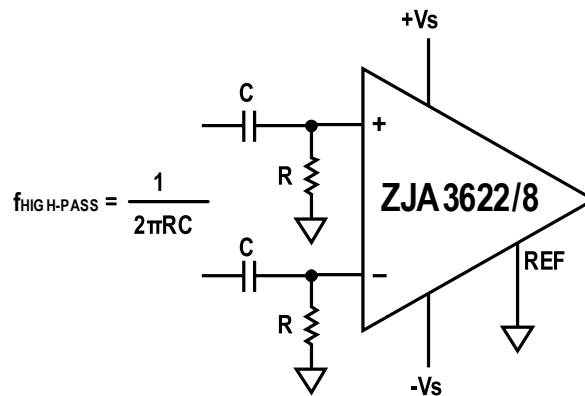


Figure 31. ZJA3622/3628 in AC Coupling Connection

Power Supply Regulation and Bypassing

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. Bypass capacitors should be used to decouple the amplifier.

A low ESR 0.1 μF capacitor should be placed close to each supply pin. High-quality surface-mount ceramic capacitors (such as X5R or X7R) are recommended. As shown in Figure 32, a 10 μF tantalum capacitor can be used, and in most cases, it can be shared by other precision integrated circuits. Refer to the Layout Example section for specific layout examples.

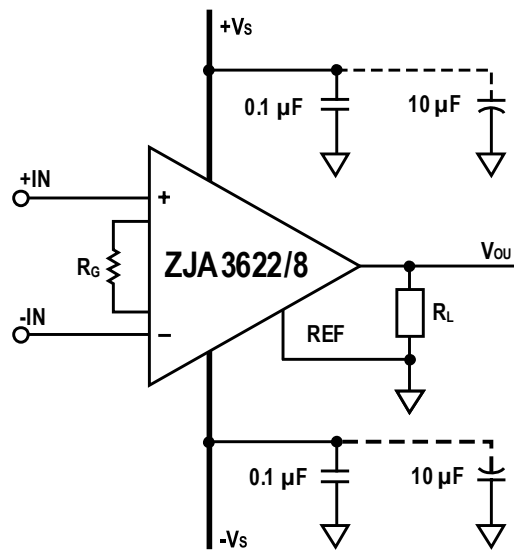


Figure 32. Supply Decoupling, REF, and Output Referred to Local Ground

Although the ZJA3622 and ZJA3628 is a very reliable chip with certain protection functions, it is generally recommended to power on the ZJA3622 and ZJA3628 before applying the input signals.

Grounding

Star grounding is recommended for the ZJA3622 and ZJA3628 circuit, as shown in Figure 32. Maintain low impedance for the REF pin because the output voltage of the ZJA3622 and ZJA3628 is developed with respect to the potential on the REF. Place the decoupling capacitors as close to the power pins as possible to minimize the loop area.

In a multilayer PCB, use a large area ground plane if possible. Place analog signals on the layer above the ground plane.

In mixed-signal environments, low level analog signals need to be isolated from the noisy digital environment. Modern precision SAR ADCs have separate analog and digital ground, and they are all connected to the analog ground. When used with this type of ADC, the ZJA3622 and ZJA3628 uses the analog ground as the reference.

The ZJA3622 and ZJA3628 has a low bias current. To reduce leakage current, it is recommended to remove the ground plane below the signal traces of the two inputs.

ZJA3622 and ZJA3628 Comparison to Zero-drift Instrumentation Amplifiers

ZJA3622 and ZJA3628 is a continuous-signal processing instrumentation amplifier, unlike chopping/auto-zero-based zero-drift amplifiers reliant on non-continuous switch-based technology. These amplifiers contain a sampling capacitor at the input, causing the input bias current to exhibit periodic glitches invisible in datasheets due to averaging. Eliminating these glitches requires an output filter, significantly limiting their usable bandwidth and often restricting them to DC and near-DC signals. Adding a filter also adds complexity to system design. Additionally, tolerance of their internal sampling capacitors leads to variations in glitch amplitude across different ICs. More critically, their linearity (THD & THD+N) is often not great. While they may boast better low-frequency noise, this comes at the cost of transferring noise to the switching frequency, resulting in a noisy spectrum with large spike components.

Consequently, their overall noise performance is often inferior to high-performance continuous sampling amplifiers like the ZJA3622 and ZJA3628.

Furthermore, the usable bandwidth of zero-drift amplifiers is typically only 1/10 or 1/100 of what their datasheets suggest, severely limiting their usability. Their settling time and overload recovery time are also often much longer, making them unsuitable for multi-channel switching or applications with dynamic performance requirements.

Applications and Implementation

Building Precision Current Source with ZJA3622/ZJA3628

Figure 33 illustrates the construction of a precision current source using a single ZJA3622 or ZJA3628 instrumentation amplifier, one ZJA3000-1 precision operational amplifier and two resistors. This design offers flexibility with a supply voltage range of ± 2.4 V to ± 18 V. The ZJA3622 or ZJA3628 characteristics simplify setting the circuit's current output. The actual current output is equal to the set value minus the input bias current of the ZJA3000, which is within 25 pA at room temperature, making it often negligible.

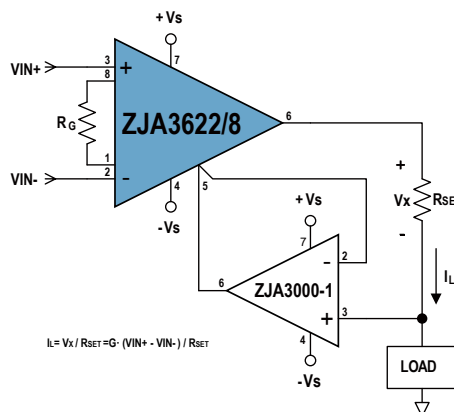


Figure 33. Building Precision Current Source with ZJA3622 or ZJA3628

Precision Current Sensing

The ZJA3622/ZJA3628 are often used for precision current sensing due to its high accuracy, wide bandwidth, low input bias current, and ease of use. As shown in Figure 34, the shunt resistor R_s is typically low, possibly a few Ohms, or even in the m Ω range. The ZJA3622/ZJA3628's high input impedance and input bias current of 0.5 nA max allow it to detect currents as low as 5 nA; its low-frequency noise of 0.9 μ V_{P-P} allows it to detect μ V-level signals. The ZJA3622/ZJA3628 have a wide input range, allowing it to accurately measure input signals with a large dynamic range from μ V to several volts. In general, current changes rapidly, so the ZJA3622/ZJA3628's wide bandwidth is very suitable. This is particularly beneficial in applications like motor control or battery monitoring, where current can fluctuate rapidly. On the other hand, the voltage V_m can be a high voltage varying at a certain frequency. In this case, the ZJA3622/ZJA3628's high CMRR is critical for accuracy.

For applications that require long-term operation and large environmental temperature changes, the ZJA3622/ZJA3628's long-term stability and temperature drift characteristics are very valuable, making the design simpler and more reliable.

In some applications, the signal dynamic range is too big, and the accuracy or linearity of the instrumentation amplifier must be sacrificed by changing R_G to meet the needs of measuring the entire dynamic range. In this case, using digital potentiometers (digi-POTs) is not a good solution, because their temperature characteristics are often not very good. Engineers may consider the series and parallel connection of precision resistors, utilizing relays with good temperature characteristics to switch between ranges. Attention should be paid to wiring in such configurations.

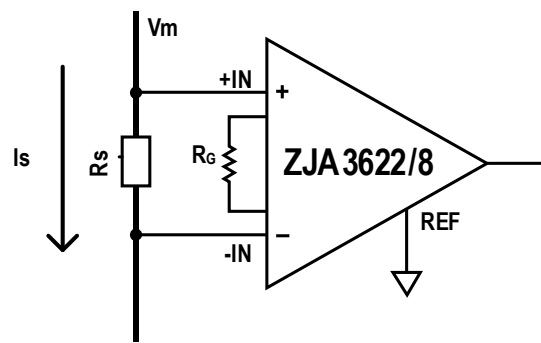


Figure 34. Using ZJA3622/ZJA3628 for Precision Current Sensing

In precision current sensing, if a zero-drift instrumentation amplifier is used, the offset voltage caused by bias current glitch and high-frequency noise will limit the minimum detectable current, thereby limiting the detection accuracy. The available bandwidth of a zero-drift instrumentation amplifier is typically 1/10 to 1/100 of its data sheet bandwidth, which limits the available bandwidth of the current to be measured. This can often make it difficult to keep up with fast-changing currents, resulting in missed information or limiting the bandwidth of closed-loop systems. The longer settling time and lower slew rate of zero-drift instrumentation amplifiers will reduce the system's response speed. The poor linearity of zero-drift instrumentation amplifiers can make the design of control systems difficult or even impossible.

The ZJA3622 and ZJA3628 is a good choice for precision current sensing applications. It offers a combination of high accuracy, wide bandwidth, low input bias current, and ease of use that is not available in other instrumentation amplifiers.

Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85 °C for 30 minutes is sufficient for most circumstances.

Layout Example

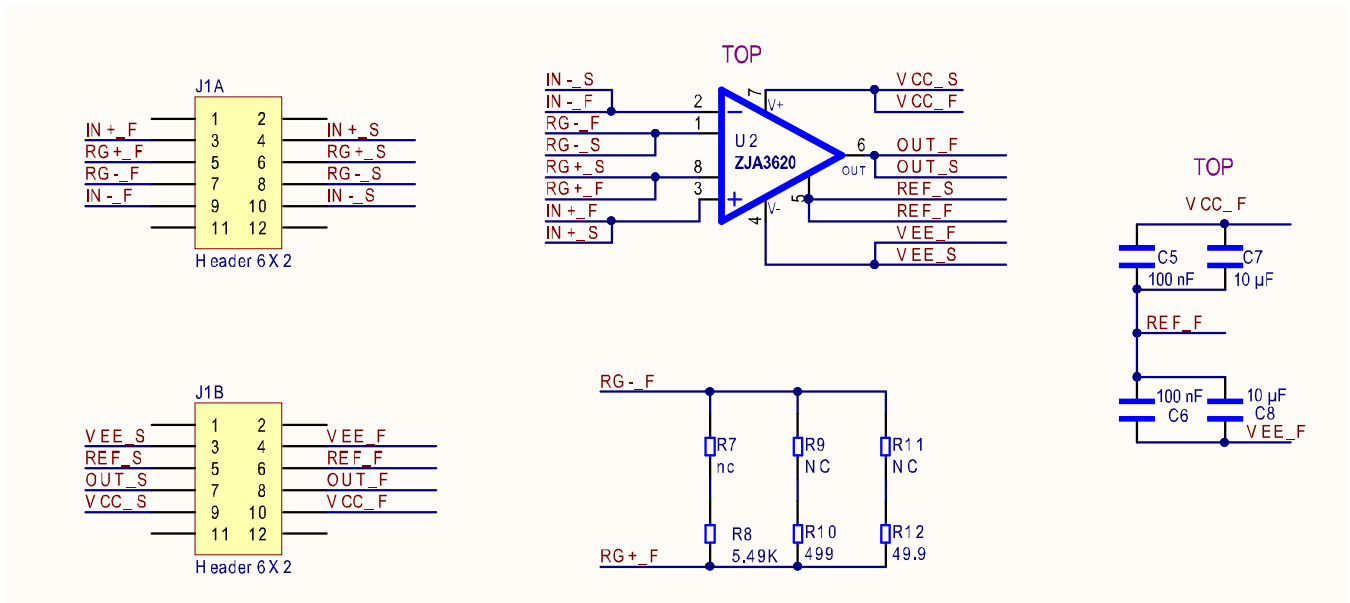


Figure 35. ZJA3620/3622/3628 Evaluation Board Schematic

The ZJA3622, ZJA3628 and ZJA3620 share the same evaluation board. During evaluation, a Kelvin connection, as shown in Figure 35, is typically not necessary. R7, R9, and R11 can be connected as needed, while R8, R10, and R12 can be selected based on the desired gain. In most cases, one of these paths is sufficient. For example, R7 could be set to 0 Ω , and R8 could be assigned the resistance value calculated for the desired gain.

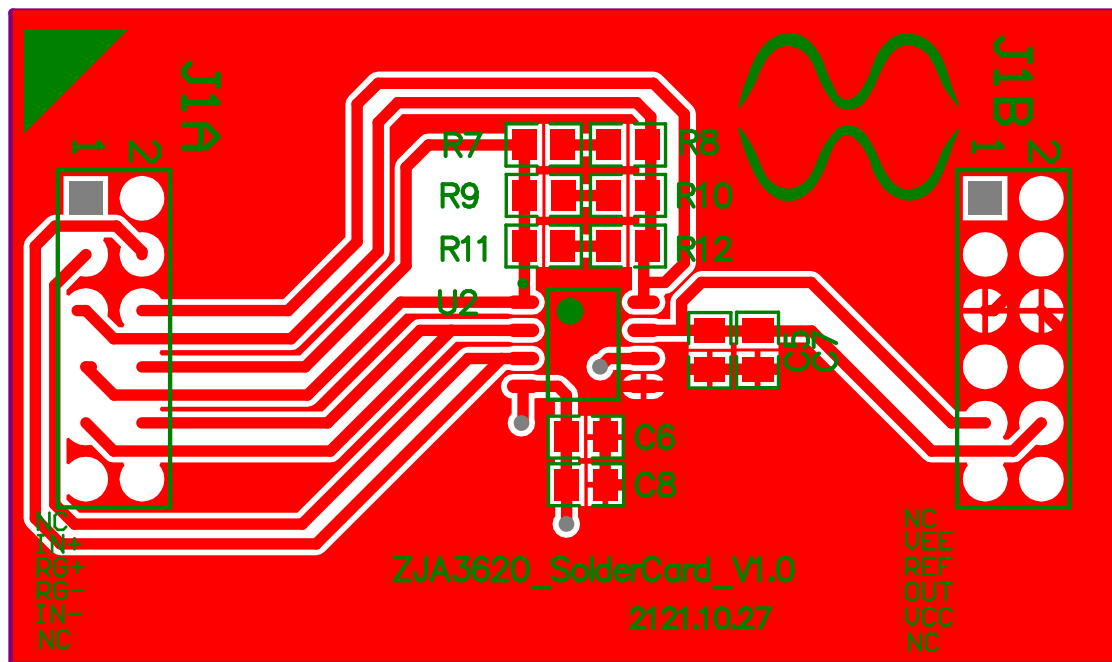


Figure 36. Layout of ZJA3620/3622/3628 Evaluation Board (Top Layer)

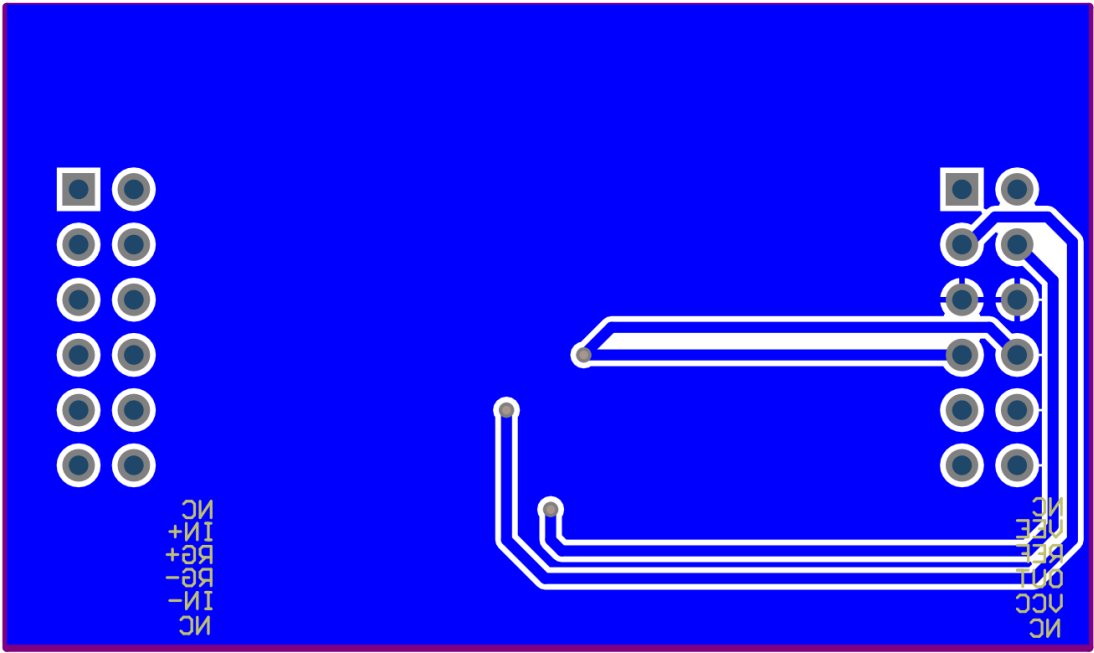


Figure 37. Layout of ZJA3620/3622/3628 Evaluation Board (Bottom Layer)

Outline Dimensions

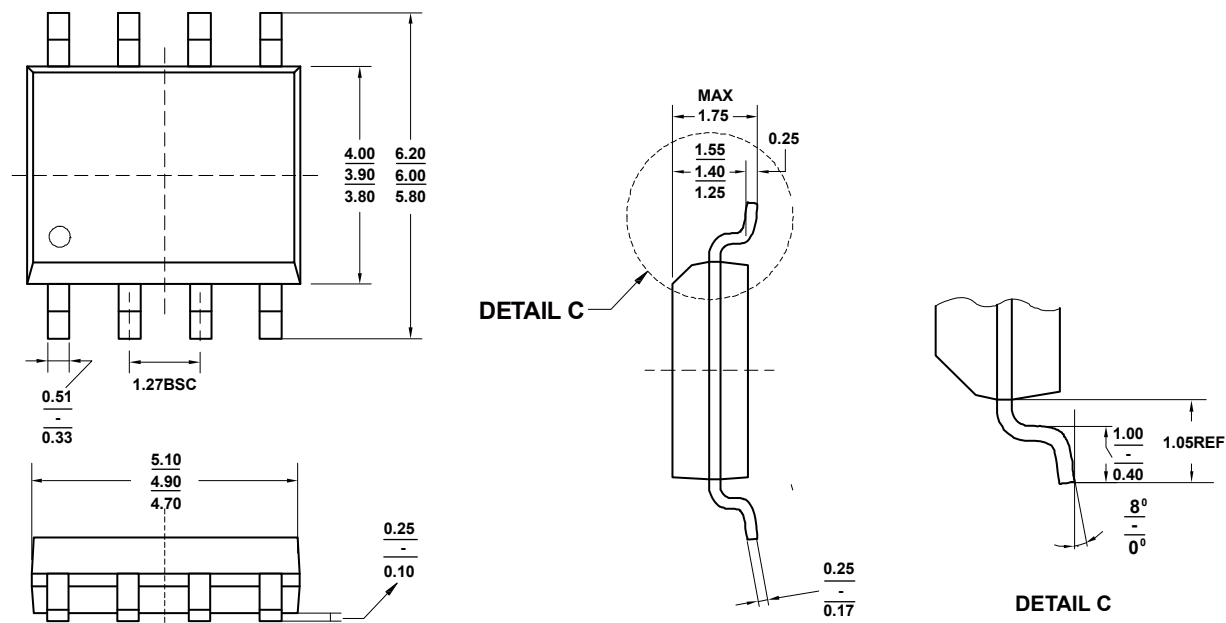


Figure 38. 8-Lead SOIC Package Dimensions shown in millimeters

Ordering Guide

Model	Package	Orderable Device	Status ¹	Temperature Range (°C)	Gain	External Package
ZJA3622	SOIC-8	ZJA3622ASAET	ACTIVE	-40 to 85	$R_G = \frac{49.4 \text{ k}\Omega}{G - 1}$	Tube
		ZJA3622ASAER	ACTIVE	-40 to 85		13" reel
ZJA3628	SOIC-8	ZJA3628ASAET	ACTIVE	-40 to 85	$R_G = \frac{50 \text{ k}\Omega}{G - 1}$	Tube
		ZJA3628ASAER	ACTIVE	-40 to 85		13" reel
ZJA3622/8 Evaluation Board		ZJA362XSAE-EVAL-R	/	25	/	/

Product Order Model

ZJXXXXX X X X X Q1

Q1: Automotive Grade

External package: T=Tube; R=Reel

Temperature range: A= -40°C to 125°C Automotive Grade 1; B= -40°C to 125°C; E= -40°C to 85°C

Number of pins: R=3; K=5; T=6, A=8; B=10; D=14; E=16; P=20

Package type: S=SOIC; U=MSOP, TSSOP, SOT (3 to 6 pins); T=DFN, QFN; K=SOT (8 pins)

Grade: B grade is better than A grade

Base: R=Voltage reference; A=Amplifier; C=Data Converter; G=Switches and Multiplexers, M=Others

¹ The marketing status values are defined as follows:

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

ACTIVE: Product device recommended for new designs.

NRND: Not recommended for new designs. Device is in production to support existing customers, but ZJW does not recommend using this part in a new design.

LIFEBUY: ZJW has announced that the device will be discontinued, and a lifetime-buy period is in effect.

OBSOLETE: ZJW has discontinued the production of the device.

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2003/2013		Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2005/2015		Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB
ZJC2008/2018		Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2009	Small size, 12-bit 1 MSPS SAR ADC	Single-ended input, SOT23-6, 2.3 V to 5 V, SINAD 73 dB, THD -89 dB
ZJC2100/1-18	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB	
ZJC2100/1-16	16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB	
ZJC2102/3-16	16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
ZJC2102/3-14	14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB	
ZJC2104/5-16	16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or $V_{REF}/2$ (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2543-18/16/14		
ZJC2542-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or $V_{REF}/2$ (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
ZJC2544-18/16/14		
Amplifier		
ZJA3000-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 μ V max Vos, 0.5 μ V/°C max TCvos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3001-1/2/4		
ZJA3018-2	OVP $\pm$ 75 V, 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 μ V max Vos, 0.5 μ V/°C max TCvos, 25 pA max Ibias, 0.5 mA/ch, OVP $\pm$ 75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3008-2		
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/ μ S, 50 μ V max Vos, 1 μ V/°C max TCvos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3217/06/02-1/2	Precision 24/11.6/5.3 MHz CMOS RRIO Op Amps	24/11.6/5.3 MHz, RRIO, 30 μ V max Vos, 1 μ V/°C max TCvos, 0.6 pA lb, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max lb, 25 μ V max Vosi, $\pm$ 2.4 V to $\pm$ 18 V, -40°C to 125°C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G $\geq$ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 μ V max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7	Low power, G = 1 Single/Dual 36 V difference amplifier	Input protection to $\pm$ 65 V, CMRR 104 dB min (G = 1), Vos 100 μ V max, gain error 15 ppm
ZJA3678/9	Low power, G = 0.5/2 Single/Dual 36 V difference amplifier	max, 500 kHz BW (G = 1), 330 μ A/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	$\pm$ 270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/ μ S, 50 nS to 16-bit, 50 μ V max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 22/10/5 MHz CMOS RRIO Op Amps	22/11/5 MHz, RRIO, 2 mV max Vos, 6 μ V/°C max TCvos, 0.6 pA lb, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 μ V max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, $\pm$ 2.4 V to $\pm$ 18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, $\pm$ 0.05% initial error, 130 μ A, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1003		
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to $\pm$ 50 V power on & off, latch-up immune, Ron 270 Ω ,14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω , 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	$\pm$ 75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV