1. Overview and characteri stics

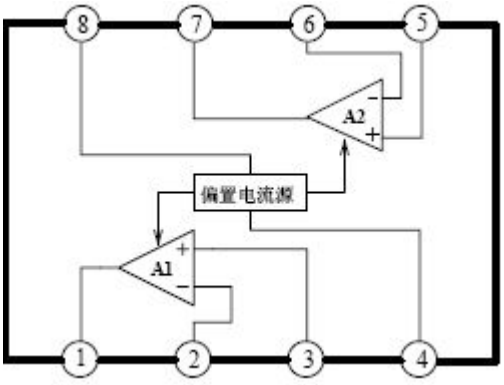
JRC4558 is a low noise dual operational amplifier circuit, which can be used as active filter, compensation amplifier, audio preamplifier, equalization amplifier and linear amplifier in electronic instruments.

Its characteristics are as follows:

- Phase compensation circuit is included;
- Low noise V_{NI}= 2.5uv;
- Speed high frequency bandwidth BW = 3MHz;
- Package form: DIP8 / SOP8;

2. Function block diagram and pin description

2.1 functional block diagram



2. 2 pin description

Pin	Symbol	function	Pin	Symbol	function
1	OUT_1	Output 1	5	IN^{2+}	In phase input 2
2	IN_{1-}	Reverse input 1	6	IN^{2-}	Invert input 2
3	IN_{1+}	In-phase input 1	7	OUT^2	Output 2
4	V_{EE}	Negative power supply	8	V_{CC}	Positive power supply

3. Electrical characteristics

3.1 limit parameters

Tamb = 25℃ unless otherwise specified

Parameter name		Symbol	Rating	Company
supply voltage		V_{CC}/V_{EE}	± 18	V
Differential mode input voltage		V_{ID}	± 30	V
Common mode input voltage		V_{IC}	± 15	V
power waste	DIP	P_D	500	mW
	SOP		360	
Working environment temperature		T_{amb}	-20～70	℃
Storage temperature		T_{stg}	-55～125	℃

3. 2 electrical characteristics

Unless otherwise specified, t_{amb}= 25 ℃, V_{CC}= + 15V, V_{EE}= -15V

Parameter name	symbol	Test conditions	Canonical value			Unit	Figure number
			Min.	Typ.	Max.		
Supply current	Icc			±4.0	±6.0	mA	4.5
Input offset current	I_{IO}			5	200	nA	4.2
Input bias current	I_{IB}			60	500	nA	4.2
Common-mode input voltage	V_{IC}		±12	±14		V	4.3
Maximum output voltage	V_{OM}	R_L=10KΩ	±12	±14		V	4.4
		R_L=2KΩ	±10	±13		V	4.4
Output short-circuit current	I_{OS}			40		mA	4.4
Output sink current	I_{Osink}			40		mA	4.4
Open-loop voltage gain	A_{VO}	V_O=±10V,R_L=2KΩ	86	100		dB	4.7
Common mode rejection ratio	CMRR		70	90		dB	4.3
Supply voltage rejection ratio	K_{SVR}			30	150	uV/V	4.1
Input offset voltage	V_{IO}			0.5	6	mV	4.1
Output voltage slew rate	SR	A_V=1,R_L=2KΩ		1		V/uS	4.6
Unit incremental bandwidth	BW	0dB		3		MHz	4.7
Equivalent input noise voltage	V_{NI}	R_S=1KΩ f=30Hz-30KHz		2.5		uV	

4. Test line

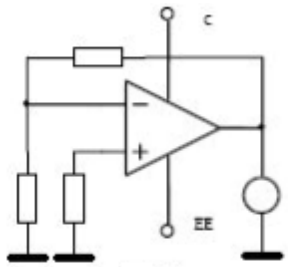


figure 4. 1

$V_{IO}=V_O/100$ (V)
$K_{SVR}=(V_{IO1}-V_{IO2})/5$ (uV/V)
V_{IO1}: $V_{CC}=+17.5V$, $V_{EE}=-17.5V$
V_{IO2}: $V_{CC}=+12.5V$, $V_{EE}=-12.5V$

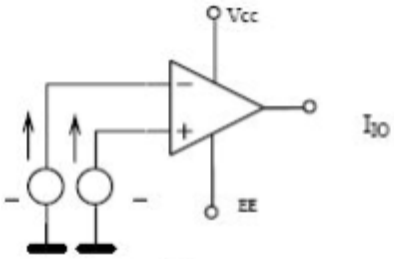


figure 4. 2

$I_{IO}=|I_I(+)-I_I(-)|$

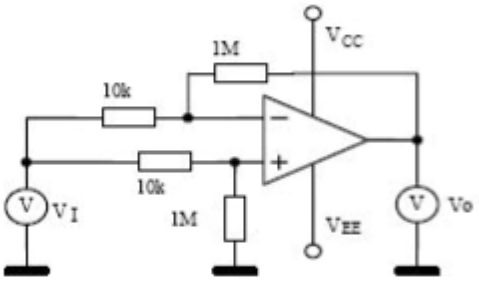


figure 4. 3

V_{IC}: V Positive and negative DC adjustable voltage The DC input voltage when it makes the output voltage 1V

CMRR The ratio of differential-mode voltage gain to common-mode

The switch positions in the left figure are as follows

VOM:

S1=output voltage when S3 is disconnected when BS2 is disconnected

S1=output voltage when S3 is disconnected

S1=output voltage when S3 is disconnected when BS2 is disconnected

S1=output voltage when S3 is disconnected when BS2 is disconnected:

IOS,iosink:

S1=input current when S3 isswitched on when as2 is disconnected,

S1=output current when S3 is switched on when BS2 is disconnected

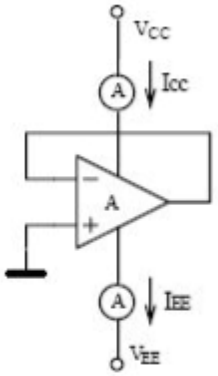


figure4. 5

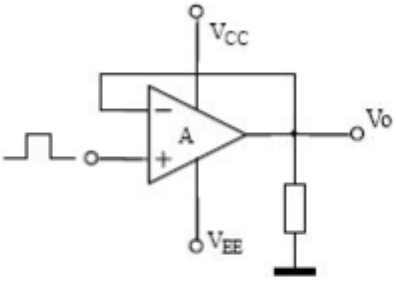


figure 4. 6

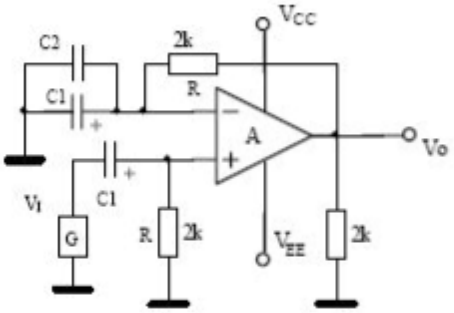
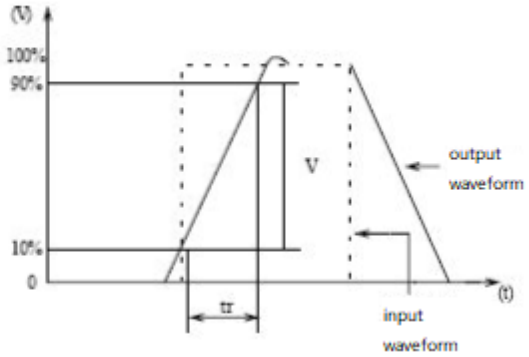


figure 4.7



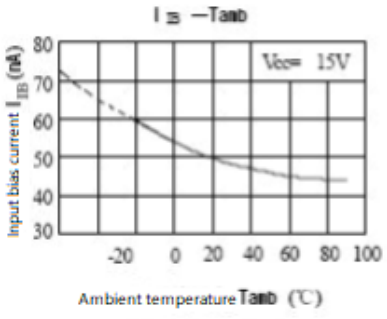
A_{VD} =20log(Vo/V)

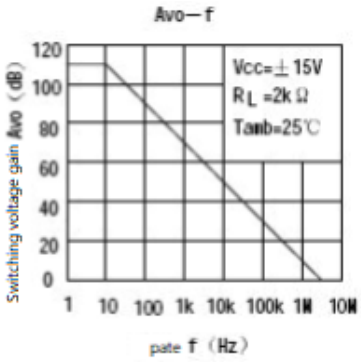
BW is the V frequency at VO = V (MHz)

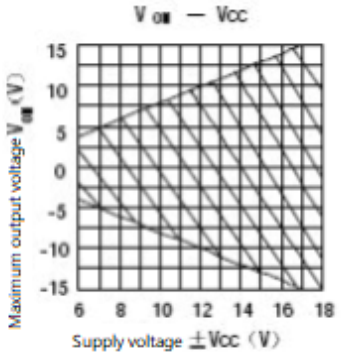
C1: DC isolation capacitor

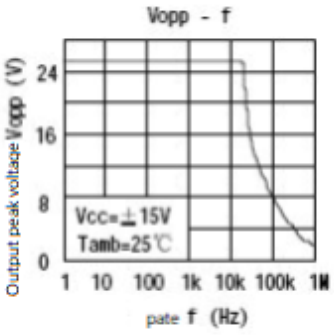
C2: high frequency capacitor of mica foil

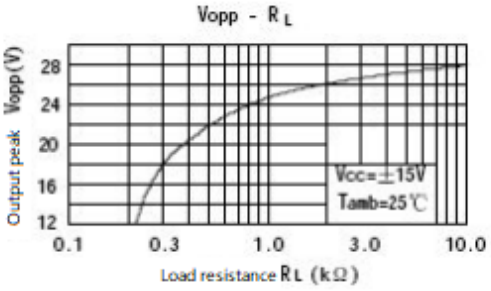
5. Characteristic curve

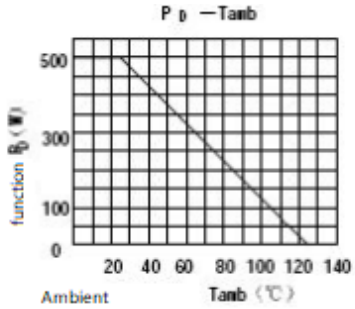




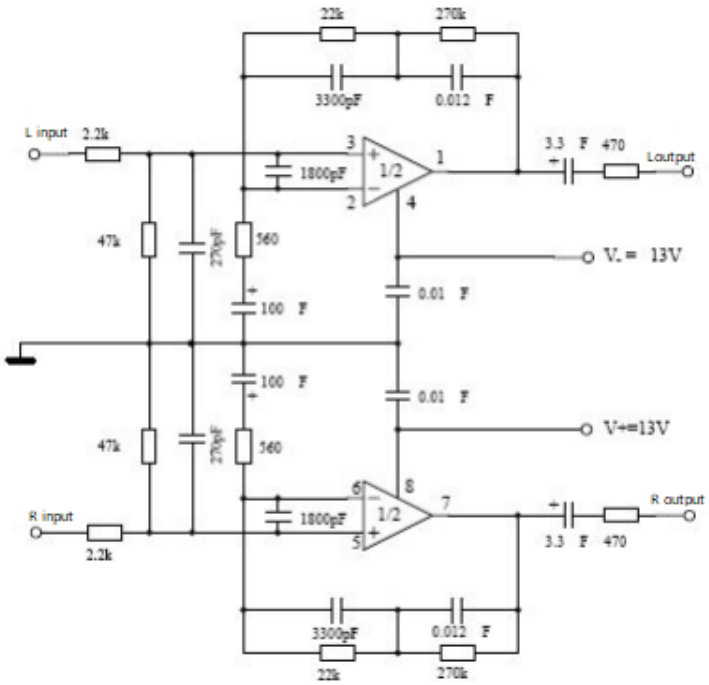






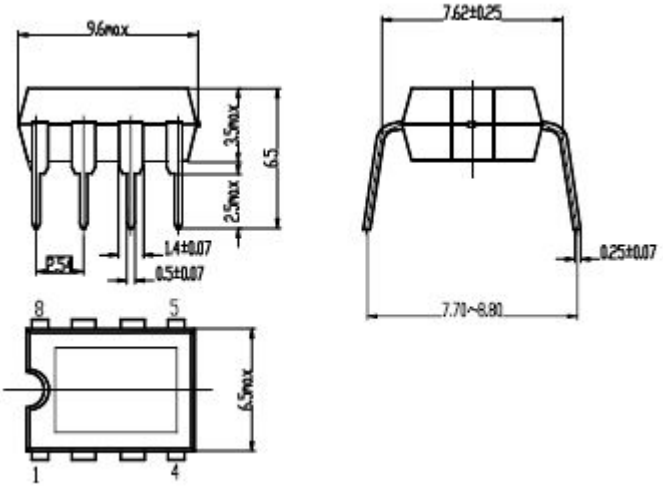


6. Application line



7. Dimensions

7.1 DIP8 package



7.2 SOP8 package