

4 Function Pin Description

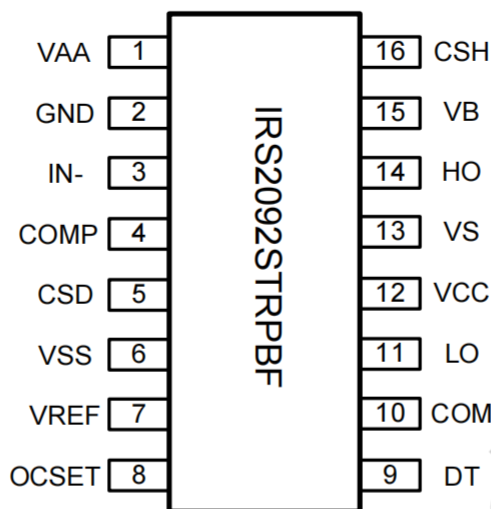


Figure 4-1 16-PinSOIC Topview

Table 4-1 Lead Definitions

PIN NO.	Name	Type	Function
1	VAA	POWER	Floating input positive supply
2	GND	GROUND	Floating input supply return
3	IN-	INPUT	Analog inverting input
4	COMP	OUTPUT	Phase compensation input, comparator input
5	CSD	IN/OUTPUT	Shutdown timing capacitor
6	VSS	POWER	Floating input negative supply
7	VREF	OUTPUT	5V reference voltage to program OCSET pin
8	OCSET	INPUT	Low side over current threshold setting
9	DT	INPUT	Deadtime program input
10	COM	GROUND	Low side supply return
11	LO	OUTPUT	Low side output
12	VCC	POWER	Low side supply
13	VS	GROUND	High side floating supply return
14	HO	OUTPUT	High side output
15	VB	POWER	High side floating supply
16	CSH	INPUT	High side over current sensing input

5 Product specifications

5.1 Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply voltage	-0.3	320	V
V_S	High side floating supply voltage ^{II}	$V_B - 20$	$V_B + 0.3$	
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CSH}	CSH pin input voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low side fixed supply voltage ^{II}	-0.3	20	
V_{LO}	Low side output voltage	-0.3	$V_{CC} + 0.3$	
V_{AA}	Floating input positive supply voltage ^{II}	See I_{AAZ}	310	
V_{SS}	Floating input negative supply voltage ^{II}	-1 See I_{SSZ}	GND+0.3	
V_{GND}	Floating input supply ground voltage	$V_{SS}-0.3$ (See I_{SSZ})	$V_{AA}+0.3$ (See I_{SSZ})	
I_{IN-}	Inverting input current ^I	—	± 3	mA
V_{CSD}	CSD pin input voltage	$V_{SS}-0.3$	$V_{AA}+0.3$	V
V_{COMP}	COMP pin input voltage	$V_{SS}-0.3$	$V_{AA}+0.3$	
V_{DT}	DT pin input voltage	-0.3	$V_{CC}+0.3$	
V_{OCSET}	OCSET pin input voltage	-0.3	$V_{CC}+0.3$	
I_{AAZ}	Floating input positive supply zener clamp current ^{II}	—	20	mA
I_{SSZ}	Floating input negative supply zener clamp current ^{II}	—	20	
I_{CCZ}	Low side supply zener clamp current ^{III}	—	10	
I_{BSZ}	Floating supply zener clamp current ^{III}	—	10	
I_{OREF}	Reference output current	—	5	
dV_S/dt	Allowable V_S voltage slew rate	—	50	V/ns
dV_{SS}/dt	Allowable V_{SS} voltage slew rate ^{III}	—	50	V/ms

I I_{IN-} contains clamping diode to GND.

II $V_{AA}-GND$, $GND-V_{SS}$, $V_{CC}-COM$ and V_B-V_S contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.

III For the rising and falling edges of step signal of 10V. $V_{SS}=15V$ to 300V

5.2 ESD rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	750	—	V
	Machine Model	200	—	V

5.3 Rated power

Symbol	Definition	MIN.	MAX.	Units
P _D	Package Power Dissipation @ TA ≤25°C	—	1	W

5.4 Thermal information

Symbol	Definition	MIN.	MAX.	Units
R _{thJA}	Thermal Resistance, Junction to Ambient	—	115	°C /W
T _J	Junction Temperature	—	150	°C
T _S	Storage Temperature	-55	150	
T _L	Lead Temperature (Soldering, 10 seconds)	—	300	

5.5 Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of V_S and V_{SS} are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to V_{SS} and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 18$	V
V_S	High side floating supply offset voltage	— ^I	300	
I_{AAZ}	Floating input positive supply clamp current	1	11	mA
I_{SSZ}	Floating input negative supply clamp current	1	11	
V_{SS}	Floating input supply absolute voltage	0	300	V
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	18	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{GND}	GND pin input voltage	V_{SS}^{III}	V_{AA}^{III}	
V_{IN-}	Inverting input voltage	$V_{GND} - 0.5$	$V_{GND} + 0.5$	
V_{CSD}	CSD pin input voltage	V_{SS}	V_{AA}	
V_{COMP}	COMP pin input voltage	V_{SS}	V_{AA}	
C_{COMP}	COMP pin phase compensation capacitor to GND	1	—	nF
V_{DT}	DT pin input voltage	0	V_{CC}	V
I_{OREF}	Reference output current to COM ^{II}	0.3	0.8	mA
V_{OCSET}	OCSET pin input voltage	0.5	5	V
V_{CSH}	CSH pin input voltage	V_S	V_B	
dV_{SS}/dt	Allowable V_{SS} voltage slew rate upon power-up ^{IV}	—	50	V/ms
I_{PW}	Input pulse width	10^V	—	ns
f_{SW}	Switching Frequency	—	800	kHz
T_A	Ambient Temperature	-40	125	°C

I Logic operational for V_S equal to -5 V to +300 V. Logic state held for V_S equal to -5 V to $-V_{BS}$.

II Nominal voltage for V_{REF} is 5.1 V. I_{OREF} of 0.3 – 0.8 mA dictates total external resistor value on V_{REF} to be 6.3 kΩ to 16.7 kΩ.

III GND input voltage is limited by I_{AAZ} and I_{SSZ} .

IV V_{SS} ramps up from 0 V to 300V.

V Output logic status may not respond correctly if input pulse width is smaller than the minimum pulse width.

5.6 Electrical Characteristics

Valid for temperature range at $T_A = 25^\circ\text{C}$, $V_{CC} = V_B = 15\text{V}$, $C_L = 1\text{nF}$, unless otherwise specified

5.6.1 Low side supply

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
UV_{CC+}	V _{CC} supply UVLO positive threshold	8.40	8.90	9.40	V	
UV_{CC-}	V _{CC} supply UVLO negative threshold	8.20	8.70	9.20		
UV_{CCHYS}	UV _{CC} hysteresis	—	0.2	—		
I_{QCC}	Low side quiescent current	—	—	3	mA	$V_{DT} = V_{CC}$
V_{clampL}	Low side supply clamp voltage	19.6	20.4	21.6	V	$I_{CC} = 5\text{mA}$

5.6.2 High Side Floating Supply

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
UV_{BS+}	High side well UVLO positive threshold	8	8.5	9.0	V	
UV_{BS-}	High side well UVLO negative threshold	7.8	8.3	8.8		
UV_{BSHYS}	UV _{BS} hysteresis	—	0.2	—		
I_{QBS}	High side quiescent current	—	—	1	mA	
I_{LK}	High to Low side leakage current	—	—	50	uA	$V_B = V_S = 300\text{V}$
V_{ClampH}	High side supply clamp voltage	19.6	20.4	21.6	V	$I_{BS} = 5\text{mA}$

5.6.3 Floating Input Supply

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
UV_{AA+}	VA+, VA- floating supply UVLO positive threshold from V _{SS}	8.2	8.7	9.2	V	$V_{SS} = 0$, GND pin floating
UV_{AA-}	VA+, VA- floating supply UVLO negative threshold from V _{SS}	7.7	8.2	8.7		$V_{SS} = 0$, GND pin floating
UV_{AAHYS}	UV _{AA} hysteresis	—	0.5	—		$V_{SS} = 0$, GND pin floating
I_{QAA0}	Floating Input positive quiescent supply current	—	0.5	2	mA	$V_{AA} = 10\text{V}$, $V_{SS} = 0\text{V}$, $V_{CSD} = V_{SS}$
I_{QAA1}	Floating Input positive quiescent supply current	—	8	11		$V_{AA} = 10\text{V}$, $V_{SS} = 0\text{V}$, $V_{CSD} = V_{AA}$
I_{QAA2}	Floating Input positive quiescent supply current	—	8	11		$V_{AA} = 10\text{V}$, $V_{SS} = 0\text{V}$, $V_{CSD} = \text{GND}$
I_{LKM}	Floating input side to Low side leakage current	—	—	50	uA	$V_{AA} = V_{SS} = V_{GND} = 100\text{V}$
V_{CLAMP+}	V _{AA} floating supply clamp voltage, positive, with respect to GND	6.0	7.0	8.0	V	$I_{AA} = 5\text{mA}$, $I_{SS} = 5\text{mA}$, $V_{GND} = 0$, $V_{CSD} = V_{SS}$
V_{CLAMP-}	V _{SS} floating supply clamp voltage, negative, with respect to GND	-8.0	-7.0	-6.0		$I_{AA} = 5\text{mA}$, $I_{SS} = 5\text{mA}$, $V_{GND} = 0$, $V_{CSD} = V_{SS}$

5.6.4 Audio Input

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{OS}	Input offset voltage	-15	0	15	mV	
I_{BIN}	Input bias current	—	—	40	nA	
BW	Small signal bandwidth	—	9	—	MHz	$C_{comp}=2nF$, $R_f=3.3k$
G_m	OTA Output voltage	—	100	—	mS	$V_{IN}=5mV$
G_v	OTA transconductance	60	—	—	dB	
V_{Nrms}	OTA input noise voltage	—	250	—	mVrms	BW=20 kHz, Resolution BW=22Hz
SR	Slew rate	—	± 5	—	V/us	$C_{comp}=1nF$
CMRR	Common-mode rejection ratio	—	60	—	dB	
PSRR	Supply voltage rejection ratio	—	60	—	dB	

5.6.6 Protection

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{ref}	Reference output voltage	4.8	5.1	5.4	V	$I_{OREF}=0.5mA$
V_{thOCL}	Low side OC threshold in V_s	1.1	1.2	1.3		OCSET=1.2V
V_{thOCH}	High side OC threshold in V_{CSH}	$1.1+V_s$	$1.2+V_s$	$1.3+V_s$		
V_{th1}	CSD pin shutdown release threshold	$0.62V_{AA}$	$0.7V_{AA}$	$0.78V_{AA}$		
V_{th2}	CSD pin self reset threshold	$0.26V_{AA}$	$0.30V_{AA}$	$0.34V_{AA}$		
I_{CSD+}	CSD pin discharge current	70	100	130	μA	$V_{CSD}=V_{SS}+5V$
I_{CSD-}	CSD pin charge current	70	100	130		$V_{CSD}=V_{SS}+5V$
t_{sd}	Shutdown propagation delay from $V_{CSD} > V_{SS} + V_{thOCH}$ to Shutdown	—	—	250	ns	
t_{och}	Propagation delay time from $V_{CSH} > V_{thOCH}$ to Shutdown	—	—	500		
t_{ocl}	Propagation delay time from $V_s > V_{thOCL}$ to Shutdown	—	—	500		

5.6.7 Gate Driver

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
I_{O+}	Output high short circuit current (Source)	—	2	—	A	$V_O=0V$, $PW<10\mu s$
I_{O-}	Output low short circuit current (Sink)	—	2	—		$V_O=12V$, $PW<10\mu s$
V_{OL}	Low level out put voltage LO – COM, HO - VS	—	—	0.1	V	$I_O=0$
V_{OH}	High level out put voltage VCC – LO, VB - HO	—	—	1.4		$I_O=0$
t_{on}	High and low side turn-on propagation delay	—	360	—	ns	$V_{DT}=V_{CC}$
t_{off}	High and low side turn-off propagation delay	—	335	—		$V_{DT}=V_{CC}$
t_r	Turn-on rise time	—	20	50		
t_f	Turn-off fall time	—	15	35		
DT1	Deadtime: LO turn-off to HO turn on (DT _{LO-HO}) & HO turn-off to LO turn-on (DT _{HO-LO})	15	25	35		$V_{DT}>V_{DT1}$
DT2		25	40	55		$V_{DT1}>V_{DT}>V_{DT2}$
DT3		50	65	85		$V_{DT2}>V_{DT}>V_{DT3}$
DT4		85	105	135		$V_{DT3}>V_{DT}$
V_{DT1}	DT mode select threshold 2	$0.51V_{CC}$	$0.57V_{CC}$	$0.63V_{CC}$	V	
V_{DT2}	DT mode select threshold 3	$0.32V_{CC}$	$0.36V_{CC}$	$0.40V_{CC}$		
V_{DT3}	DT mode select threshold 4	$0.21V_{CC}$	$0.23V_{CC}$	$0.25V_{CC}$		

6 Waveform definitions

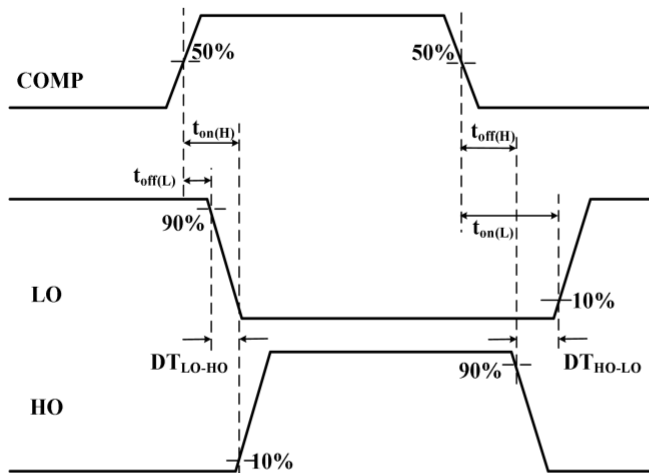


Figure 6-1. Switching Time Waveform Definitions

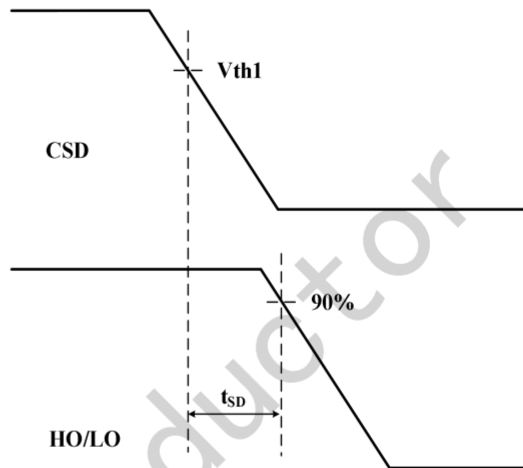


Figure 6-2. CSD to Shutdown Waveform Definitions

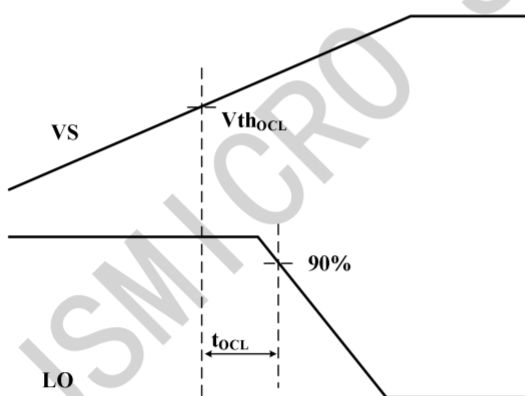


Figure 6-3. $V_S > V_{thOCL}$ to Shutdown Waveform

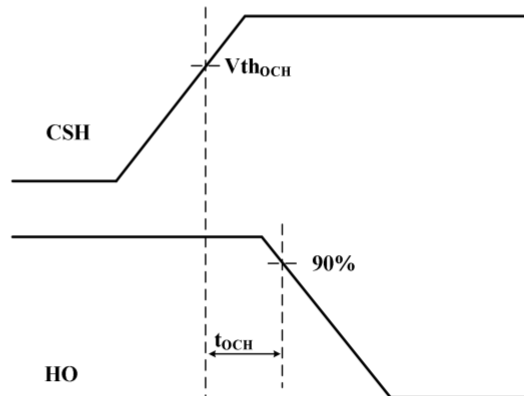


Figure 6-4. $V_{CSH} > V_{thOCH}$ to Shutdown Waveform

7 Input/Output Pin Equivalent Circuit Diagrams

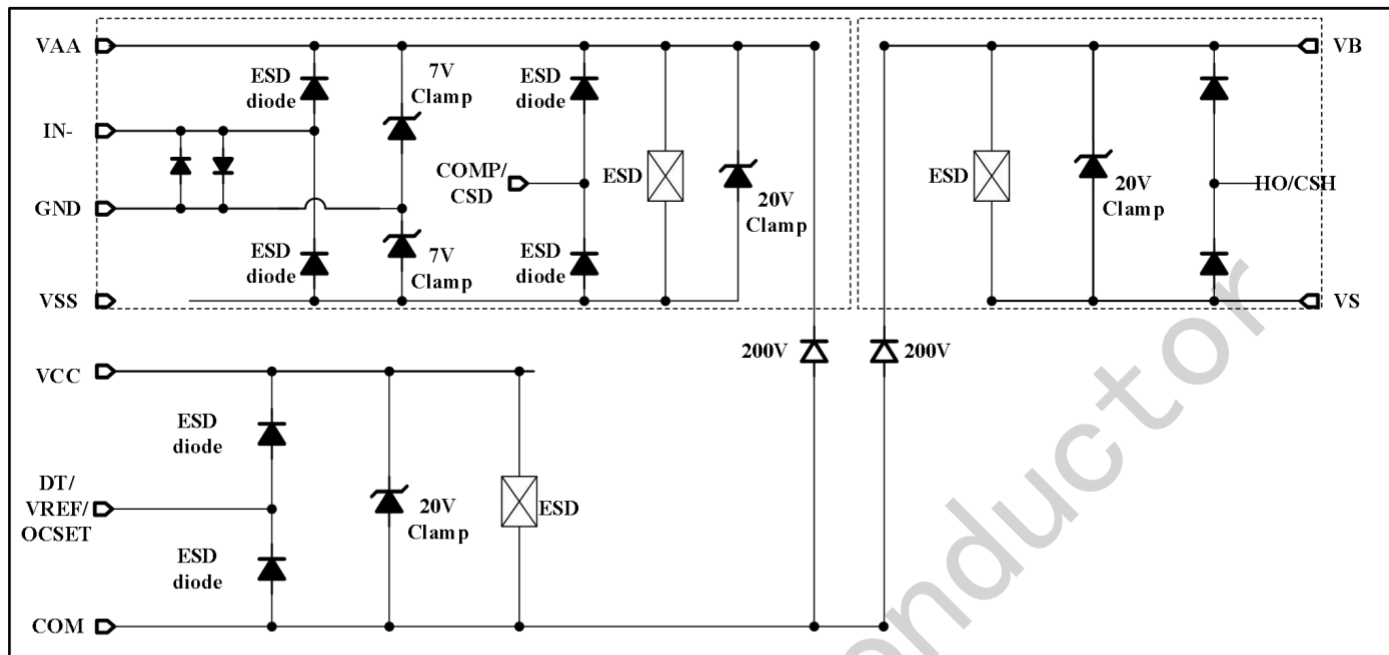


Figure 7-1 Input/Output Pin Equivalent Circuit

8 General Description

8.1 Functional Description

The IRS2092S is a Class D audio amplifier driver with integrated PWM modulator and over current protection. Combined with two external MOSFETs and a few external components, the IRS2092S forms a complete Class D amplifier with dual over current, and shoot-through protection, as well as UVLO protection for the three bias supplies. The versatile structure of the analog input section with an error amplifier and a PWM comparator has the flexibility of implementing different types of PWM modulator schemes.

Loss-less current sensing utilizes $R_{DS(on)}$ of the MOSFETs. The protection control logic monitors the status of the power supplies and load current across each MOSFET.

For the convenience of half bridge configuration, the analog PWM modulator and protection logic are constructed on a floating well.

The IRS2092S implements start-up click noise elimination to suppress unwanted audible noise during PWM start-up and shut-down.

8.2 Functional Block Diagram

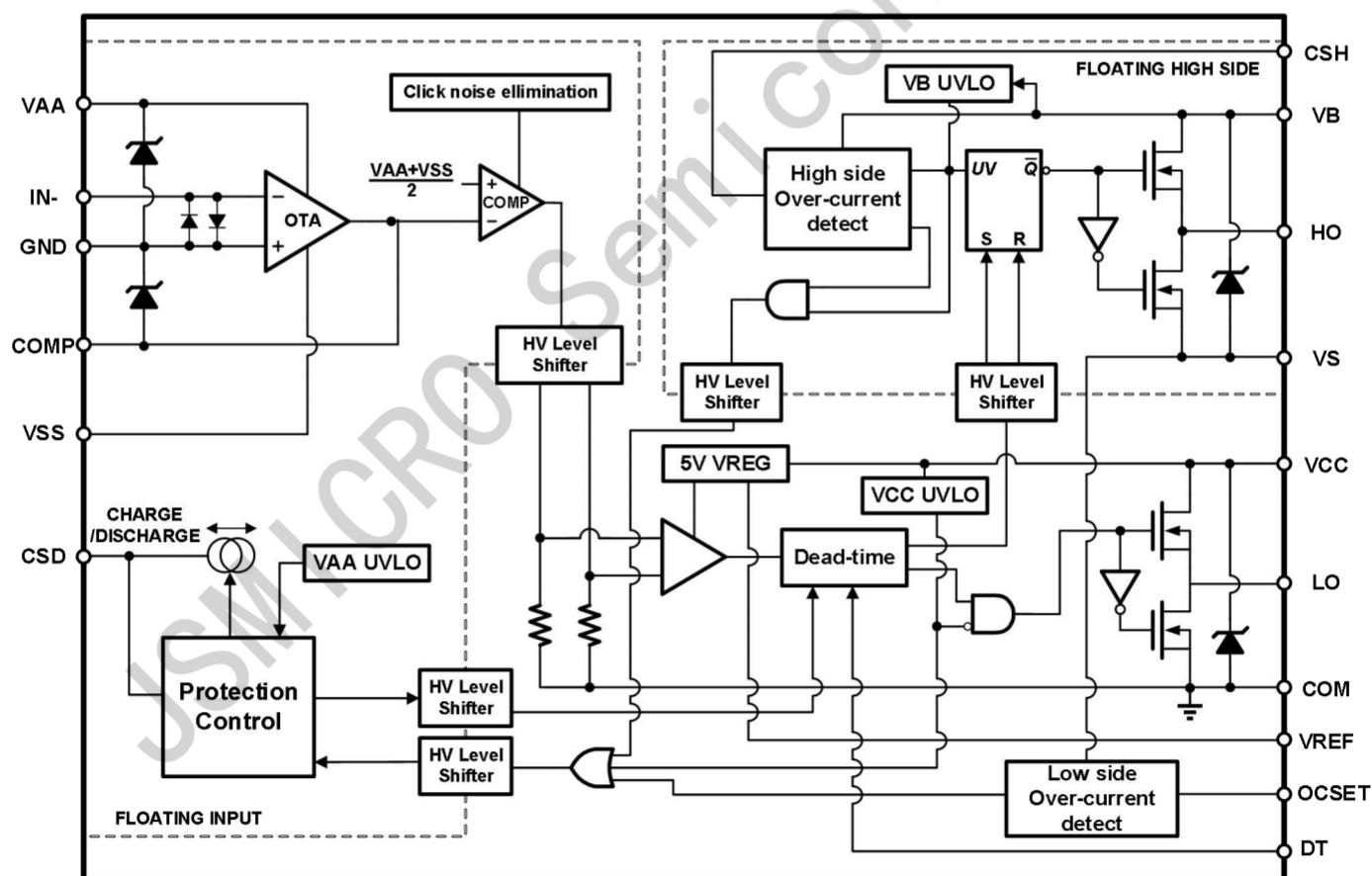


Figure 8-1 Functional Block Diagram

8.3 Typical Connection Diagram

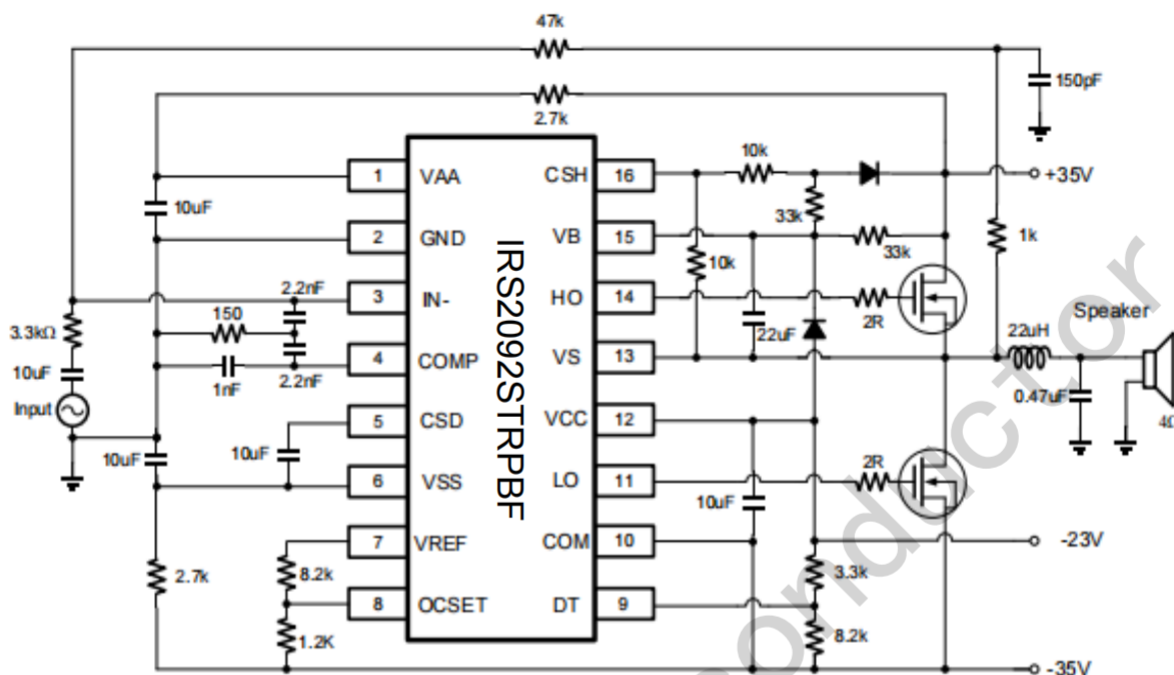


Figure 8-2 Typical Connection Diagram

8.4 Typical Control Loop Design

The audio input stage of IRS2092S is configured as an inverting error amplifier. In Figure 8-3, the voltage gain of the amplifier G_V is determined by input resistor R_{IN} and feedback resistor R_{FB} .

$$G_V = \frac{R_{FB}}{R_{IN}}$$

Since the feedback resistor R_{FB} is part of an integrator time constant, which determines switching frequency, changing overall voltage gain by R_{IN} is simpler and, therefore, recommended in most cases. Note that the input impedance of the amplifier is equal to the input resistor R_{IN} .

A DC blocking capacitor C_{IN} should be connected in series with R_{IN} to minimize DC offset in the output. A ceramic capacitor is not recommended due to potential distortion. Minimizing DC offset is essential for audible noise-less Turn-ON and -OFF.

The connection of the non-inverting input $IN+$ is a reference for the error amplifier, and thus is crucial for audio performance. Connect $IN+$ to the signal reference ground in the system, which has same potential as the negative terminal of the speaker output.

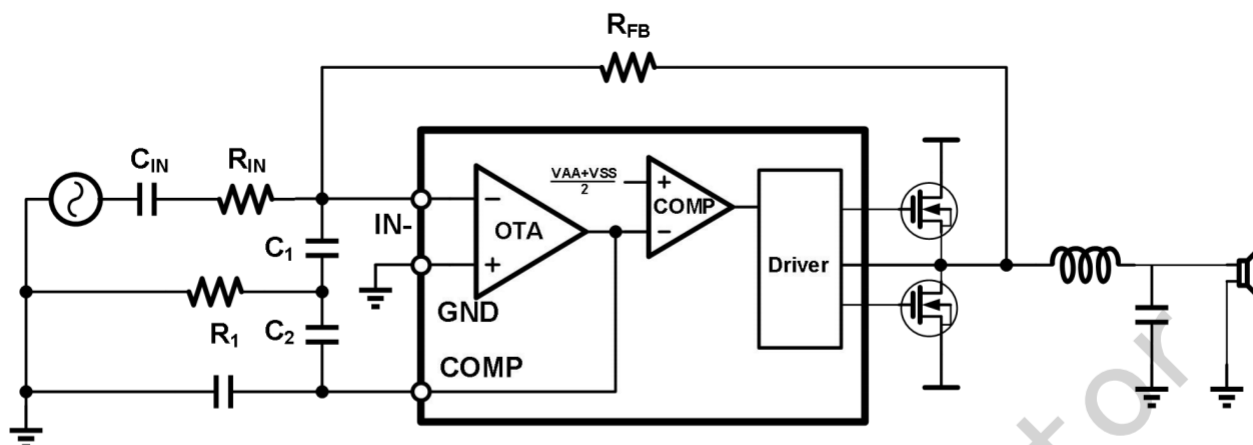


Figure 8-3 Typical Control Loop Design

8.4.1 OTA

The front end error amplifier of the IRS2092S features an operational trans-conductance amplifier (OTA), which is carefully designed to obtain optimal audio performance. The OTA outputs a current output to the COMP pin, unlike a voltage output in an operational amplifier (OPA). The non-inverting input is internally tied to the GND pin.

The inverting input has clamping diodes to GND to improve recovery from clipping as well as ensuring stable start up.

The OTA output COMP is internally connected to the PWM comparator whose threshold is $(V_{AA}+V_{SS})/2$.

For stable operation of the OTA, a compensation capacitor C_c minimum of 1nF is required.

The OTA is shut off when $V_{CSD} < V_{th2}$.

8.4.2 PWM Modulator

In this section, all the explanations are based on a typical application circuit of a self oscillating PWM. For better audio performance, 2nd order integration in the front end is chosen. Self oscillating frequency is determined mainly by the following items in Figure 8-3.

- Integration capacitors, C1 and C2
- Integration resistor, R1
- Propagation delay in the gate driver
- Feedback resistor, R_{FB}
- Duty cycle

Self oscillating frequency has little influences from bus voltage and input resistance R_{IN} . Note that as is the nature of a self-oscillating PWM, the switching frequency decreases as PWM modulation deviates from idling.

Choosing switching frequency entails making a trade off between many aspects.

At lower switching frequency, the efficiency at MOSFET stage improves, but inductor ripple current increases. The output carrier leakage increases.

At higher switching frequency, the efficiency degrades due to switching loss, but wider bandwidth can be achieved. The inductor ripple decreases yet iron loss increases. The junction temperature of gate driver IC might be a stopper for going higher frequency.

For these reasons, 400kHz is chosen for a typical design example, which can be seen in the IRAUDAMP5 reference design.

8.5 Click Noise Elimination

IRS2092S has a unique feature that minimizes Turn-ON and -OFF audible click noise. When CSD is in between V_{th1} and V_{th2} during start up, an internal closed loop around the OTA enables an oscillation that generates voltages at COMP and IN-, bringing them to steady state values. It runs at around 1MHz, independent from the switching oscillation.

As a result, all capacitive components connected to COMP and IN- pins, such as C1, C2, C3 and C_{IN} in Figure8-4, are pre-charged to their steady state values during the star up sequence. This allows instant settling of PWM operation.

To utilize the click noise reduction function, following conditions must be met.

(1) CSD pin has slow enough ramp up from V_{th1} to V_{th2} such that the voltages in the capacitors can settle to their target values.

(2) High side bootstrap power supply needs to be charged up prior to starting oscillation.

(3) Audio input has to be zero.

(4) For internal local loop to override external feedback during the startup period, DC offset at speaker output prior to shutdown release has to satisfy the following condition. $DC_{offset} < 30\mu A * R_{FB}$.

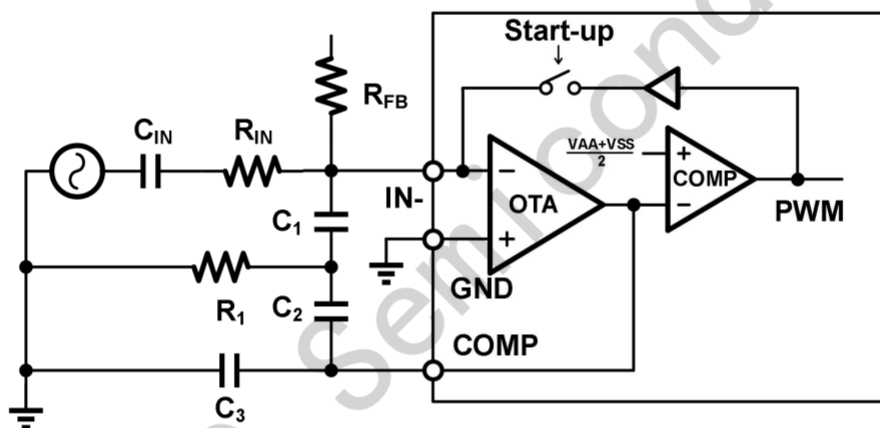


Figure 8-4 Click Noise Elimination

8.6 CSD Voltage and OTA Operational Mode

The CSD pin determines the operational mode of the IRS2092S. The OTA has three operational modes; cut off, local oscillation and normal operation while the gate driver section has two modes;

normal and shutdown with CSD voltage. When $V_{CSD} < V_{th2}$, the IC is in shutdown mode and the OTA is cut off.

When $V_{th2} < V_{CSD} < V_{th1}$, the HO and LO outputs are still in shutdown mode. The OTA is activated and starts local oscillation, which pre-biases all the capacitive components in the error amplifier.

When $V_{CSD} > V_{th1}$, shutdown is released and PWM operation starts.

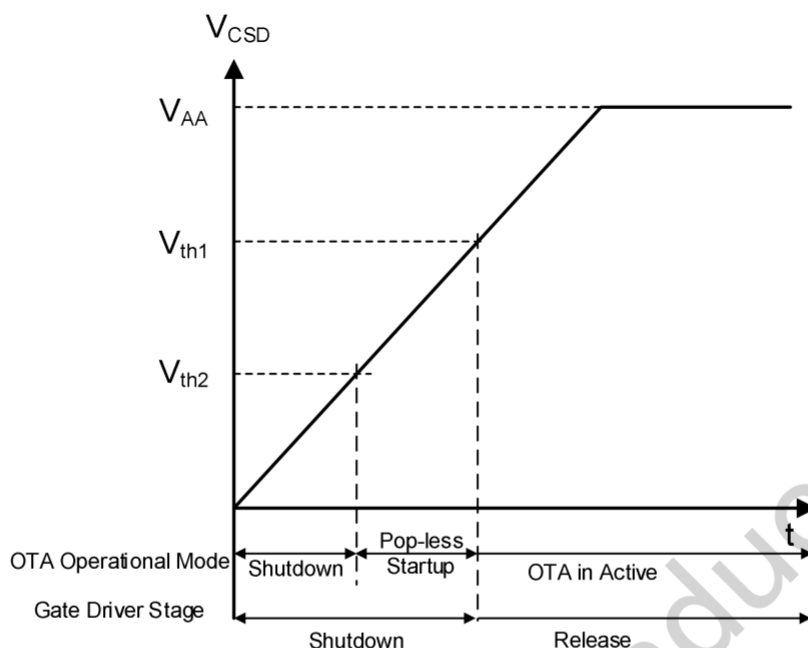


Figure 8-5 V_{CSD} and OTA Mode

8.7 Over Current Protection

The IRS2092S features over current protection to protect the power MOSFETs during abnormal load conditions. The IRS2092S starts a sequence of events when it detects an over current condition during either high side or low side turn on of a pulse.

As soon as either the high side or low side current sensing block detects over current:

- (1) The OC Latch (OCL) flips logic states and shutdowns the outputs LO and HO.
- (2) The CSD pin starts discharging the external capacitor C_t .
- (3) When V_{CSD} , the voltage across C_t , falls below the lower threshold V_{th2} , an output signal from COMP2 resets OCL.
- (4) When V_{CSD} goes above the upper threshold V_{th1} , the logic on COMP1 flips and the IC resumes operation.

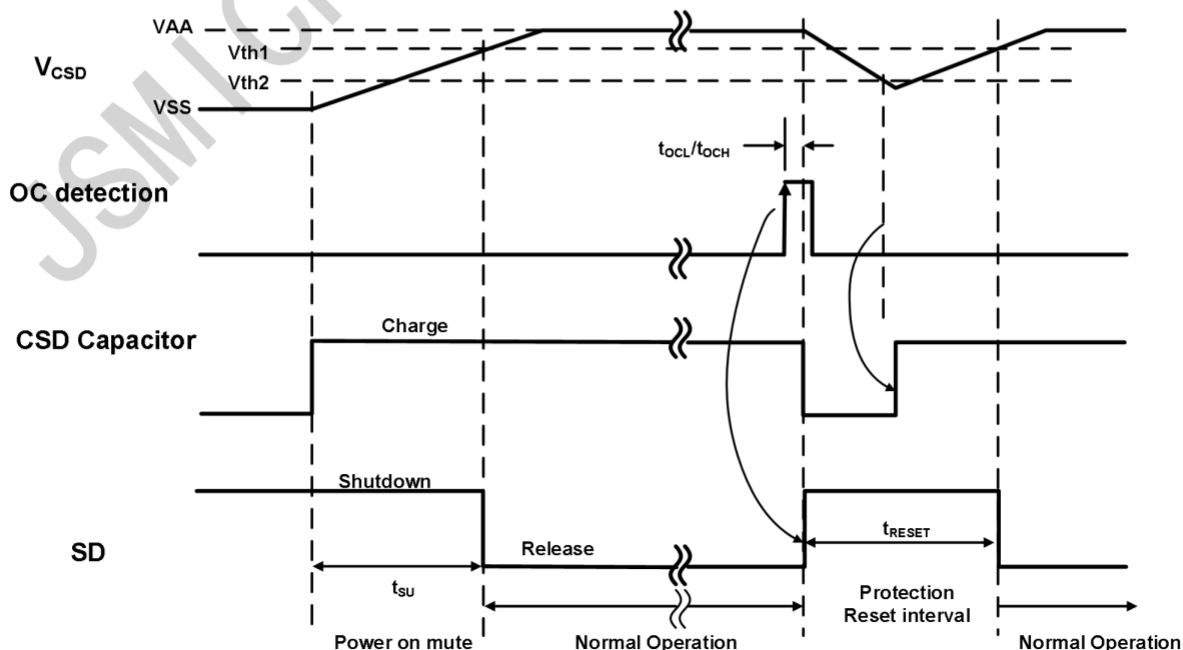


Figure 8-6 Shutdown Functional Block Diagram

8.8 Programming Dead-Time

The IRS2092S selects the dead-time from a range of preset dead-time values based on the voltage applied at the DT pin.

When $V_{DT} < 0.23V_{CC}$, $DT = 105ns$;

When $0.23V_{CC} < V_{DT} < 0.36V_{CC}$, $DT = 75ns$;

When $0.36V_{CC} < V_{DT} < 0.57V_{CC}$, $DT = 45ns$;

When $0.57V_{CC} < V_{DT} < V_{CC}$, $DT = 25ns$.

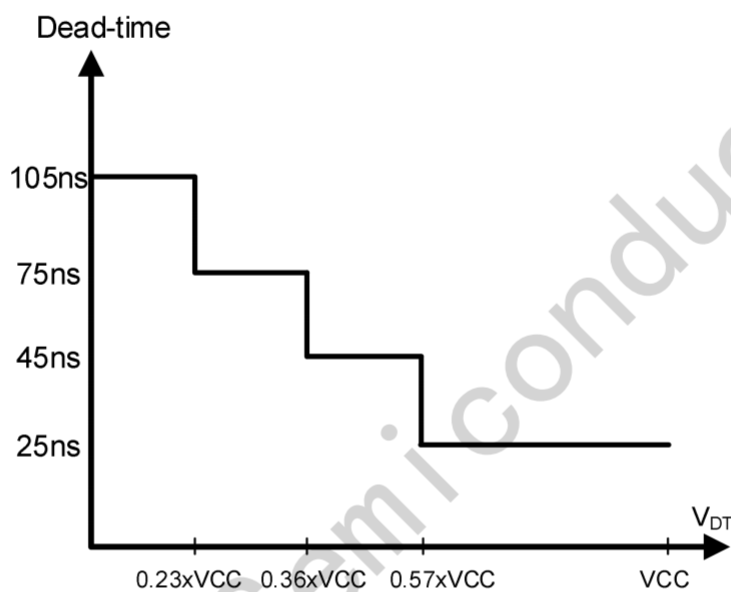
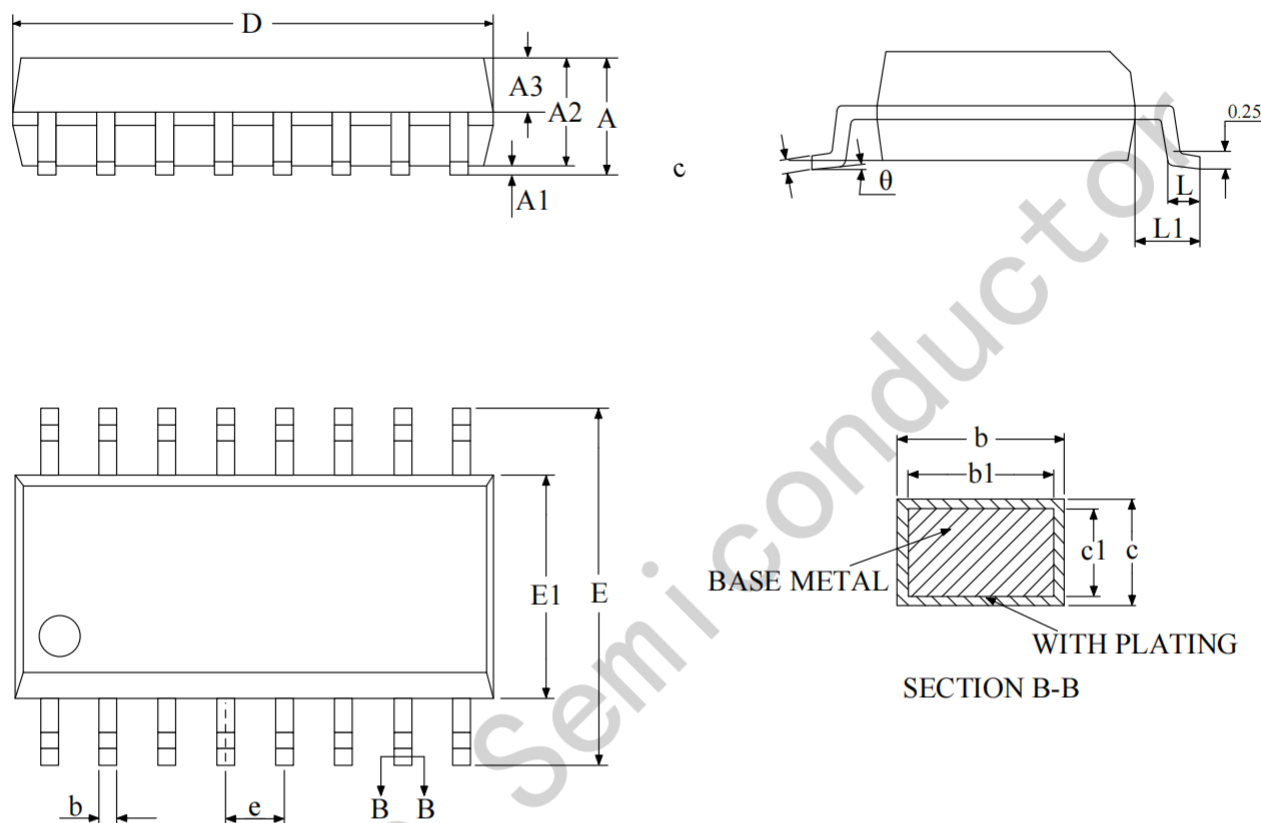


Figure 8-6 Dead Time vs. V_{DT}

9 Package Information

SOIC16 Package Outlines



SOIC16 Package Dimensions

Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	9.70	9.90	10.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	L	0.25	-	0.50
b1	0.38	0.41	0.43	L1	1.4BSC		
c	0.21	-	0.26	θ	0	-	8°
c1	0.19	0.20	0.21				