HX1700-3302-ST Low Quiescent Current LDO

General Description

The HX1700-3302-ST CMOS LDO regulators deliver up to 250 mA with just 1.6 μA quiescent current. Operating from 2.3V to 6.0V, they're ideal for 2/3-cell battery or Li-Ion apps. With a 178 mV dropout at 250 mA, they offer ±0.4% tolerance at +25°C and ±3% over -40°C to +125°C. Output ranges from 1.2V to 5.0V, stable with 1 μF cap. Features overcurrent limit and overtemp shutdown for robust performance.

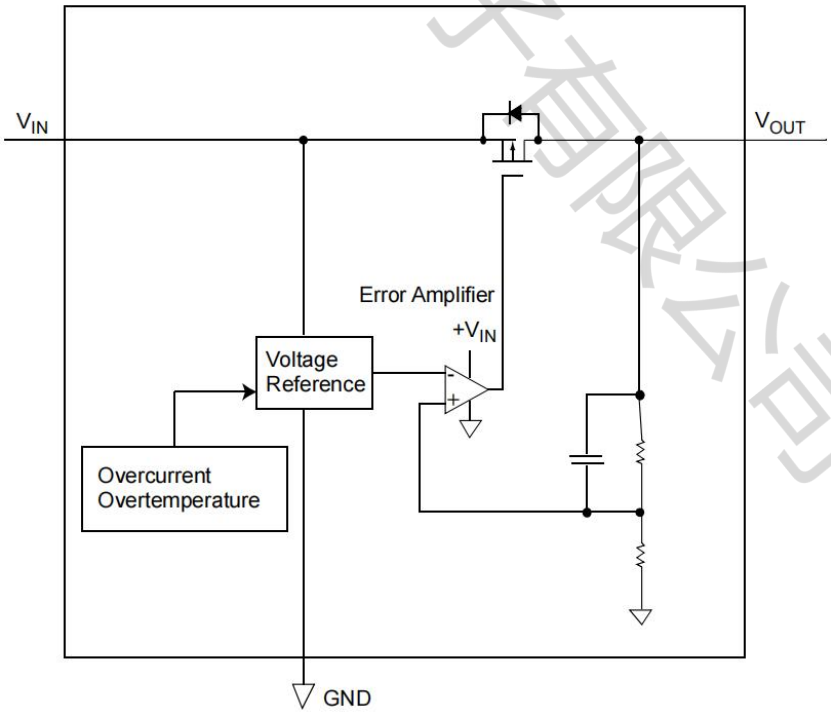
Features

- 1.6 μATypical Quiescent Current
- Input Operating Voltage Range: 2.3V to 6.0V
- Output Voltage Range: 1.2V to 5.0V
- 250 mA Output Current for Output Voltages ≥ 2.5V
- 200 mA Output Current for Output Voltages < 2.5V
- Low Dropout (LDO) Voltage
  - 178 mV Typical @ 250 mA for V OUT = 2.8V
- 0.4% Typical Output Voltage Tolerance
- Standard Output Voltage Options:
  - 1.2V, 1.8V, 2.5V, 2.8V, 2.9V, 3.0V, 3.3V, 5.0V
- Stable with 1.0 μF Ceramic Output Capacitor
- Short Circuit Protection
- Overtemperature Protection

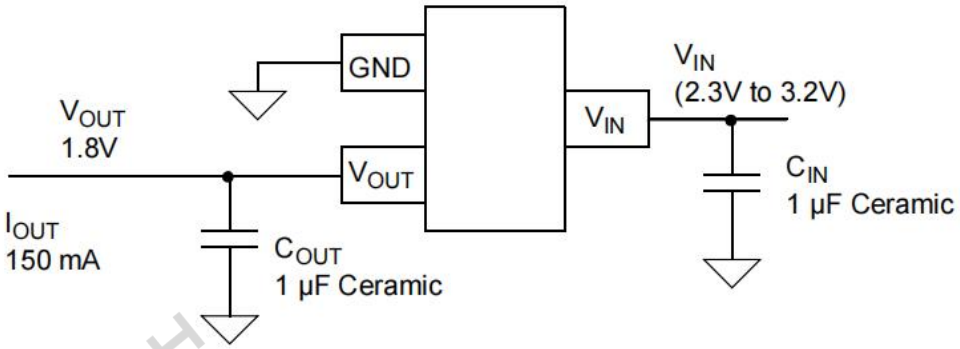
Applications

- Battery-Powered Devices
- Battery-Powered Alarm Circuits
- Smoke Detectors
- CO2 Detectors
- Pagers and Cellular Phones
- Smart Battery Packs
- Low Quiescent Current Voltage Reference
- PDAs
- Digital Cameras
- Microcontroller Power

Functional Block Diagrams



Typical Application Circuits



Absolute Maximum Ratings †

V DD.....+6.5V

All inputs and outputs w.r.t. ..... (VSS - 0.3V) to (VIN+ 0.3V)

Peak Output Current ..... Internally Limited

Storage Temperature -65°C to +150°C

Maximum Junction Temperature 150°C

Operating Junction Temperature -40°C to +125°C

ESD protection on all pins (HBM;MM) ≥ 4 kV; ≥ 400V

DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified, all limits are established for V_{IN} = V_R + 1V, I_{LOAD} = 100 µA, C_{OUT} = 1 µF (X7R), C_{IN} = 1 µF (X7R), T_A = +25°C.
Boldface type applies for junction temperatures, T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input/Output Characteristics						
Input Operating Voltage	V_{IN}	**2.3**	—	**6.0**	V	
Input Quiescent Current	I_q	—	1.6	**4**	µA	I_L = 0 mA, V_{IN} = V_R + 1V
Maximum Output Current	I_{OUT_mA}	**250** **200**	— —	— —	mA	For V_R ≥ 2.5V For V_R < 2.5V
Output Short Circuit Current	I_{OUT_SC}	—	408	—	mA	V_{IN} = V_R+ 1V, V_{OUT} = GND Current (peak current) measured 10 ms after short is applied.
Output Voltage Regulation	V_{OUT}	V_R - 2.0% **V_R - 3.0%**	V_R± 0.4%	V_R + 2.0% **V_R+ 3.0%**	V	
V_{OUT} Temperature Coefficient	TCV_{OUT}	—	50	—	ppm/°C	
Line Regulation	$\Delta V_{OUT}/(V_{OUT}X\Delta V_{IN})$	**-1.0**	±0.75	**+1.0**	%/V	(V_R + 1)V ≤ V_{IN} ≤ 6V

Load Regulation	$\Delta V_{OUT}/V_{OUT}$	**-1.5**	±1.0	**+1.5**	%	I_L= 0.1 mAto 250 mA for $V_R \geq$ 2.5V I_L= 0.1 mAto 200 mA for V_R < 2.5V
Dropout Voltage V_R > 2.5V	V_{IN} - V_{OUT}	—	178	**350**	mV	I_L = 250 mA,
Dropout Voltage V_R < 2.5V	V_{IN} - V_{OUT}	—	150	**350**	mV	I_L = 200 mA,
Output Rise Time	T_R	—	500	—	µs	10% V_R to 90% V_R V_{IN} = 0V to 6V, R_L = 50Ω resistive
Output Noise	eN	—	3	—	µV/(Hz)1/2	I_L = 100 mA, f = 1 kHz, C_{OUT} = 1 µF
Power Supply Ripple Rejection Ratio	PSRR	—	44	—	dB	f = 100 Hz, C_{OUT} = 1 µF, I_L = 50 mA, V_{INAC} = 100 mV pk-pk, C_{IN} = 0 µF, V_R = 1.2V
Thermal Shutdown Protection	T_{SD}	—	140	—	°C	V_{IN} = V_R + 1V, I_L = 100 µA

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, all limits are established for V_{IN} = V_R + 1V, I_{LOAD} = 100 µA, C_{OUT} = 1 µF (X7R), C_{IN} = 1 µF (X7R), T_A = +25°C.
Boldface type applies for junction temperatures, T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40		+125	°C	
Operating Temperature Range	T_J	-40		+125	°C	
Storage Temperature Range	T_A	-65		+150	°C	
Thermal Package Resistance						
Thermal Resistance, 2x2 DFN	θ_{JA}	—	91	—	°C/W	EIA/JEDEC® JESD51-7 FR-4 4-Layer Board
	$\theta_{JC(Top)}$	—	286	—	°C/W	
	$\theta_{JC(Bottom)}$	—	28.57	—	°C/W	
	Ψ_{JT}	—	8.95	—	°C/W	
Thermal Resistance, SOT-23	θ_{JA}	—	212	—	°C/W	EIA/JEDEC JESD51-7 FR-4 4-Layer Board
	$\theta_{JC(Top)}$	—	139	—	°C/W	
	$\theta_{JC(Bottom)}$	—	11.95	—	°C/W	
	Ψ_{JT}	—	6.15	—	°C/W	
Thermal Resistance, SOT-89	θ_{JA}	—	104	—	°C/W	EIA/JEDEC JESD51-7 FR-4 4-Layer Board
	$\theta_{JC(Top)}$	—	74	—	°C/W	
	Ψ_{JT}	—	30	—	°C/W	
Thermal Resistance, TO-92	θ_{JA}	—	92	—	°C/W	EIA/JEDEC JESD51-7 FR-4 4-Layer Board
	$\theta_{JC(Top)}$	—	74	—	°C/W	

TYPICAL PERFORMANCE CURVES

Unless otherwise indicated: VR = 1.8V, COUT = 1 µF Ceramic (X7R), CIN = 1 µF Ceramic (X7R), IL = 100 µA, TA = +25°C, VIN = VR + 1V.

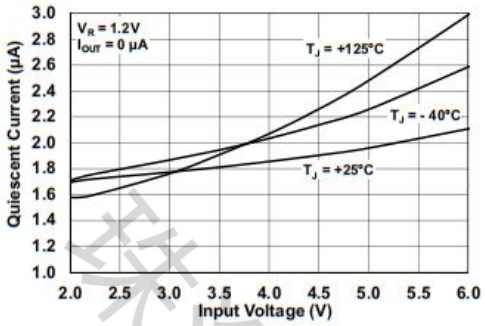


FIGURE 1: *Input Quiescent Current vs. Input Voltage.*

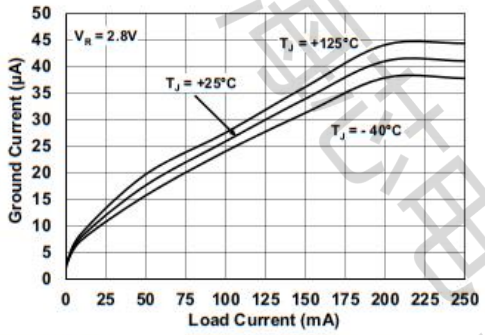


FIGURE 2: *Ground Current vs. Load Current.*

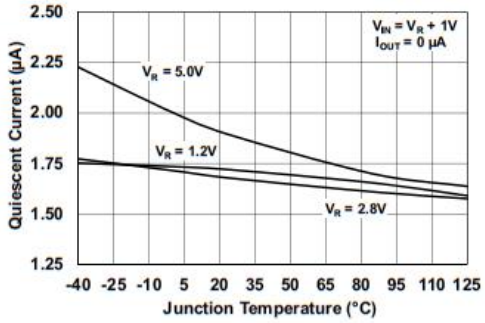


FIGURE 3: *Quiescent Current vs. Junction Temperature.*

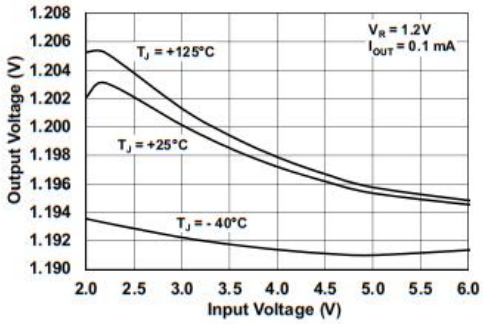


FIGURE 4: *Output Voltage vs. Input Voltage (V_R = 1.2V).*

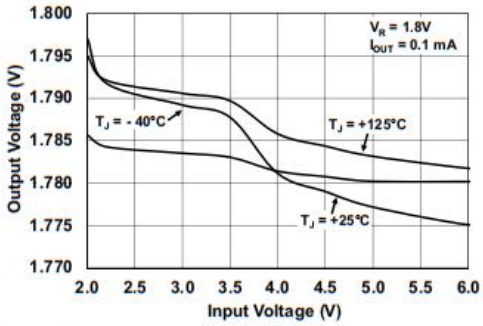


FIGURE 5: *Output Voltage vs. Input Voltage (V_R = 1.8V).*

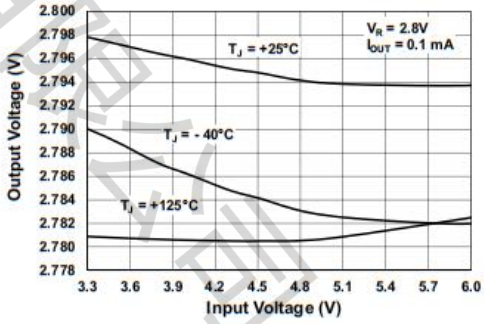


FIGURE 6: *Output Voltage vs. Input Voltage (V_R = 2.8V).*

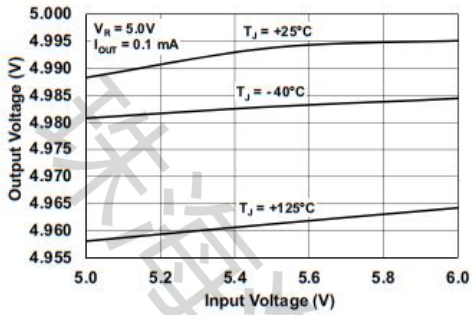


FIGURE 7: *Output Voltage vs. Input Voltage (V_R = 5.0V).*

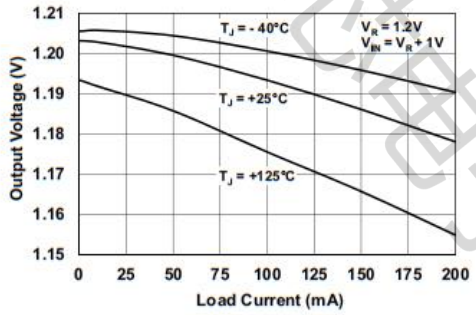


FIGURE 8: *Output Voltage vs. Load Current (V_R = 1.2V).*

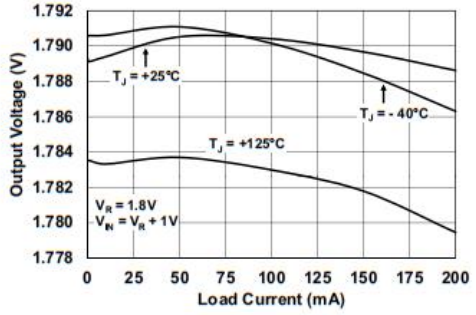


FIGURE 9: *Output Voltage vs. Load Current (V_R = 1.8V).*

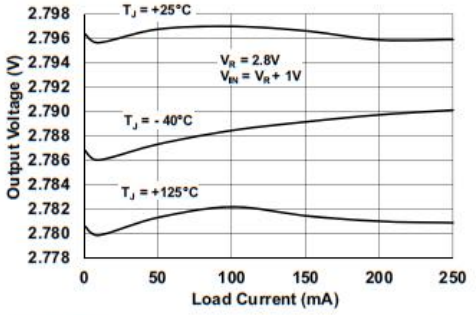


FIGURE 10: *Output Voltage vs. Load Current (V_R = 2.8V).*

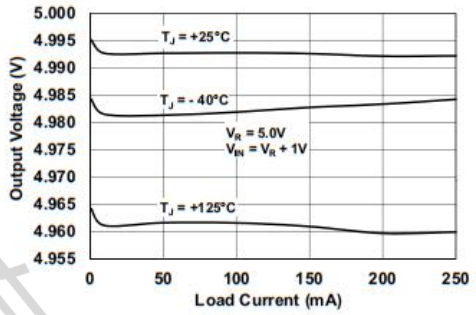


FIGURE 11: *Output Voltage vs. Load Current (V_R = 5.0V).*

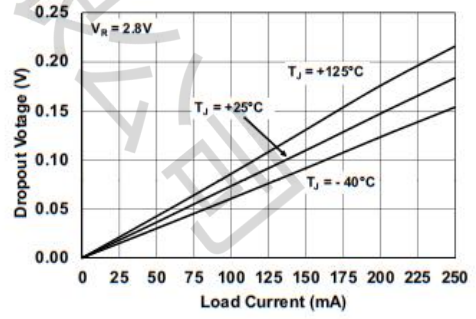


FIGURE 12: *Dropout Voltage vs. Load Current (V_R = 2.8V).*

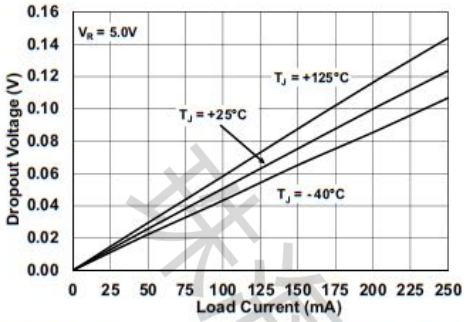


FIGURE 13: *Dropout Voltage vs. Load Current (V_R = 5.0V).*

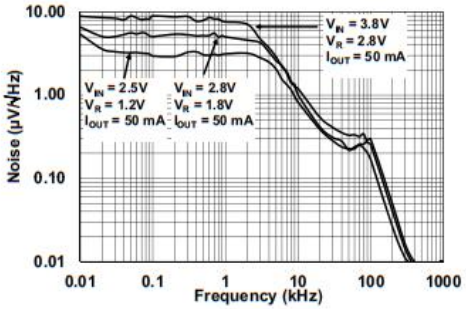


FIGURE 16: *Noise vs. Frequency.*

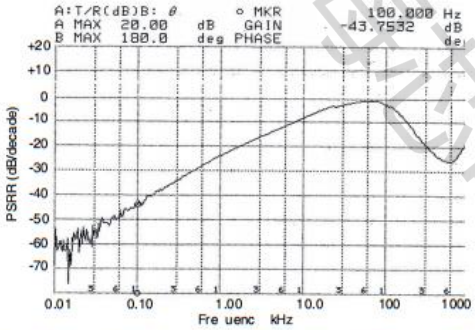


FIGURE 14: *Power Supply Ripple Rejection vs. Frequency (V_R = 1.2V).*

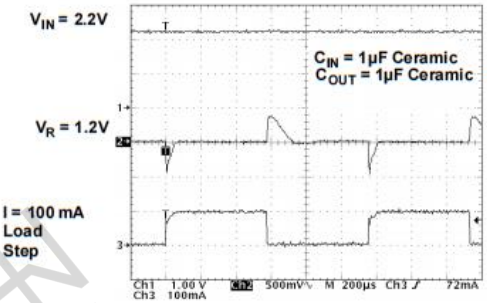


FIGURE 17: *Dynamic Load Step (V_R = 1.2V).*

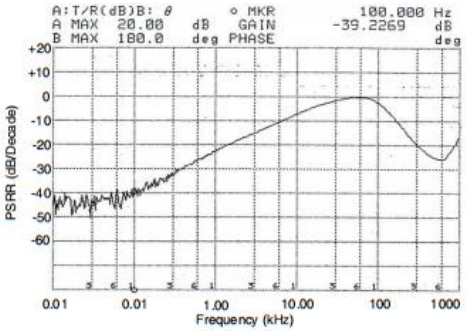


FIGURE 15: *Power Supply Ripple Rejection vs. Frequency (V_R = 2.8V).*

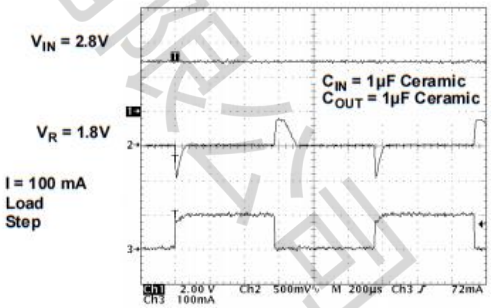


FIGURE 18: *Dynamic Load Step (V_R = 1.8V).*

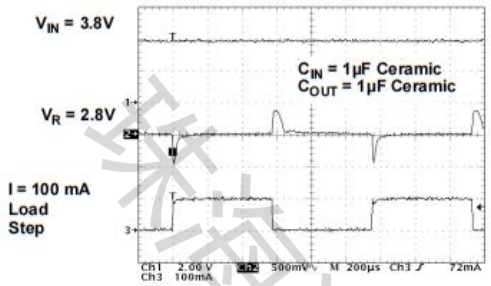


FIGURE 19: *Dynamic Load Step (V_R = 2.8V).*

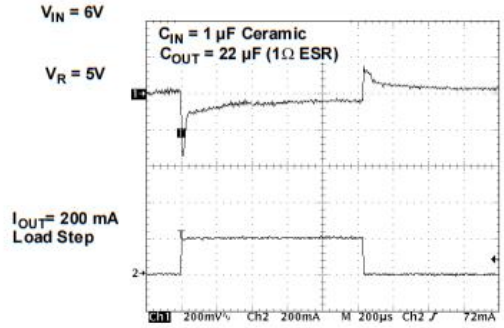


FIGURE 22: *Dynamic Load Step (V_R = 5.0V).*

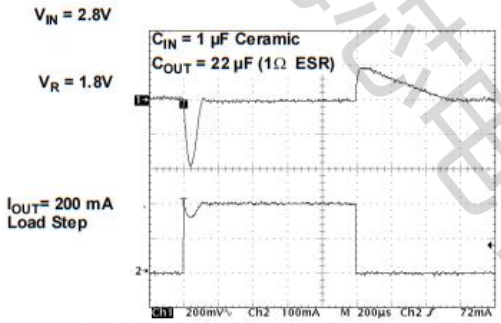


FIGURE 20: *Dynamic Load Step (V_R = 1.8V).*

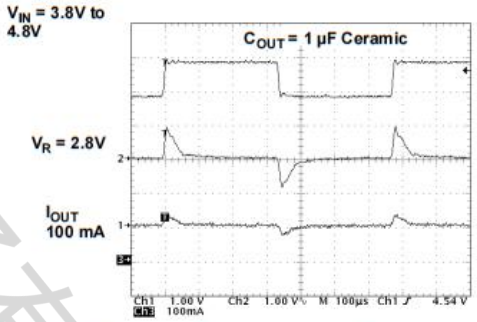


FIGURE 23: *Dynamic Line Step (V_R = 2.8V).*

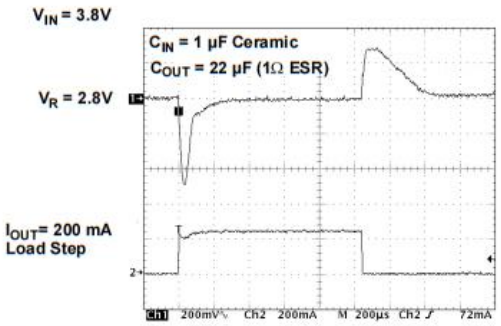


FIGURE 21: *Dynamic Load Step (V_R = 2.8V).*

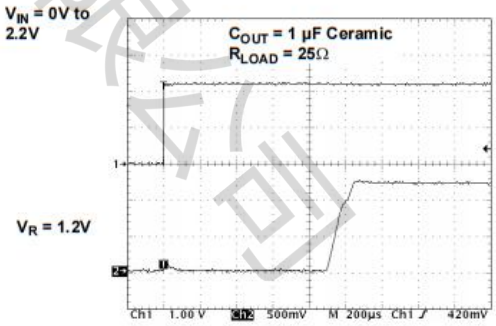


FIGURE 24: *Start-up from V_{IN} (V_R = 1.2V).*

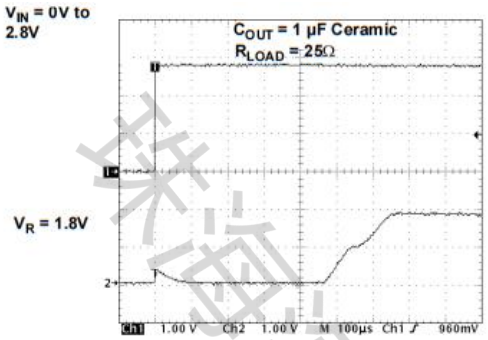


FIGURE 25: *Start-up from V_{IN} (V_R = 1.8V).*

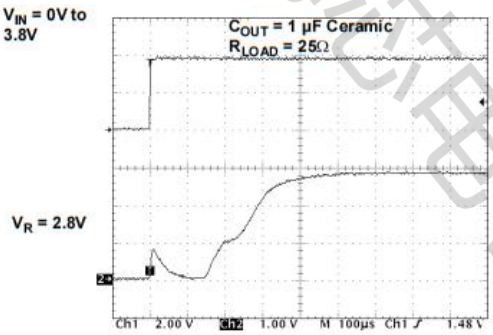


FIGURE 26: *Start-up from V_{IN} (V_R = 2.8V).*

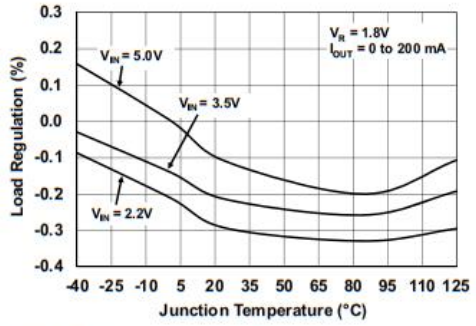


FIGURE 27: *Load Regulation vs. Junction Temperature (V_R = 1.8V).*

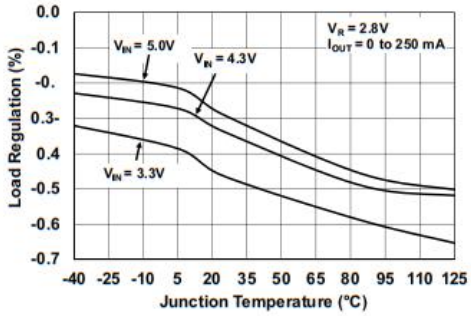


FIGURE 28: *Load Regulation vs. Junction Temperature (V_R = 2.8V).*

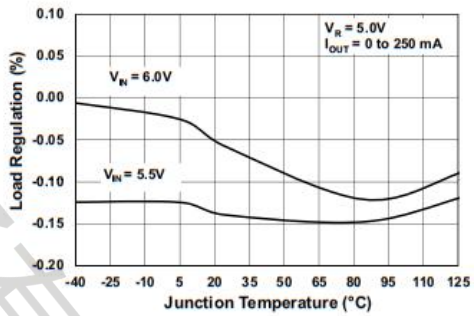


FIGURE 29: *Load Regulation vs. Junction Temperature (V_R = 5.0V).*

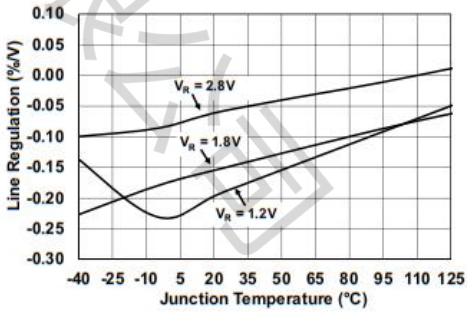


FIGURE 30: *Line Regulation vs. Temperature (V_R = 1.2V, 1.8V, 2.8V).*

PIN DESCRIPTIONS

PIN FUNCTION TABLE

Pin No. SOT-23	Name	Function
1	GND	Ground Terminal
2	VOUT	Regulated Voltage Output
3	VIN	Unregulated Supply Voltage

Ground Terminal (GND)

Connect the GND pin to the negative terminals of both the output and input capacitors, serving as the regulator's ground reference. This pin primarily conducts the LDO's bias current (typically 1.6 μA), without significant high current flow. The LDO output regulation is referenced to this pin; hence, minimize voltage drops between it and the load's negative side.

Regulated Output Voltage (VOUT)

Attach the VOUT pin to the positive side of the load and the positive terminal of the output capacitor. Position the output capacitor's positive side as close as feasible to the LDO's VOUT pin for optimal performance. The DC load current flows out of this pin.

Unregulated Input Voltage Pin (VIN)

Connect VIN to the unregulated input source voltage. For stable LDO operation, a low source impedance is crucial, influenced by the proximity of input capacitors or battery type. Generally, 1 μF of capacitance ensures stability, though for loads under 100 mA, this requirement can be reduced. Suitable capacitors include ceramic, tantalum, or aluminum electrolytic types, with ceramic capacitors offering better noise and PSRR performance at high frequencies due to their low ESR characteristics.

No Connect (NC)

Pins labeled NC have no internal connection and should remain unconnected in the circuit.

Exposed Thermal Pad (EP)

The Exposed Thermal Pad (EP) is electrically connected to the GND pin internally. On the Printed Circuit Board (PCB), ensure both are tied to the same potential for proper thermal and electrical management.

DETAILED DESCRIPTION

Output Regulation:

The LDO compares feedback output voltage with an internal reference, adjusting P-Channel transistor current to maintain the desired output voltage.

Overcurrent Protection:

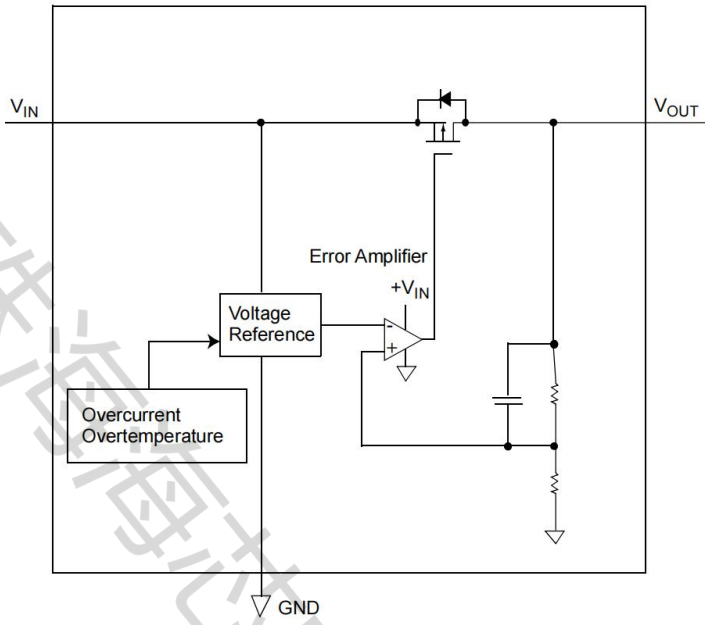
HX1700-3302-ST monitors current, temporarily disables transistor in case of overcurrent, and retries to avoid damage.

Overtemperature Safeguard:

Excessive power dissipation raises internal temperature, triggering shutdown until safe operating temperatures are reached. Repeated if needed to prevent failure.

FUNCTIONAL SUMMARY

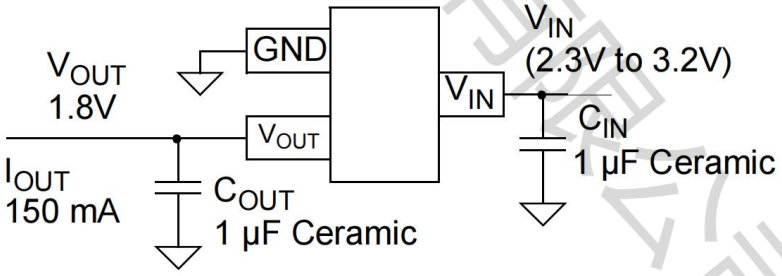
The HX1700-3302-ST LDO supports 0-250mA load with VR ⩾ 2.5V, operating from 2.3V-6.0V inputs. Requires low input impedance for stability. 1μF+ output cap for stability up to 250mA. Controlled 500μs output rise time during startup.



APPLICATION CIRCUITS AND ISSUES

Typical Application

The HX1700-3302-ST is most commonly used as a voltage regulator. Its low quiescent current and low dropout voltage make it ideal for many battery-powered applications.



APPLICATION INPUT REQUIREMENTS

POWER ASSESSMENT

POWER DISSIPATION CALCULATION

The HX1700-3302-ST's internal power dissipation depends on input voltage (VIN), output voltage (VOUT), and output current (IOUT). The quiescent current's contribution to dissipation is negligible (1.6 μA x VIN). Calculate internal power dissipation using:

Equation 6-1:

PLDO =(VIN(MAX) −VOUT(MIN))×IOUT(MAX)

where:

PLDO = Internal power dissipation of the LDO pass device

VIN(MAX) = Maximum input voltage

VOUT(MIN) = Minimum output voltage of the LDO

IOUT(MAX) = Maximum output current

6.2.2 ESTIMATING INTERNAL JUNCTION TEMPERATURE

The maximum continuous junction temperature for the HX1700-3302-ST is +125° C. To estimate the internal junction temperature, multiply the total power dissipation by the thermal resistance from junction to ambient (R θ JA):

Equation 6-2:

TJ(MAX) =PTOTAL ×R θ JA +TA(MAX)

where:

TJ(MAX) = Maximum continuous junction temperature

PTOTAL = Total power dissipation of the device

R θ JA = Thermal resistance from junction to ambient (SOT-23: ~230° C/W)

TA(MAX) = Maximum ambient temperature

6.2.3 MAXIMUM POWER DISSIPATION LIMIT

Determine the maximum power dissipation capability of the package based on the junction-to-ambient thermal resistance and maximum ambient temperature:

Equation 6-3 & 6-4 Combined:

PD(MAX) =R T −T

where:

PD(MAX) = Maximum power dissipation of the device

Other variables as defined above

Example Calculation:

Given:

Package Type: SOT-23

Input Voltage Range: 2.3V to 3.2V

VIN(MAX) = 3.2V

VOUT(TYP) = 1.8V (assuming minimum close to this)

IOUT(MAX) = 150 mA

Calculate PLDO :

PLDO =(3.2V−1.8V)×150mA=210mW

Assuming TA(MAX) = 25° C and R θ JA = 230° C/W for SOT-23, calculate TJ(MAX) :

TJ(MAX) =210mW×230° C/W+25° C=73.3° C+25° C=98.3° C (well within limits)

For maximum power dissipation capability, use:

PD(MAX) =230° C/W125° C−25° C ≈0.435W

Section 6.3: Voltage Regulator Power Calculations and Thermal Considerations

Internal power dissipation, junction temperature rise, junction temperature, and maximum power dissipation are analyzed in the following example. Ground current's contribution to power dissipation is insignificant and is therefore neglected.

Power Dissipation Calculation Example

Device Junction Temperature Analysis

The internal junction temperature rise is determined by the internal power dissipation and the thermal resistance from junction to ambient (R θ JA) specific to the application. R θ JA values are derived from industry standards like

EIA/JEDEC JESD51-7, which outlines test methods and board specifications for measuring thermal resistance in small surface-mount packages. Note that actual R θ JA can vary based on factors like copper area and thickness in a given design. For more detailed analysis, refer to AN792, "A Method to Determine How Much Power a SOT-23 Can Dissipate in an Application" (DS00792).

Estimating Junction Temperature

To assess the internal junction temperature, add the calculated temperature rise to the ambient or offset temperature. Below, we estimate the worst-case junction temperature for a given scenario.

Maximum Package Power Dissipation at +40° C Ambient

Package Type: SOT-23 (for primary example), with other package types considered for comparison

Input Voltage: VIN = 2.3V to 3.2V

LDO Output: VOUT = 1.8V, IOUT = 150 mA

Maximum Ambient Temperature: TA(MAX) = +40° C

Internal Power Dissipation Calculation

Internal power dissipation is the product of the LDO output current and the voltage drop across the LDO (VIN to VOUT). Assuming a typical dropout voltage, we calculate:

PLDO(MAX) =(VIN(MAX) −(0.97×VOUT))×IOUT(MAX)

PLDO =(3.2V−(0.97×1.8V))×150mA=218.1mW

Junction Temperature Rise and Total Junction Temperature

TJ(RISE) =PTOTAL ×R θ JA

TJ(RISE) =218.1mW×212° C/W=46.2° C

TJ =TJ(RISE) +TA(MAX)

TJ =46.2° C+40° C=86.2° C

Maximum Power Dissipation for Different Packages

The maximum power dissipation capability of various packages can be estimated as follows, using their respective R θ JA values and assuming a maximum junction temperature of 125° C:

2x2 DFN-6: R θ JA =91° C/W

PD(MAX) =91° C/W125° C−40° C ≈934mW

SOT-23: R θ JA =212° C/W

PD(MAX) =212° C/W125° C−40° C ≈401mW

PD(MAX) =92° C/W125° C−40° C ≈924mW

These calculations demonstrate the importance of considering thermal management when selecting a package for a given application's power requirements.

Voltage Reference Capability

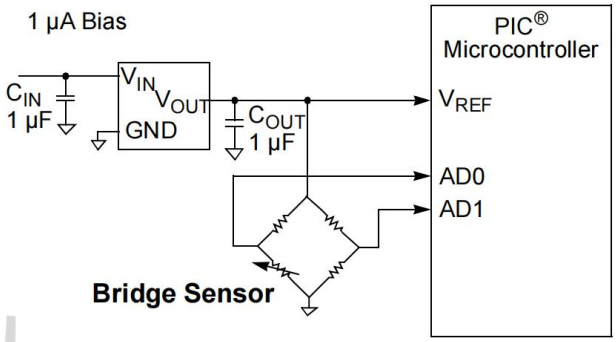
The HX1700-3302-ST boasts versatility, functioning not merely as a regulator but also as a voltage reference with minimal quiescent current. In numerous microcontroller applications, the initial precision of this reference can be fine-tuned through production testing equipment or by employing ratio-based measurements. Once calibrated for initial accuracy, the primary sources of error introduced by the HX1700-3302-ST LDO are limited to its thermal stability and line regulation tolerance. Additionally, its cost-effectiveness, low quiescent current consumption, and compact ceramic output capacitor make it an attractive choice for voltage reference applications.

Handling Pulsed Load Demands

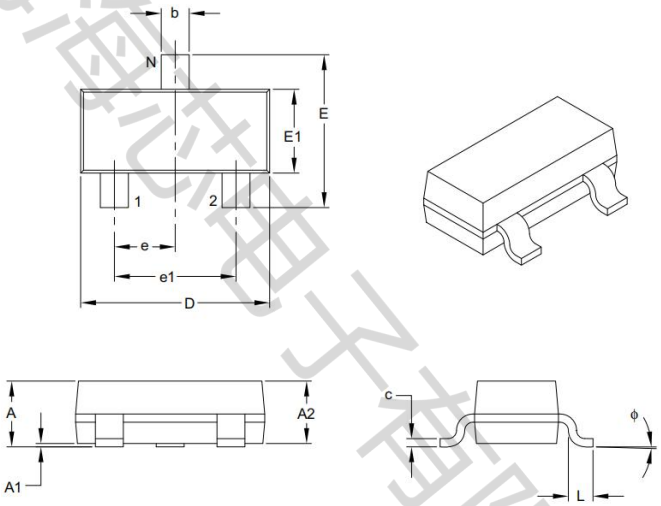
In certain applications, pulsed load currents may surge beyond the HX1700-3302-ST's specified maximum of 250 mA. However, the device's internal current limiting mechanism safeguards against irreparable damage caused by such

transient high peak loads. It's important to note that the 250 mA rating refers to the maximum average continuous current. Provided the average current remains within this limit, the HX1700-3302-ST can accommodate pulsed loads exceeding this threshold. At a typical ambient temperature of +25° C, the HX1700-3302-ST's current limit is set at 550 mA, allowing for flexibility in handling intermittent high load demands.

Ratio Metric Reference



PACKAGING INFORMATION



units		MILLIMETERS		
Dimension Limits		MIN	NoM	MAX
Number of Leads	N		3	
pitch	e		1.50 BSC	
outside Lead pitch	e1		3.00 BSC	
overall Height	A	1.40	1.50	1.60
overall width	H	3.94	4.10	4.25
Molded package width at Base	E		2.50 BSC	
Molded package width at Top	E1	2.13	2.20	2.29
overall Length	D		4.50 BSC	
Tab Length (option A)	D1A	1.63	1.73	1.83
Tab Length (option B)	D1B	1.40	1.60	1.75
Tab Length (option C)	D1C	1.62	1.73	1.83
Foot Length	L	0.79	1.10	1.20
Lead Thickness	c	0.35	0.40	0.44
Lead 2 width	b	0.41	0.50	0.56
Leads 1 & 3 width	b1	0.36	0.42	0.48