Multi-Port High-Speed ONFI Switch (ENHub) with Presence Indication

Features

- 19 Signal 4:1 Mux/Demux
- Supports Switching from Host Port to One of Four ONFI NAND ports
- Switching Time - 12ns Typical
- 1000MHz Bandwidth for Each Channel
- Low Propagation Delay of 500ps Max
- Max. 10ps Skew within Differential Signals
- Max. 50ps Skew for Bus Signals in Group (within Same NAND Port)
- Switch Presence Indication
- Low Operating Power Supply: 2.375V – 3.6V
- Wide Temperature Range: 0°C to 100°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Package: 115-ball TFBGA (7mm×7mm) with 0.5mm Pitch

Description

The PI3SSD1914 is designed to work in ONFI applications for advanced SSD SKUs. The purpose of the PI3SSD1914 is to effectively de-multiplex ONFI-4 NAND commands and write data to one of the NAND ports as shown in Figure 1.

The device also multiplexes the ONFI-4 NAND bus on a particular ONFI-4 NAND port to allow a selected target NAND bus to be routed to the host controller for data reads as shown in Figure 2.

The PI3SSD1914 multiplexes/de-multiplexes, four ONFI-4-compliant NAND ports with typical 12ns switching time and maximum 500ps propagation delay. The core of the PI3SSD1914 operates at a supply voltage of 2.5V to 3.6V while the I/O interface circuits operate with an independent supply voltage from 1.2V to 1.8V. The supply voltage can be further reduced to 2.375V (min) for 1.2V VDDIO applications.

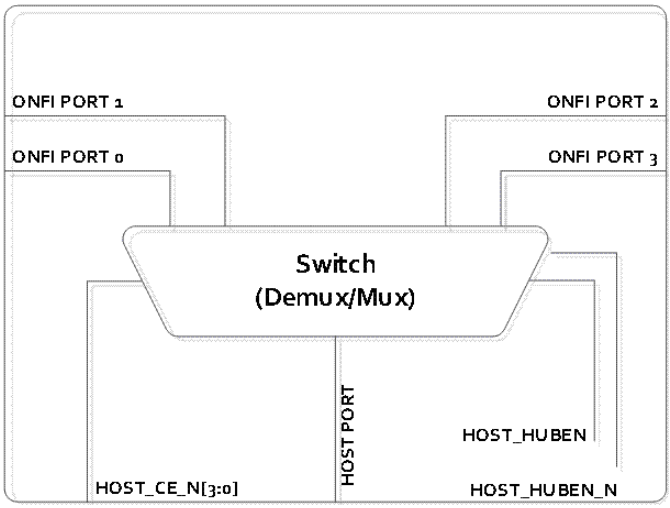


Figure 1: Block Diagram

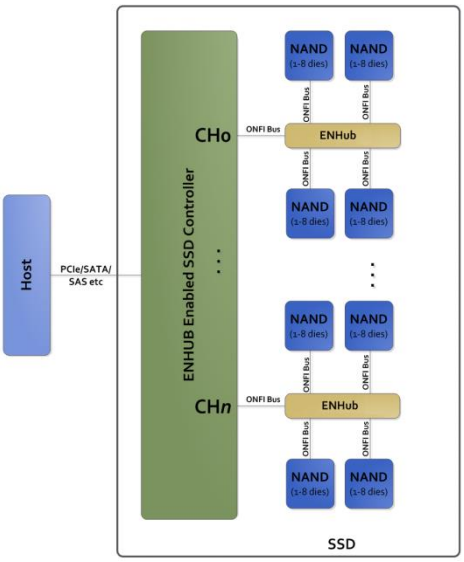
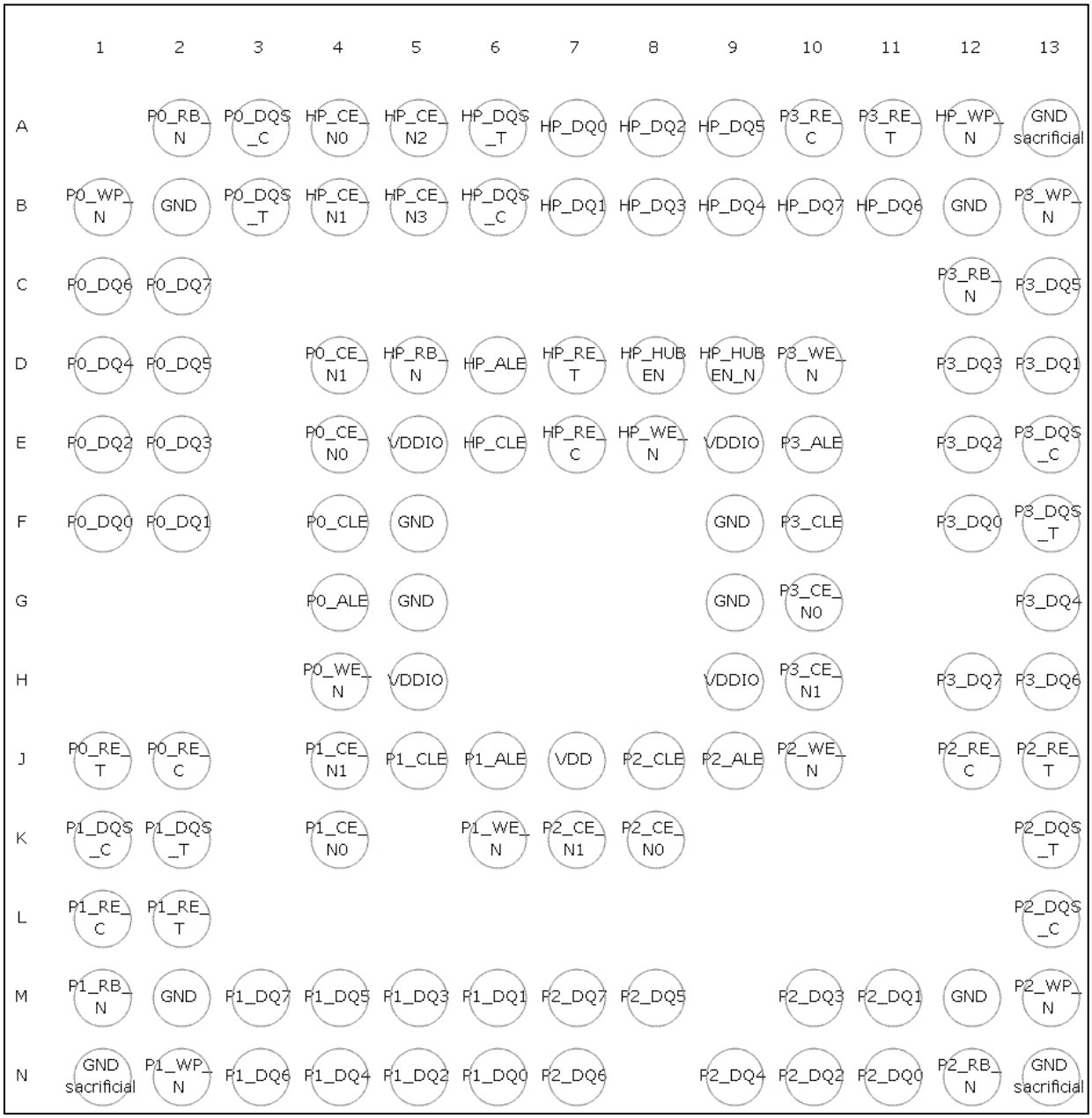


Figure 2: ENHub Enabled SSD Architecture

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Assignment (Top View)



ENHub Pin Diagram

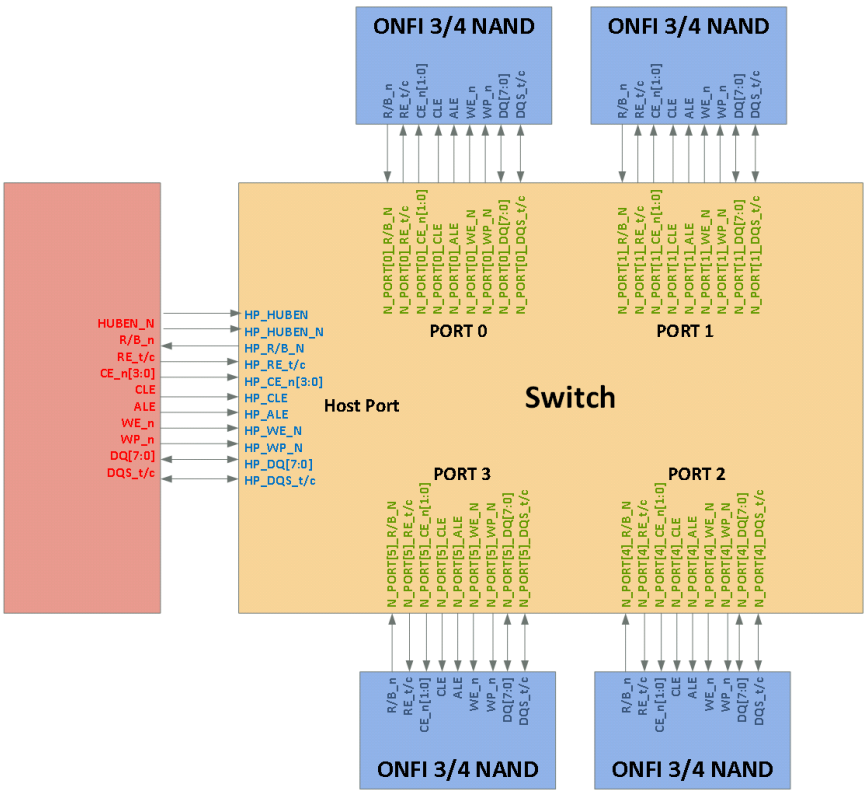


Figure 3. PI3SSD1914 EnHub Interconnect Diagram

As shown in Figure 3, the ENHub has the following ports:

- Four ONFI NAND ports that interface to ONFI3/4-compatible NAND with two CE_N signals each.
- A host port that interfaces to the host controller with the following ENHUB control signals:
  - HUBEN and HUBEN_N signals that enable the ENHUB.
  - Four HP_CE_N signals that indicate which ONFI NAND port to select. One combination indicates nothing is selected, and one combination indicates ENHub is selected (see Table 5).

In normal operation, the host controller enables the ENHub using the HUBEN and HUBEN_N pins then selects the appropriate ONFI NAND port using the HP_CE_N signals. These signals are decoded by the ENHub and drive the CE_N pins to control the specific NAND port. Once selected, the ONFI data and control signals from the host controller are channeled through FET switches to the appropriate NAND port.

Power Supply Signals

Signal	Description
VDD	Core Supply Voltage: 2.5V to 3.6V
VDDIO	Digital I/O Supply Voltage – NAND Interface: 1.8V or 1.2V ±10%
VSS	Ground

It is most recommended to firstly power-up VDD for 500µs before voltage is applied to VDDIO. By connecting HP_HUB_EN to VDDIO, the N_PORT[3:0]_CE_N[1:0] signals are outputted directly based on the decoding table provided in Table 5. The 500µs delay would ensure the analog circuitry is ready before the N port is activated by the N_PORT[3:0]_CE_N[1:0] signals.

It is also possible to ramp up VDD and VDDIO at the same time. In this case, even though the HP_HUB_EN is connected with VDDIO, the N_PORT[3:0]_CE_N[1:0] first goes to its default state (all pullup) and waits until the analogy circuitry is ready. As soon as the analogy circuitry is powered-up and ready (less than 500µs), the corresponding data channels and N_PORT[3:0]_CE_N[1:0] is outputted according to the decoding tale provided in Table 5.

It is not recommended to ramp up VDDIO prior to VDD to avoid potential I/O leakages.

IO Description

This section describes the signals for all the interfaces of PI3SSD1914.
Table 1 lists the signal types that are referenced in the descriptions. The voltages listed in the type field indicate nominal operating voltages.

Table 1: Signal Types

Signal Type	Description
I	Input
I/O	Input and output
O	Output
D	Differential Signal with true (_t) and complement (_c) components
*	Voltage only used for ONFI-4 Interface

ONFI Port Interfaces for PI3SSD1914

- Used for connection to the ONFI-4/3 NAND devices.
- Supports Asynchronous Timing modes 0 (10MT/s) and 5 (50MT/s)
- Supports NVDDR Timing modes 2 (100MT/s), 3 (133MT/s), 4 (166MT/s), 5 (200MT/s)
- Supports NVDDR2/3 Timing modes 2 (100MT/s), 3 (133MT/s), 4 (166MT/s), 5 (200MT/s), 6 (266MT/s), 7 (400MT/s), 8 (533MT/s), 9 (667MT/s), and 10 (800MT/s)
- Four ONFI Ports with two CEs each.

Table 2: NAND Interface Signals

Signal	Type	Description
N_PORT[3:0]_DQ[7:0]	I/O 1.8V/1.2V*	**Data** This bidirectional bus transfers address, data, and command information.
N_PORT[3:0]_DQS_t N_PORT[3:0]_DQS_c	I/O 1.8V/1.2V* D	**Data Strobes (Sync)** The bidirectional data strobes are used in sync mode only. They are inputs for reads and edge-aligned with read data. They are outputs for writes and center-aligned with write data.
N_PORT[3:0]_ALE	O 1.8V/1.2V*	**Address Latch Enable** When high, this signal indicates an address is on the corresponding port's DQ [7:0]. ALE signal on the corresponding port is also used to enter and exit data input or output modes.
N_PORT[3:0]_CLE	O 1.8V/1.2V*	**Command Latch Enable** When high, this signal indicates a command is on the corresponding port's DQ [7:0]. CLE signal on the corresponding port is also used to

Signal	Type	Description
		enter and exit data input or output modes.
N_PORT[3:0]_RE_t N_PORT[3:0]_RE_c	O 1.8V/1.2V* D	**Read Enable (Async)/Read Strobes (Sync)** *Asynchronous Mode:* The falling edge of this signal triggers the NAND flash to output data for a read operation. *Synchronous Mode:* When high, the corresponding port's DQ [7:0] and DQS are inputs to the NAND flash. The Read Enable signal behaves as a strobe for data output from the NAND. In that case, DQ [7:0] and DQS from the corresponding port are outputs from the NAND flash.
N_PORT[3:0]_WE_N	O 1.8V/1.2V*	**Write Enable** *Asynchronous Mode:* The rising edge of this signal triggers the NAND flash to capture an address, command, or data for a write operation. *Synchronous Mode:* This signal controls the latching of commands and addresses in the NV-DDR2 or NV-DDR3 data interface. Data, commands and addresses are latched on the rising edge.
N_PORT[3:0]_CE_N[1:0]	O 1.8V/1.2V*	**Chip Enable** When low, these asynchronous outputs enable the corresponding NAND target devices. These pins are driven by the ENHUB based on the encodings in Table 5.
N_PORT[3:0]_R/B_N	I 1.8V/1.2V*	**Ready/Busy/Spare 1** This is the status pin connected to the NAND, indicating the completion of a command or device busy.
N_PORT[3:0]_WP_N	O 1.8V/1.2V*	**Write Protect/Spare 2** This is the write protect pin indicating the NAND should be Write Protected.

Host Port Interface

- Used for connection to the host controller which will use the ONFI-4 protocol.
- Supports Asynchronous Timing modes 0 (10MT/s) and 5 (50MT/s)
- Supports NVDDR Timing modes 2 (100MT/s), 3 (133MT/s), 4 (166MT/s), 5 (200MT/s)
- Supports NVDDR2/3 Timing modes 2 (100MT/s), 3 (133MT/s), 4 (166MT/s), 5 (200MT/s), 6 (266MT/s), 7 (400MT/s), 8 (533MT/s), 9 (667MT/s), and 10 (800MT/s).
- Four incoming CEs from the host
- Two Hub enable pins (HUBEN, HUBEN_N) for enabling the Hub. These are used to attach two ENHubs per channel.

Table 3: Upstream Port Interface Signals

Signal	Type	Description
HP_DQ_[7:0]	I/O 1.8V/1.2V*	**Data** This bidirectional bus transfers address, data, and command information from the host.
HP_DQS_t HP_DQS_c	I/O 1.8V/1.2V* D	**Data Strobes (Sync)** The bidirectional data strobes from host are used in sync mode only. They are inputs for reads and edge-aligned with read data. They are outputs for writes and center-aligned with write data.
HP_ALE	I 1.8V/1.2V*	**Address Latch Enable** When high, this signal indicates an address is on HP_DQ[7:0]. HP_ALE is also used to enter and exit data input or output modes.
HP_CLE	I 1.8V/1.2V*	**Command Latch Enable** When high, this signal indicates a command is on HP_DQ[7:0]. HP_CLE is also used to enter and exit data input or output modes.

Signal	Type	Description
HP_RE_t HP_RE_c	I 1.8V/1.2V* D	**Read Enable (Async)/Read Strobes (Sync)** *Asynchronous Mode:* The falling edge of this signal triggers output data for a read operation. *Synchronous Mode:* When high, HP_DQ[7:0] and HP_DQS are inputs to the NAND flash. The Read Enable signal behaves as a strobe for data output from the NAND. In that case, HP_DQ[7:0] and HP_ DQS pads are outputs from the NAND flash.
HP_WE_N	I 1.8V/1.2V*	**Write Enable** *Asynchronous Mode:* The rising edge of this signal triggers a capture of an address, command, or data for a write operation. *Synchronous Mode:* This signal controls the latching of commands and addresses in the NV-DDR2 or NV-DDR3 data interface. Data, commands, and addresses are latched on the rising edge.
HP_CE_N_[3:0]	I 1.8V/1.2V*	**Chip Enable** When low, these asynchronous outputs enable the corresponding NAND target devices attached. See Table 5 for encoding of these chip enable signals.
HP_R/B_N	O 1.8V/1.2V*	**Ready/Busy/Spare 1** This is the status pin indicating the completion of a command or device busy as indicated by the selected port.
HP_WP_N	I 1.8V/1.2V*	**Write Protect/Spare 2** This is the write protect pin indicating the NAND should be Write Protected on the selected port.
HP_HUBEN	I 1.8V/1.2V*	**ENHub Enable** This is the Hub enable pin, which enables ENHub functionality in conjunction with HP_HUBEN_N pin, as defined by Table 5.
HP_HUBEN_N	I 1.8V/1.2V*	**ENHub Enable Complement** This is the Hub enable pin, which enables ENHub functionality in conjunction with HP_HUBEN pin, as defined by Table 5.

Signal States in a Deselected Port

When a port is deselected, the ENHub pulls up to VDDIO or pulls down the signals in the affected port per Table 4, where all resistor values are 20KΩ.

All values are 20KΩ
U = Pullup to VDDIO
D = Pulldown to ground

Table 4: List of Pullup/Pulldown Resistors at Various I/Os

Signal Name	ENHub Internal Pullup/Pulldown
R/B_n	U
WP_n	U
RE_t	U
RE_c	D
CE_n[1:0]	N/A – Always Driven
CLE	D
ALE	D
WE_n	U
DQ[7:0]	U
DQS_t	U
DQS_c	D

Chip Enable and HUB Enable Pins

The HP_HUBEN and HP_HUBEN_N signals from the host are used to enable the ENHub. When HP_HUBEN_N pin is low, and the HP_HUBEN pin is high, the ENHub is enabled. All other combinations of these two pins would leave the ENHUB in "deselect all" mode and all incoming HP_CE_N[3:0] are ignored. To support two hubs on a channel, one ENHUB part ties HUBEN_N low and the other will tie HUBEN high. The remaining HUBEN and HUBEN_N pins are tied together and connected to a single host signal, enabling one hub when high, and the other when low.

The HP_CE_N_[3:0] signals from the host are used by the ENHub to determine which NAND port and corresponding CE_N to be connected to the host port.

For PI3SSD1914 with 4 ONFI NAND ports, the encoded HP_CE_N[3:0] signals provide CE addressability for 2 CE_N signals per NAND port (12 CE_Ns total). Note the CE# polarity.

The PI3SSD1914 generates the N_PORT[3:0]_CE_N[1:0] signals based on the decoding table provided in Table 5. These chip enable signals are active low.

Table 5: HP_CE_N Pin Decoding/Mapping for PI3SSD1914

PI3SSD1914	Hub Enable		Encoded HOST CE_N Vector				NAND PORT CE_N	NAND Port 0		NAND Port 1		NAND Port 2		NAND Port 3		PI3SSD1914
	HP_HUBEN	HP_HUBEN_N	HP_CE_N[3]	HP_CE_N[2]	HP_CE_N[1]	HP_CE_N[0]	Selected	CE0	CE1	CE0	CE1	CE0	CE1	CE0	CE1	
	0	x	x	x	x	x	Deselect all	1	1	1	1	1	1	1	1	
	x	1	x	x	x	x	Deselect all	1	1	1	1	1	1	1	1	
	1	0	1	1	1	1	Deselect all	1	1	1	1	1	1	1	1	
	1	0	1	1	1	0	Switch Selected	1	1	1	1	1	1	1	1	
	1	0	1	1	0	1	Port 0, CE 0	0	1	1	1	1	1	1	1	
	1	0	1	1	0	0	Reserved/Deselect all	1	1	1	1	1	1	1	1	
	1	0	1	0	1	1	Port 1, CE 0	1	1	0	1	1	1	1	1	
	1	0	1	0	1	0	Port 2, CE 0	1	1	1	1	0	1	1	1	
	1	0	1	0	0	1	Reserved/Deselect all	1	1	1	1	1	1	1	1	
	1	0	1	0	0	0	Port 3, CE 0	1	1	1	1	1	1	0	1	
	1	0	0	1	1	1	Reserved/Deselect all	1	1	1	1	1	1	1	1	
	1	0	0	1	1	0	Reserved/Deselect all	1	1	1	1	1	1	1	1	
	1	0	0	1	0	1	Port 0, CE 1	1	0	1	1	1	1	1	1	
	1	0	0	1	0	0	Reserved/Deselect all	1	1	1	1	1	1	1	1	
	1	0	0	0	1	1	Port 1, CE 1	1	1	1	0	1	1	1	1	
	1	0	0	0	1	0	Port 2, CE 1	1	1	1	1	1	0	1	1	
	1	0	0	0	0	1	Reserved/Deselect all	1	1	1	1	1	1	1	1	
	1	0	0	0	0	0	Port 3, CE 1	1	1	1	1	1	1	1	0	

When no NAND is selected, the corresponding decoded value will be asserted and used as a "deselect all" state where no CEs are selected. One pattern is reserved for ENHub selected which is used for ENHub identification. See following section.

ENHub Identification

When the value of HP_CE_N[3:0] is equal to '0b1110' (ENHub Selected), HP_RE_N is low, HP_HUBEN is high, and HP_HUBEN_N is low, the ENHub part returns the value of '0x5A' (0b0101 1010) on the DQ bus of the host port.

The value presented by the ENHub on the HP_DQ bus is read by the host controller and used to positively identify whether a ENHub is present on the channel or not.

The expected use case of this capability would be for the controller to issue a read ID command as shown in Figure 4, which is taken from an ONFI NAND datasheet.

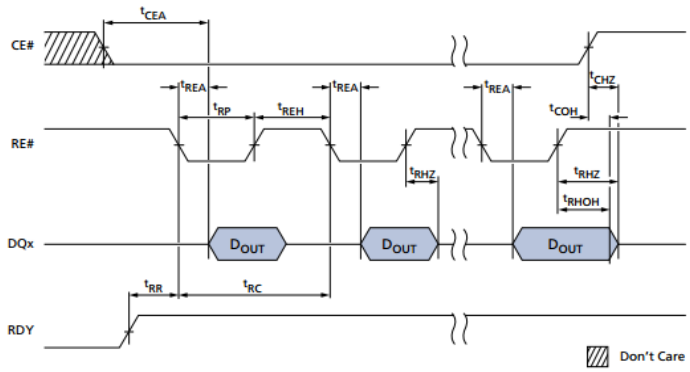


Figure 4: Timing Diagram of Read ID Command

Typically there would only be a single RE# pulse, but if the controller kept reading by issuing multiple pulses, it would get the same value for DOUT (0x5A) each time. ENHub does not control the RDY signal. The value driven on the bus is the same for all ENHub parts. Table 6 is a truth table of ENHub identification.

Table 6: Truth Table of ENHub Identification

Input					**Output**
HP_HUBEN	HP_HUBEN_N	HP_CE_N<3:0>	HP_RE_t	HP_RE_c	HP_DQ_<7:0>
X	1	X	X	X	Hi-Z
0	X	X	X	X	Hi-Z
1	0	0b1110	1	X	Hi-Z
1	0	0b1110	0	X	0x5A

Maximum Ratings

Storage Temperature	-65°C to +150°C
Junction Temperature	125°C
Core Supply Voltage (VDD)	-0.3V to +3.8V
VDDIO Voltage	-0.3V to +2.4V
Peak Current (Channels)	50mA
Input Voltage (Channels)	-0.3V to +2.4V
ESD: HBM all pins	2000V
CDM all pins	500V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Parameter		Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	For 1.2V to 1.8V VDDIO	2.5	3.3	3.6	V
		For 1.2V VDDIO	2.375	2.5	3.6	
VDDIO	IO Supply Voltage		1.62 1.08	1.8 1.2	1.98 1.32	V
Ta	Ambient Temperature		0	25	100	°C
Tj	Junction Temperature		0	—	125	°C
Pw	Operating Power Target		—	—	0.1	W

DC Electrical Characteristics

Minimum/Maximum values apply for T_A between 0°C to 100°C (unless otherwise noted).
Typical values are referenced to T_A=+25°C, V_{DD}=3.3V±10%, V_{DDIO}=1.8V (unless otherwise noted).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Switch on Resistance						
R_{ON}	All Channels	I_{LOAD} = -8mA, V_{in} = 0V, 1.8V	—	5	8	Ω
I_{OZ}	Output Leakage Current for ONFI NAND Port when Port is Off	V_{DD} = 3.3V, switch = off, V_{in} = 0V (for ports with internal pulldown*) V_{in} = 1.8V (for ports with internal pullup*)	—	—	±2	µA
Interface Pin						
V_{IH}	Input High Voltage of HP_CE_N	—	$0.7V_{DDIO}$	—	V_{DDIO}+0.4	V
V_{IL}	Input Low Voltage of HP_CE_N	—	-0.3	—	$0.3V_{DDIO}$	V
I_{IC}	Input Current of HP_CE_N	V_{IC} = 0V, 1.8V	-1	—	1	µA
V_{OH}	Output High Voltage	+2.5mA source current	V_{DDIO} -0.2	—	—	V
V_{OL}	Output Low Voltage	-2.5mA sink current	—	—	0.2	V
Current Consumption						
I_{DD}	Core Supply Current	—	—	—	200	µA
I_{VDDIO}	VDDIO Supply Current	All ports deselected	—	—	60	µA
R_{UD}	Pullup/Pulldown Resistor	—	10	20	36	kΩ
V_{UVLD}	VDD Under Voltage Lockout	—	—	—	2.3	V

*** See Table 4**

Capacitance

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_I	Capacitance for each HP_CE_N pin	f = 1MHz	—	2	—	pF
C_{ON}	On Capacitance of Each Channel	f = 1MHz	—	5	—	pF
COFF	Off Capacitance of Each Channel	f = 1MHz	—	4.5	—	pF

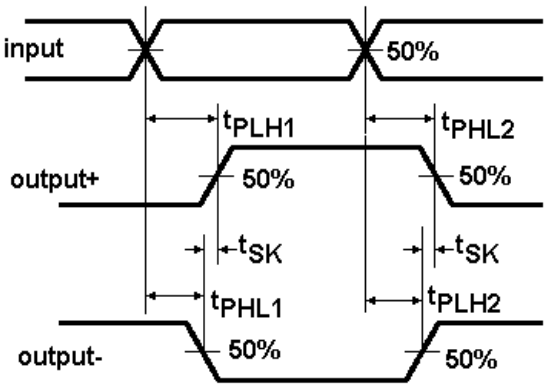
Switch AC Electrical Characteristics

Minimum/Maximum values apply for T_A between 0°C to 100°C (unless otherwise noted).
Typical values are referenced to T_A=+25°C, V_{DD}=3.3V±10%, V_{DDIO}=1.8V (unless otherwise noted).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
DB-3dB	-3dB Differential Bandwidth	C_L = 0pF	—	1	—	GHz
SB-3dB	-3dB Single-Ended Bandwidth	C_L = 0pF	—	1	—	GHz
DDDIL	Differential Insertion Loss	C_L = 0pF, Channel is ON, f = 266MHz	—	-0.9	—	dB
		C_L = 0pF, Channel is ON, f = 400MHz	—	-1	—	dB
DDI	Channel Off Isolation	C_L = 0pF, Channel is OFF, f=266MHz	—	-30	—	dB
		C_L = 0pF, Channel is OFF, f=400MHz	—	-28	—	dB
DDRL	Differential Return Loss	C_L = 0pF, f = 266MHz	—	-13	—	dB
		C_L = 0pF, f = 400MHz	—	-10	—	dB
Tskd	Differential Skew Time (Figure 5)	R_S = R_L = 50Ω, C_L = 30pF (between 'n' and 'p' within the differential pair)	—	—	10	ps
Tskb	Bus Skew Time (Figure 6)	R_S=R_L=50Ω, C_L=30pF (all signals within a 'bus' (NAND port) group)	—	—	50	ps
Tprog	Propagation Delay between Host Port signals and N_Port[n] Signals (Figure 7)	R_S = R_L = 50Ω, C_L = 30pF	—	—	500	ps
Tsw	Port Switching Time (Figure 8)	C_L = 30pF	—	12	20	ns

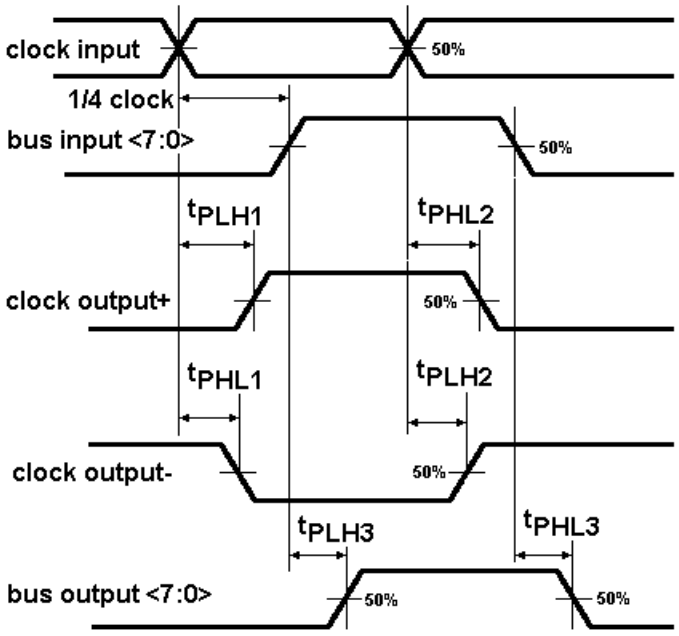
Note: S-parameters are measured with 50Ω source termination and 50Ω load termination (no capacitive loads).
Skew is measured one channel at a time.

Parameter Measurement Information



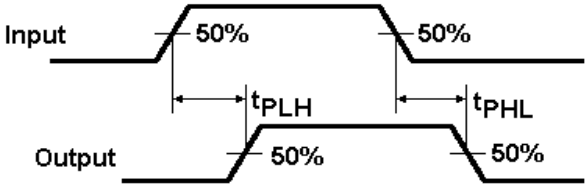
$t_{SKD} = |t_{PHL1} - t_{PLH1}|$ or $|t_{PHL2} - t_{PLH2}|$

Figure 5: Differential Skew Time



$t_{SKB} = \max(t_{PLH1}, t_{PHL1}, t_{PLH3}) - \min(t_{PLH1}, t_{PHL1}, t_{PLH3})$
or $\max(t_{PHL2}, t_{PLH2}, t_{PHL3}) - \min(t_{PHL2}, t_{PLH2}, t_{PHL3})$

Figure 6: Bus Skew Time



$t_{PROG} = t_{PLH}$ or t_{PHL}

Figure 7: Propagation delay

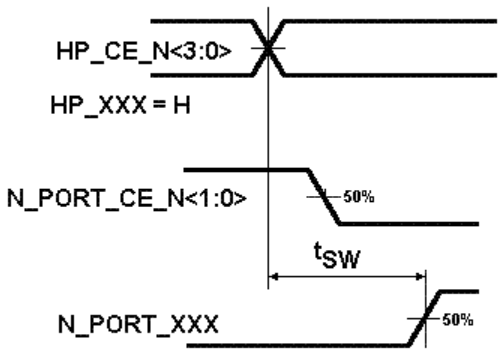


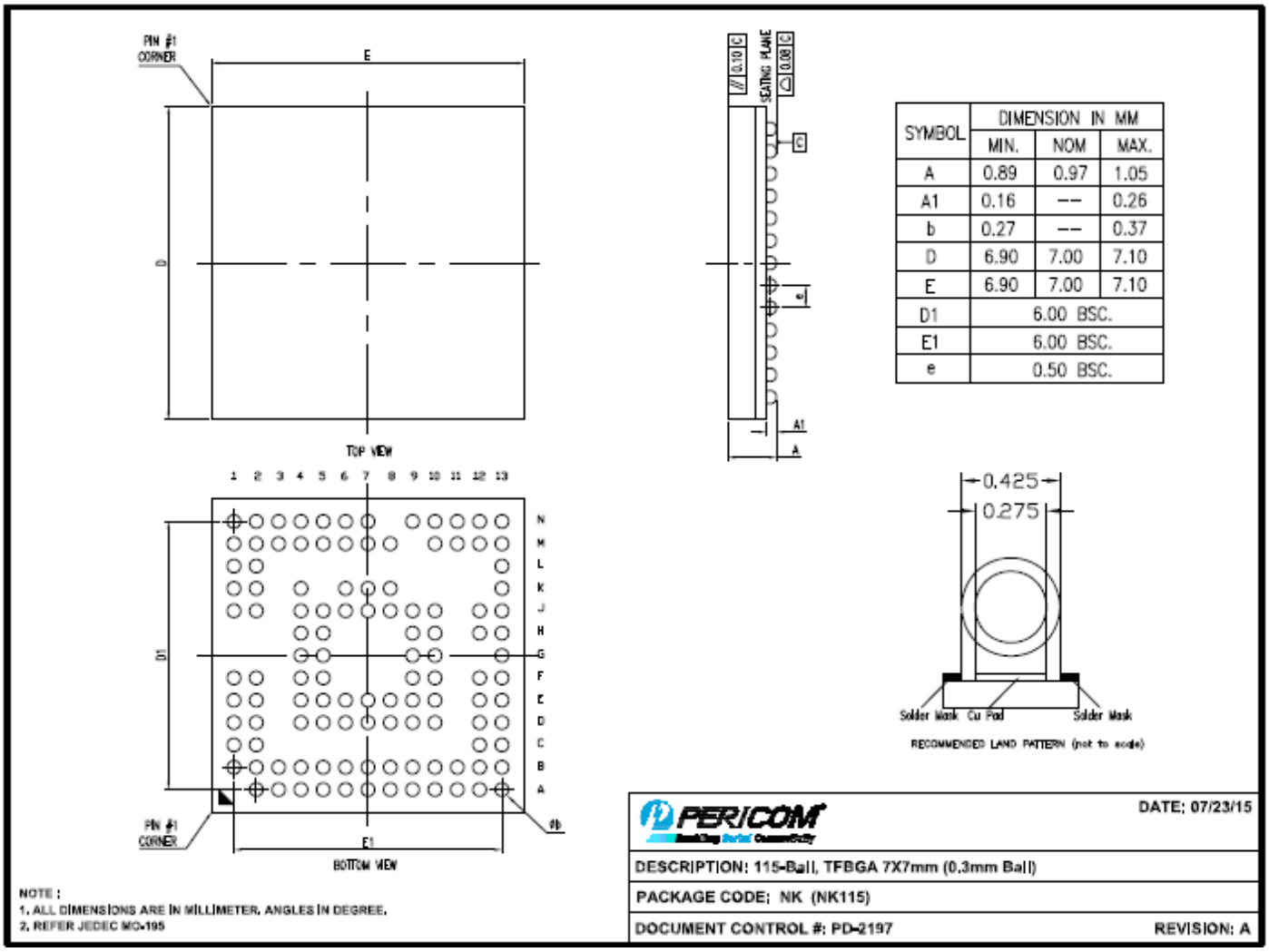
Figure 8: Port Switching Time

Part Marking

Greatek with Au Wire

Packaging Mechanical:

115-TFBGA (NK)



SYMBOL	DIMENSION IN MM		
	MIN.	NOM	MAX.
A	0.89	0.97	1.05
A1	0.16	--	0.26
b	0.27	--	0.37
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D1	6.00 BSC.		
E1	6.00 BSC.		
e	0.50 BSC.		

NOTE :
1. ALL DIMENSIONS ARE IN MILLIMETER, ANGLES IN DEGREE.
2. REFER JEDEC MO-195

PERICOM

DATE: 07/23/15

DESCRIPTION: 115-Ball, TFBGA 7X7mm (0.3mm Ball)

PACKAGE CODE: NK (NK115)

DOCUMENT CONTROL #: PD-2197 REVISION: A

For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Ordering Number	Package Code	Package Description
PI3SSD1914NKE+DG	NK	115-Ball, 7mm×7mm (0.3mm Ball) (TFBGA) (Greatek) with Au Wire
PI3SSD1914NKE+DGX	NK	115-Ball, 7mm×7mm (0.3mm Ball) (TFBGA) Greatek tape & reel for Au wire

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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