Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

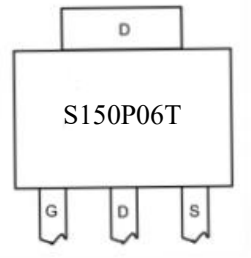
Bvdss	Rdson	ID
-60V	3.6mΩ	-150A

RoHS

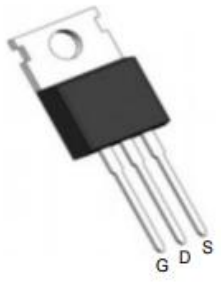
Application

- DC-DC Converters
- Synchronous-rectification applications
- Power management functions

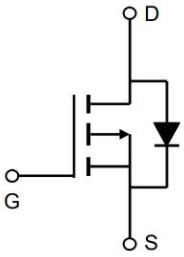
Package



Marking and pin assignment



TO-220 top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
150P06	S150P06T	TO-220	50

Absolute Maximum Ratings (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25° C	I_D	-150	A
	T_C=100° C	I_D	-91.7	A
Pulsed Drain Current		I_{DM}[1]	-580	A
Single Pulse Avalanche Energy		E_{AS}[2]	2058	mJ
Power Dissipation	T_C = 25℃	P_D	183	W
Operating junction and storage temperature		T_J, T_{STG}	150, -55 ~ 150	℃
Maximum Temperature for Soldering		T_L	260	℃

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	0.68	℃/W
Thermal Resistance, Junction -to-Ambient	$R_{\theta JA}$	60	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS150P06T	TO-220	1	2	3	Tube

Electrical Characteristics (Tj=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250μA	-60	-	-	V
Gate-body Leakage current	I_{GSS}	V_{GS}=±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-60V, V_{GS}=0V	-	-	1	μA
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS} , I_D = -250μA	-2	-2.4	-2.8	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -20A	-	3.6	4.3	mΩ
Input Capacitance	C_{ISS}	V_{DS} = -30V,V_{GS} =0V, f =1MHz	-	9123	-	pF
Output Capacitance	C_{OSS}		-	1583	-	
Reverse Transfer Capacitance	C_{RSS}		-	85.6	-	
Gate Resistance	R_g	-	-	-	-	Ω
Total Gate Charge	Q_g	V_{GS} = -10V,V_{DS} = -30V, I_D = -10A	-	135	-	nC
Gate-Source Charge	Q_{gs}		-	28	-	
Gate-Drain Charge	Q_{gd}		-	22.4	-	
Turn-On Delay Time	$T_{d(on)}$	V_{GS} = -10V, V_{DS} = -30V, R_G = 3Ω, I_D = -10A	-	70	-	ns
Rise Time	T_R		-	45	-	
Turn-Off Delay Time	$T_{d(off)}$		-	165	-	
Fall Time	T_F		-	50	-	
Diode Forward Current	I_S	T_C=25℃	-	-	-150	A
Diode Forward Voltage	V_{SD}	I_S=-20A, V_{GS}=0V	-	-	-1.2	V
Reverse Recovery time	T_{rr}	I_S=-10A, V_{DD}=-30V dI/dt=100A/μs	-	45	-	ns
Reverse Recovery Charge	Q_{rr}		-	100	-	nC

Typical Performance Characteristics

Fig1:Typ. output characteristics

ID=f(-VDS)

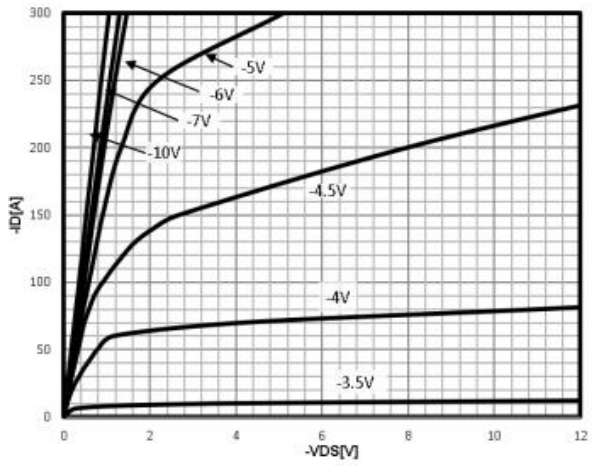


Fig2:Typ. drain-source on resistance

RDS(on)=f(-ID)

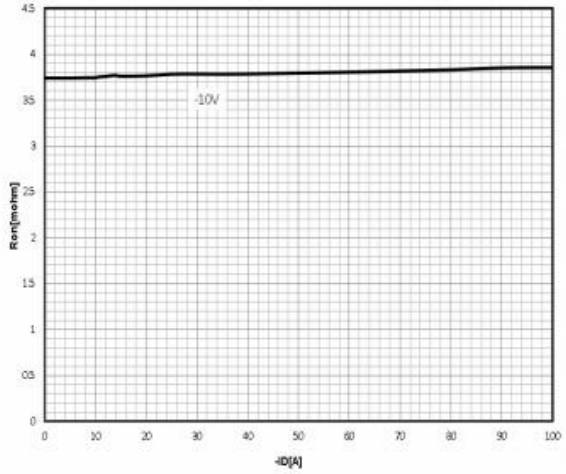


Fig3:Typ. transfer characteristics

$-I_D=f(-V_{GS})$;

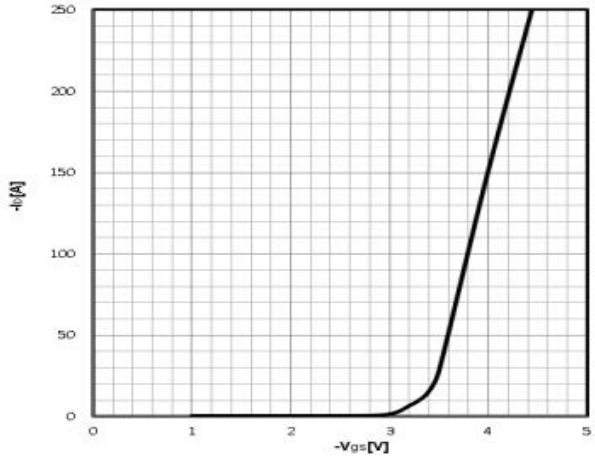


Fig4:Drain-source on-state resistance

RDS(on)=f(Tj);ID=-20A; VGS=-10V

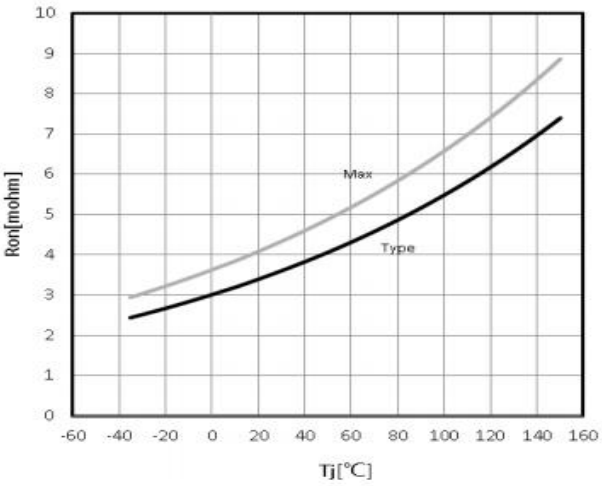


Fig5:Gate Threshold Voltage

-VTH=f(Tj); ID=-250uA

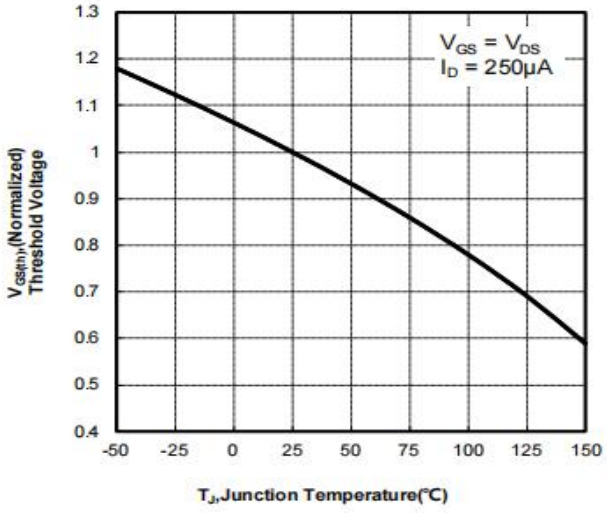


Fig6:Drain-source breakdown voltage

VBR(DSS)=f(Tj); ID=-250uA

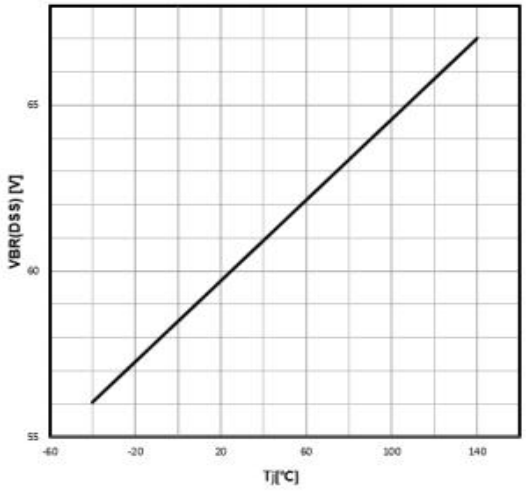


Fig7:Typ. gate charge

VGS=f(Qg), ID=-10A;

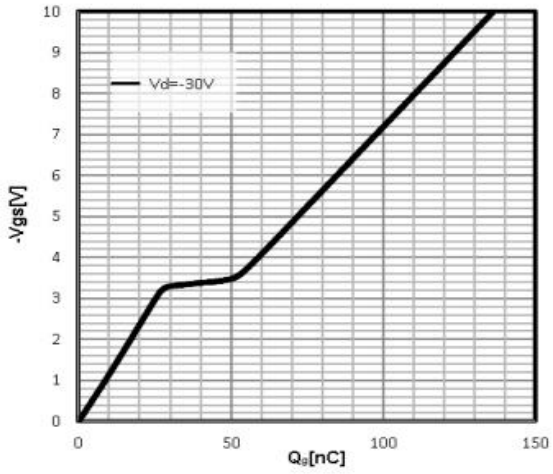


Fig8:Typ. capacitances

C =f(VDS); VGS=0V; f =1MHz

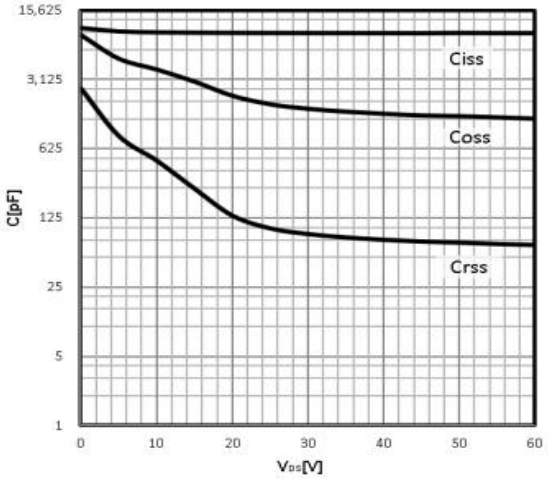


Fig9:Power Dissipation

$P_{tot}=f(T_C)$

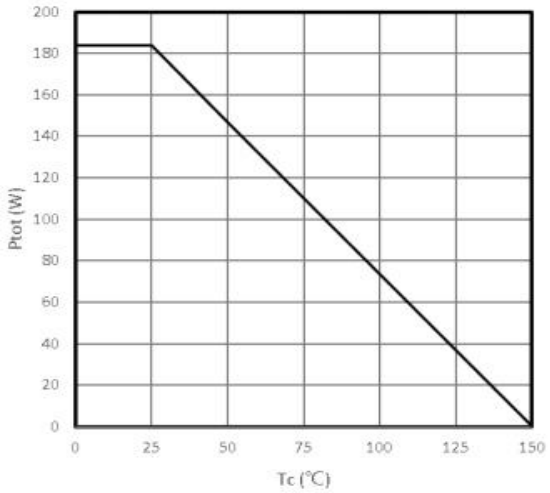


Fig10:Maximum Drain Current

-ID=f(TC)

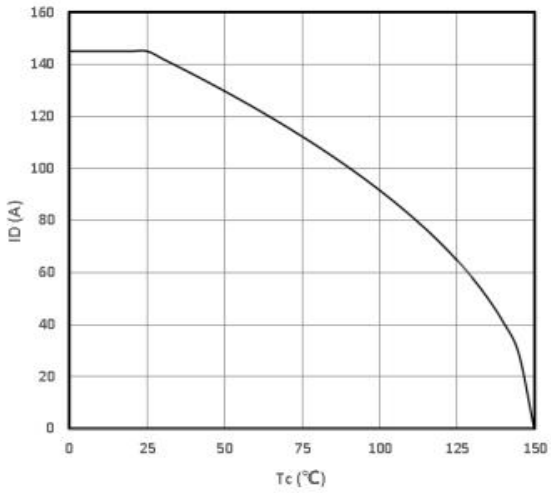


Fig11:Safe operating area

ID=f(VDS)

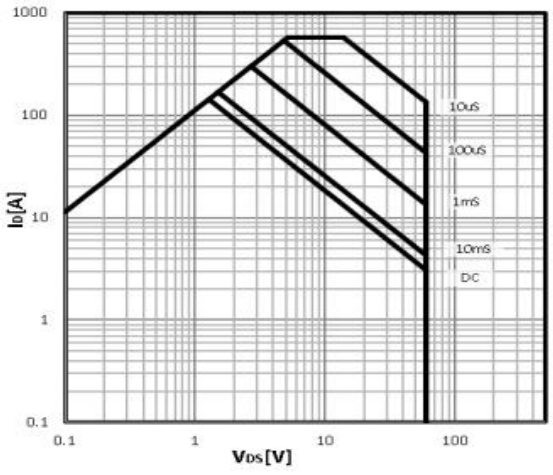


Fig12:Body Diode Forward Voltage Variation

-IF=f(-VDS)

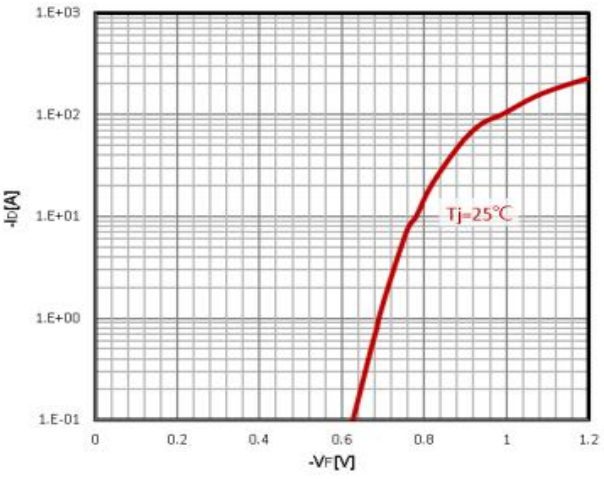
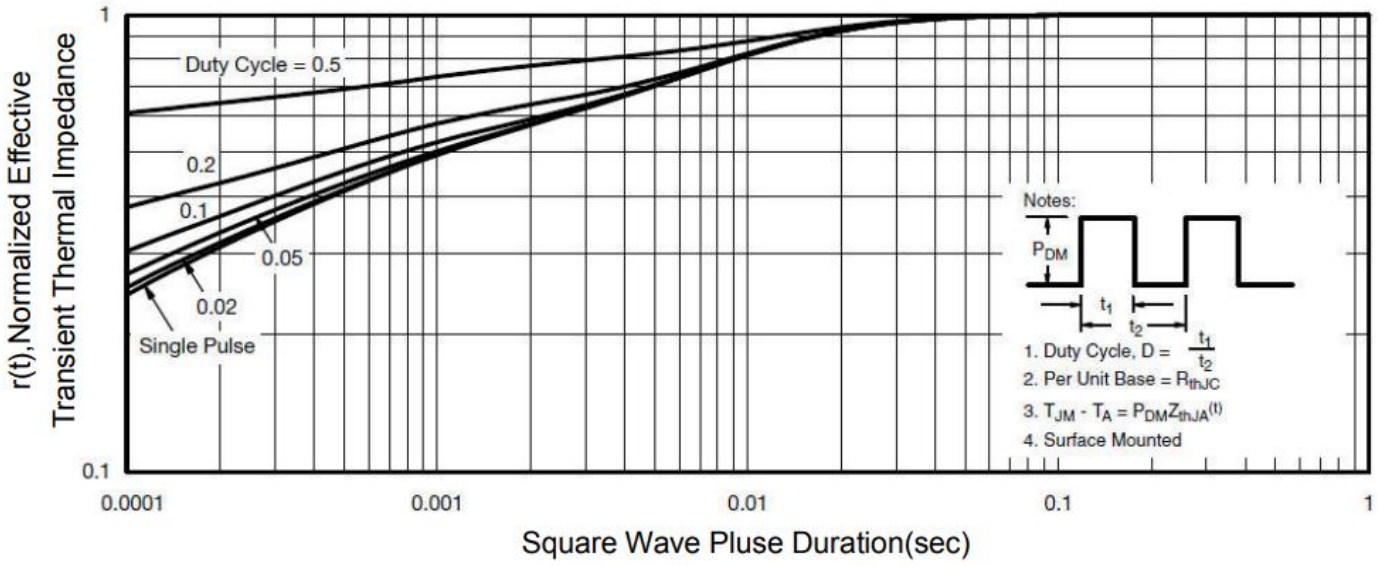


Figure 13: Max. Transient Thermal Impedance

$Z_{thJC}=f(t_p)$



Test Circuit and Waveform:

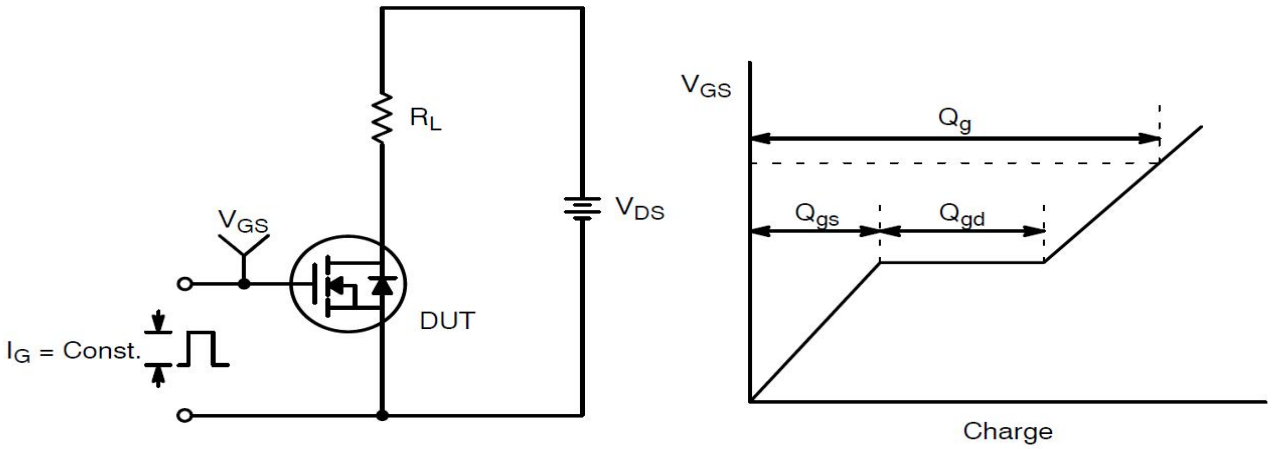


Figure.1： Gate Charge Test Circuit & Waveform

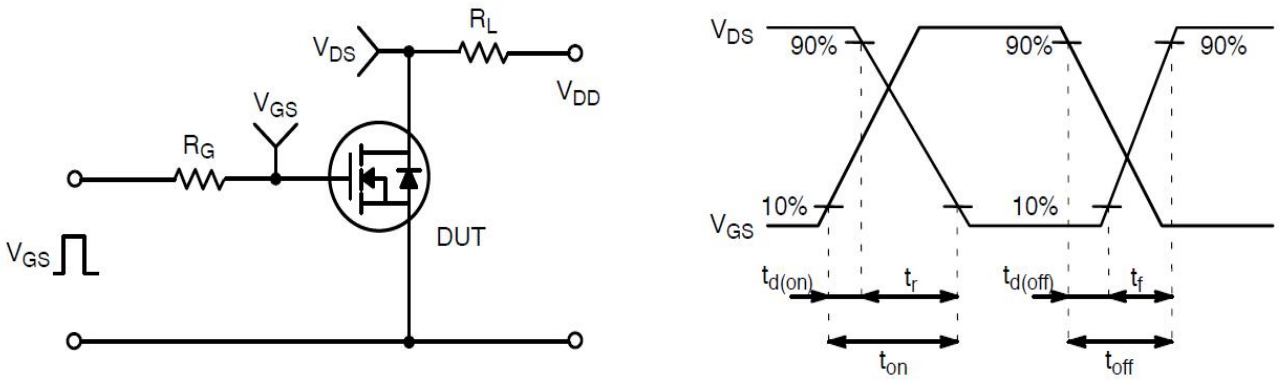


Figure.2： Resistive Switching Test Circuit & Wave forms

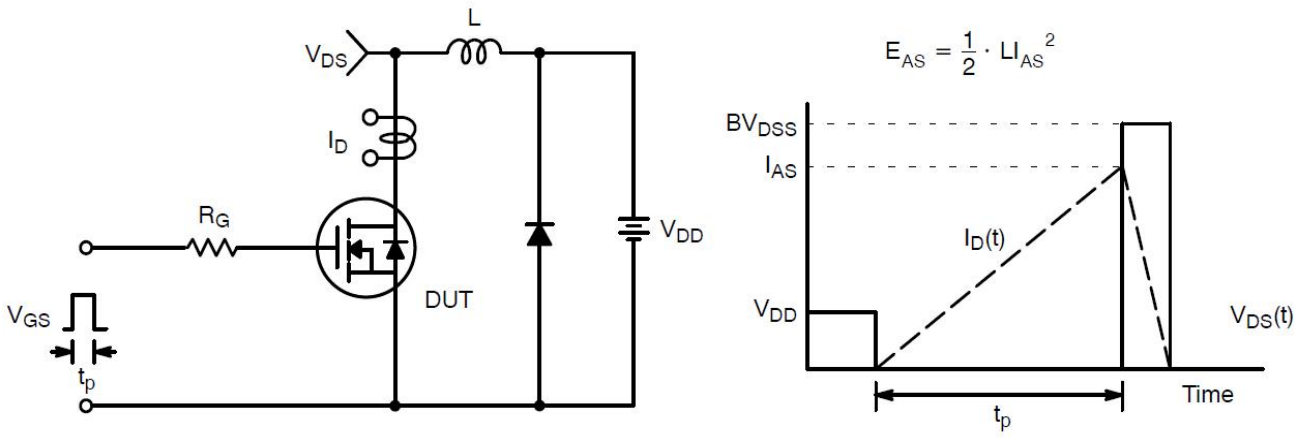
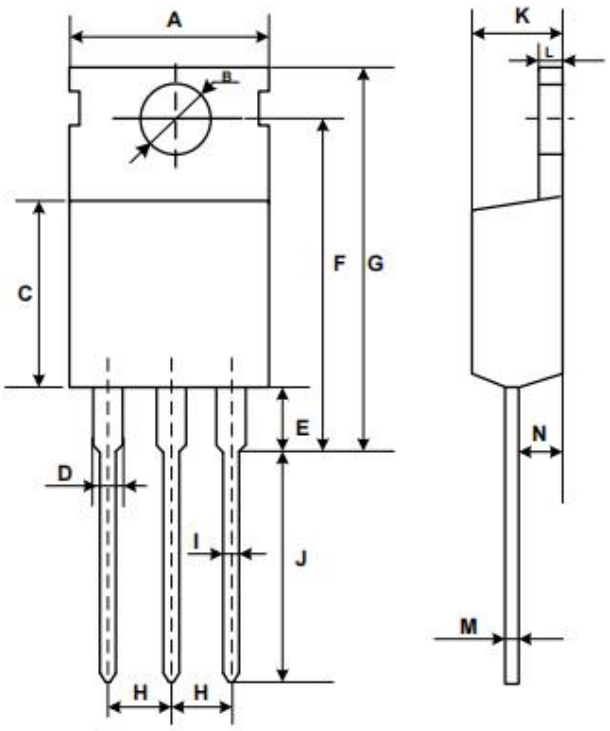


Figure.3： Unclamped inductive Switching Test Circuit & Wave forms

Package Dimensions TO-220



OMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	9.70	10.30
B	3.40	3.80
C	8.80	9.40
D	1.17	1.47
E	2.60	3.50
F	15.10	16.70
G	19.55MAX	
H	2.54REF	
I	0.70	0.95
J	9.35	11.00
K	4.30	4.77
L	1.20	1.45
M	0.40	0.65
N	2.20	2.60

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