SFT040N150C3

N-MOSFET 150V, 3.3mΩ, 190A

Features

- Low on resistance
- Low gate charge
- Fast switching
- High avalanche current
- Low reverse transfer capacitances

Product Summary

V_{DS}	150V
$R_{DS(on)typ.}$	3.3mΩ
I_D	190A

100% DVDS Tested

100% Avalanche Tested

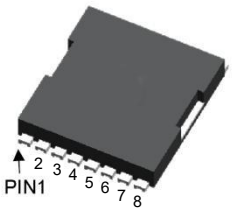
RoHS

Application

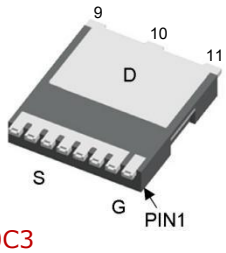
- Brushed and BLDC Motor drive systems
- Battery Management
- DC/DC and AC/DC Converter
- UPS

TOLL

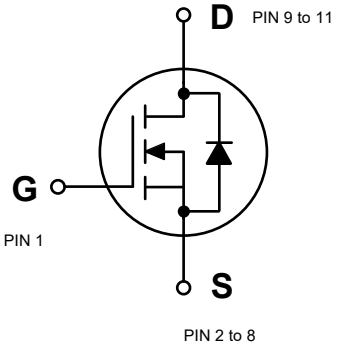
Top View



Bottom View



SFT040N150C3



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
SFT040N150C3	040N150C3	TOLL	Reel&Tape	330×28.5mm	24mm	2000pcs

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain - Source Voltage		V_{DS}	150	V
Gate - Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25℃	I_D	190	A
	T_C = 100℃		135	
Pulsed Drain Current(Tc=25℃,t_p limited by T_{jmax})		$I_{D,Pulse}$	760	A
Single Pulsed Avalanche Energy(T_C=25℃)		E_{AS}	2154	mJ
Power Dissipation	T_C = 25℃	P_{tot}	260	W
Junction Temperature		T_J	-55 ~ 150	℃
Storage Temperature		T_{STG}	-55 ~ 150	℃

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance , junction – case	R_{thJC}	0.48	℃/W
Thermal resistance , junction – ambient(min. footprint)	R_{thJA}	62	℃/W

Electrical Characteristics (T_J = 25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain - Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	150	165	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 150V, V_{GS} = 0V T_C=25℃ T_C=100℃	 - -	 - -	 1 100	μA
Gate - Body Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2	3	4	V
Drain-source On-resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 50A	-	3.3	4.0	mΩ
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS} = 75V, V_{GS} = 0V, f = 1MHz	-	9562	-	pF
Output Capacitance	C_{oss}		-	815	-	
Reverse Transfer Capacitance	C_{rss}		-	254	-	
Gate Resistance	R_g	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz	-	2.3	-	Ω
Switching Characteristics						
Total Gate Charge	Q_g	V_{DS} = 75V, V_{GS} = 10V, I_D = 50A	-	112	-	nC
Gate-source Charge	Q_{gs}		-	36	-	
Gate-drain Charge	Q_{gd}		-	25	-	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 75V, V_{GS} = 10V, R_G=4.7Ω	-	39	-	ns
Turn-on Rise Time	t_r		-	41	-	
Turn-off Delay Ttime	$t_{d(off)}$		-	72	-	
Turn-off Fall Time	t_f		-	15	-	

Body Diode Characteristic

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Diode continous forward current	I_S	-	-	-	190	A
Diode pulse current	$I_{S,pulse}$	Pulsed, tp ≤ 10 μs	-	-	760	A
Body Diode Forward Voltage	V_{SD}	V_{GS} = 0V,I_{SD} = 50A	-	-	1.2	V
Body Diode Reverse Recovery Time	T_{rr}	I_F=50A,di/dt=100A/μs	-	102	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=50A,di/dt=100A/μs	-	276	-	nC

Typical Performance Characteristics

Diagram 1: Power dissipation

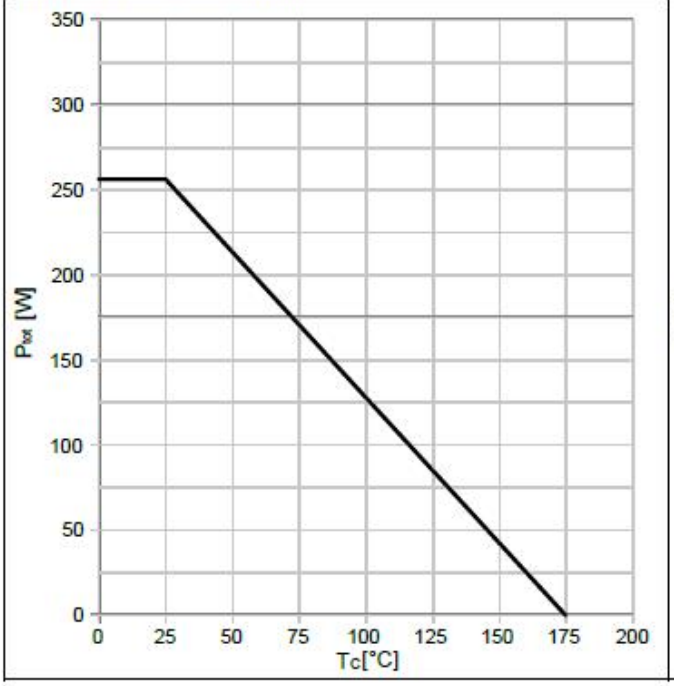


Diagram 2: Drain current

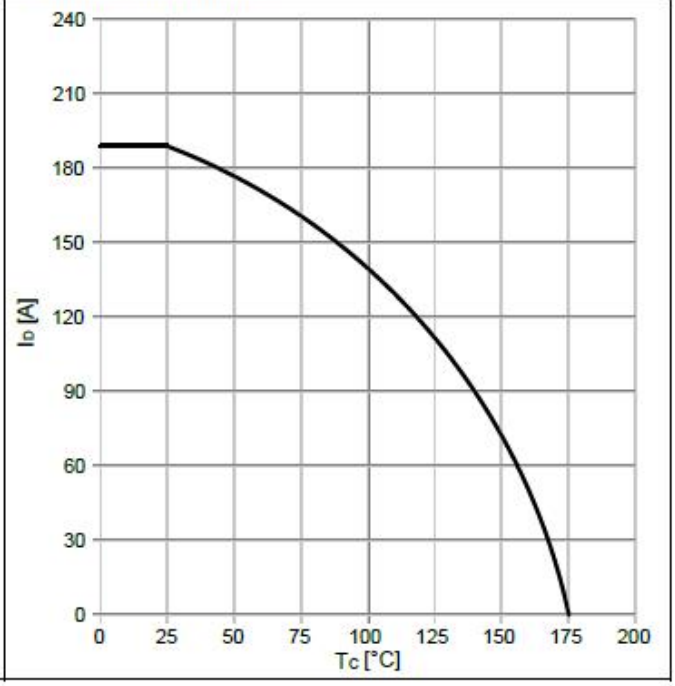


Diagram 3: Safe operating area

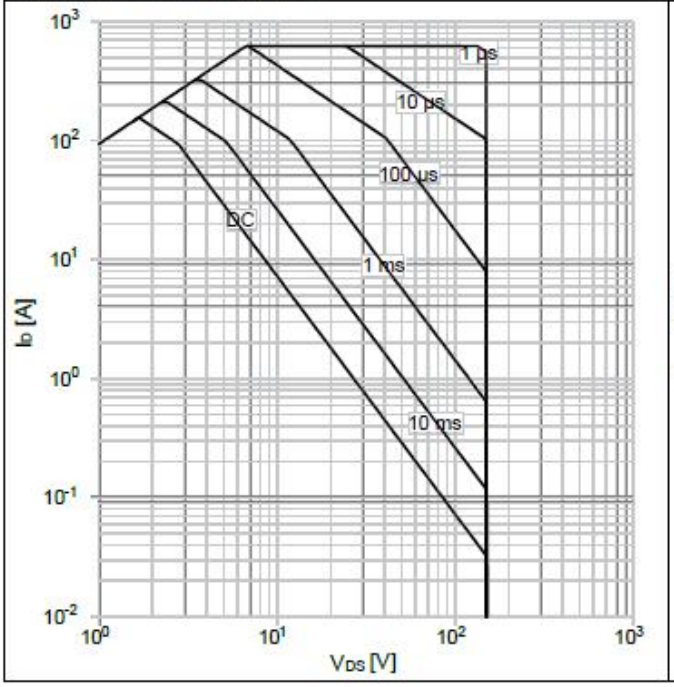


Diagram 4: Max. transient thermal impedance

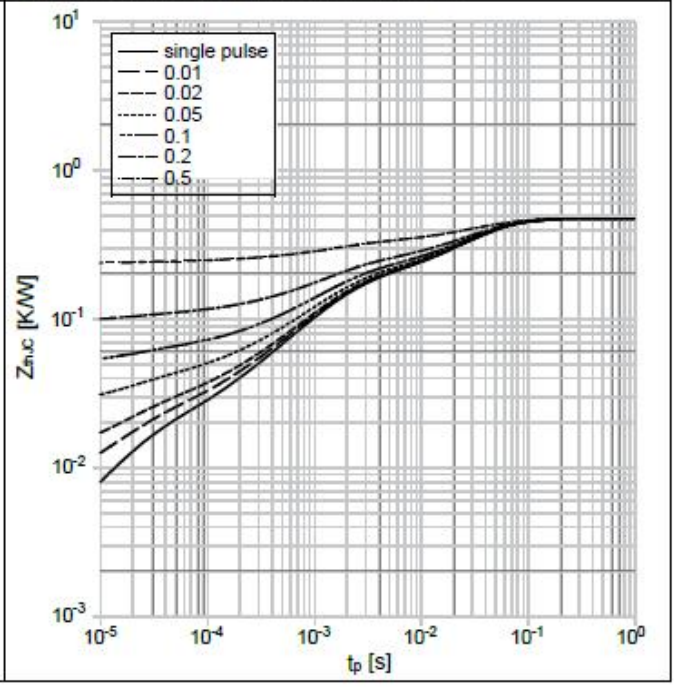
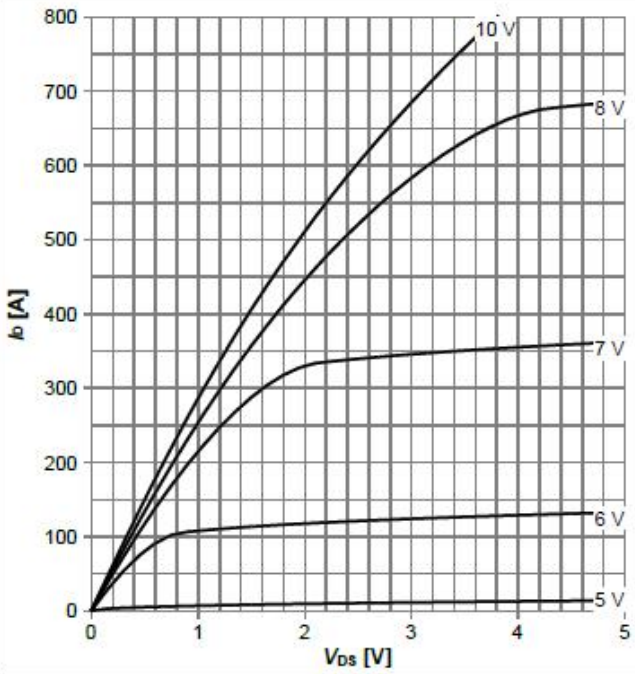
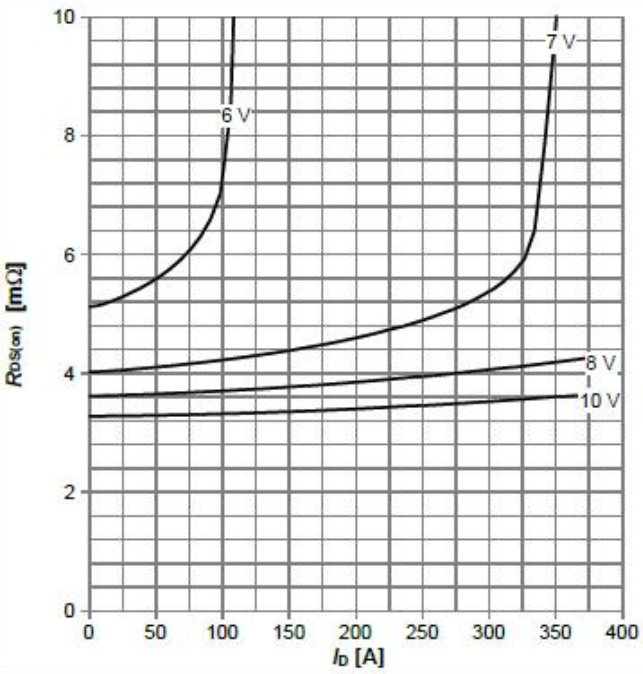


Diagram 5: Typ. output characteristics



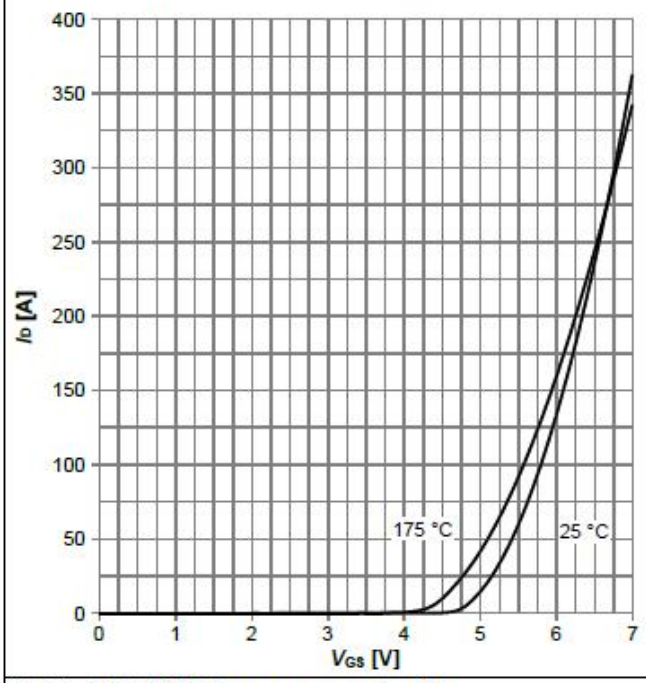
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



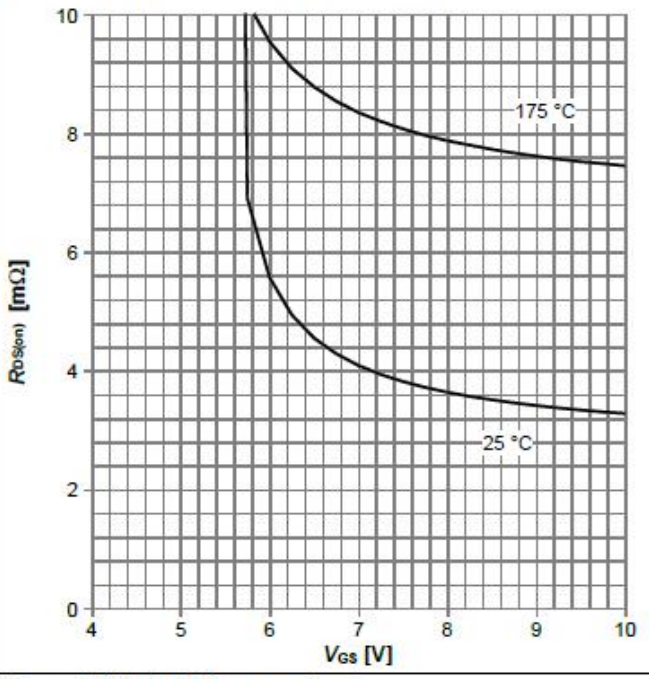
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



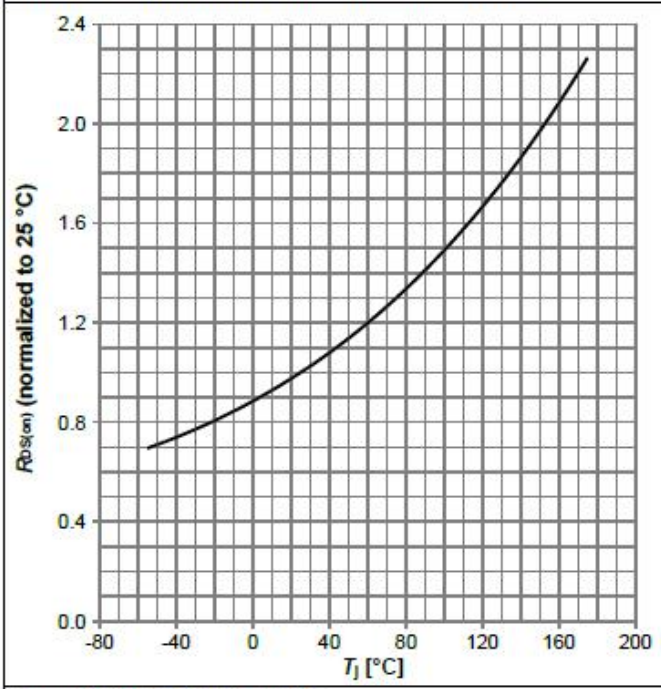
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



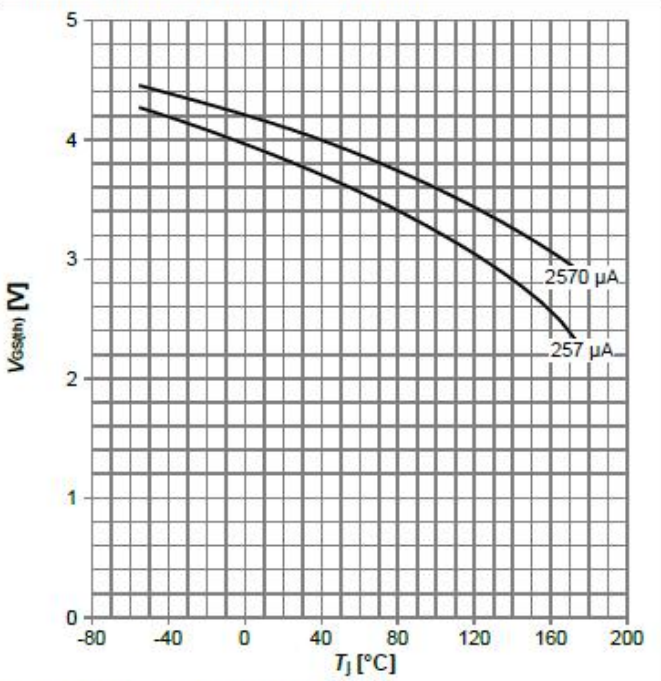
$R_{DS(on)}=f(V_{GS})$, $I_D=50$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



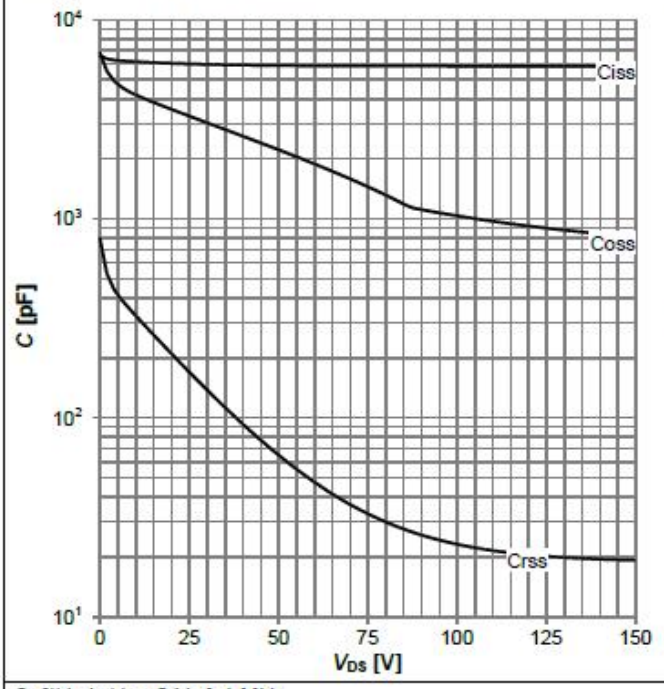
$R_{DS(on)}=f(T_j)$, I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



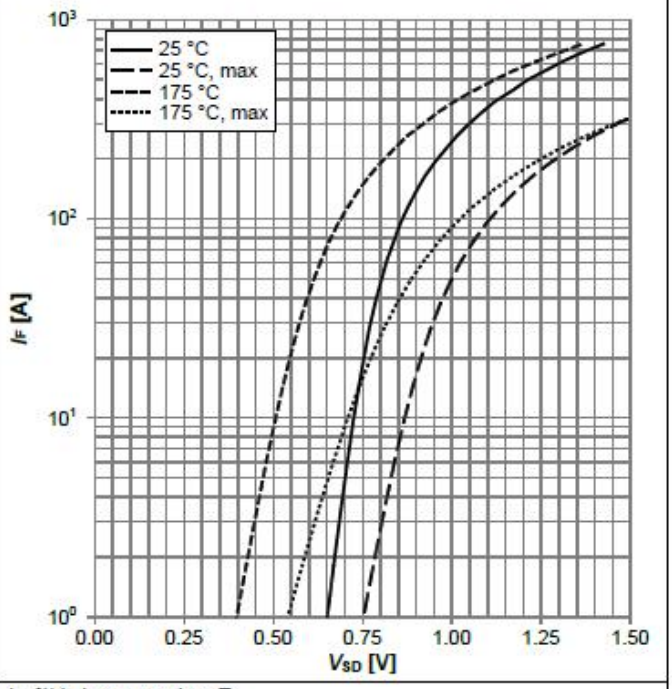
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



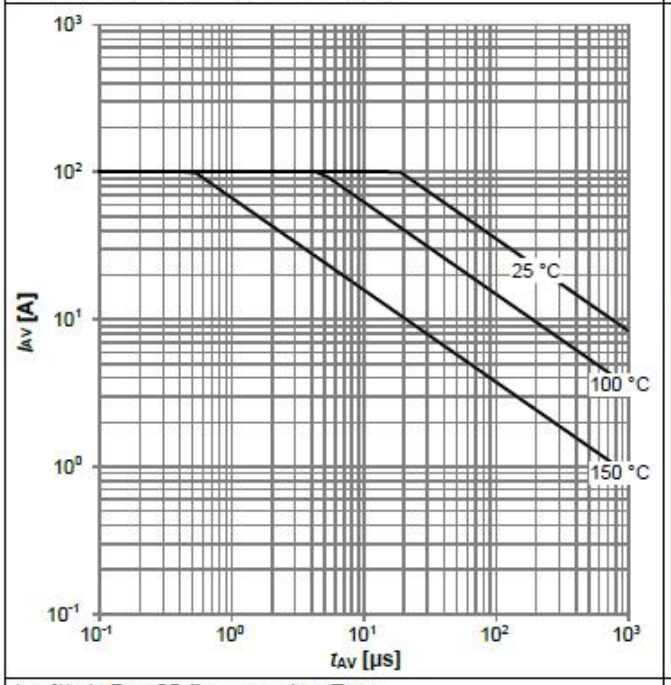
$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



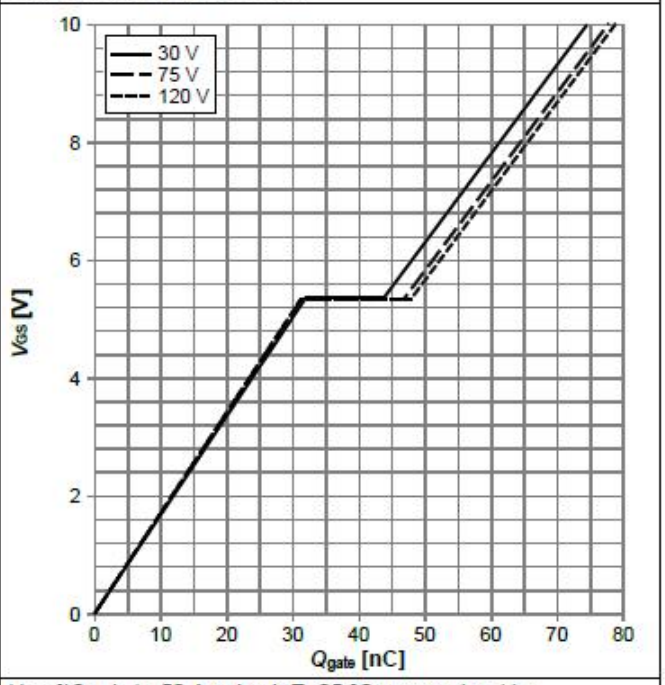
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



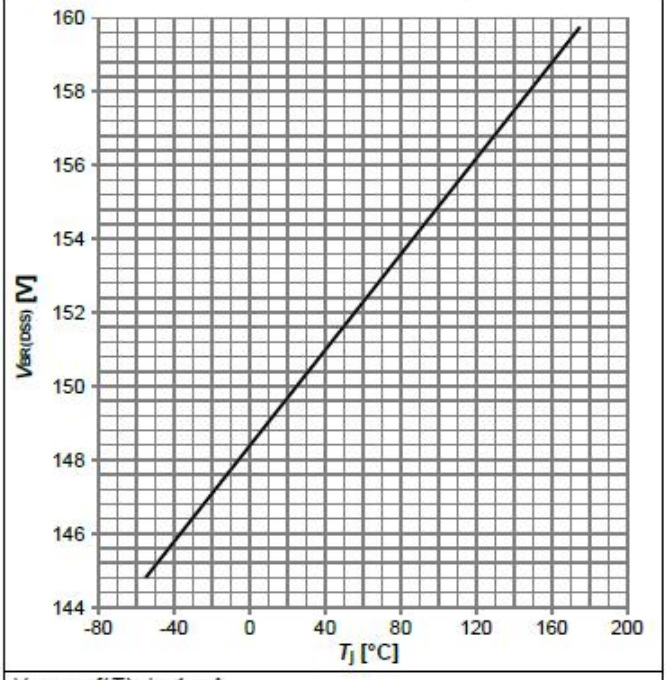
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

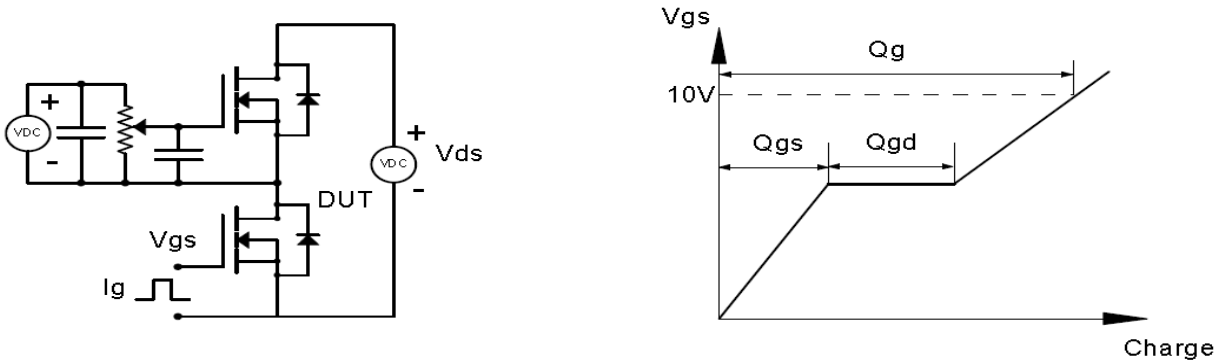
Diagram 15: Drain-source breakdown voltage



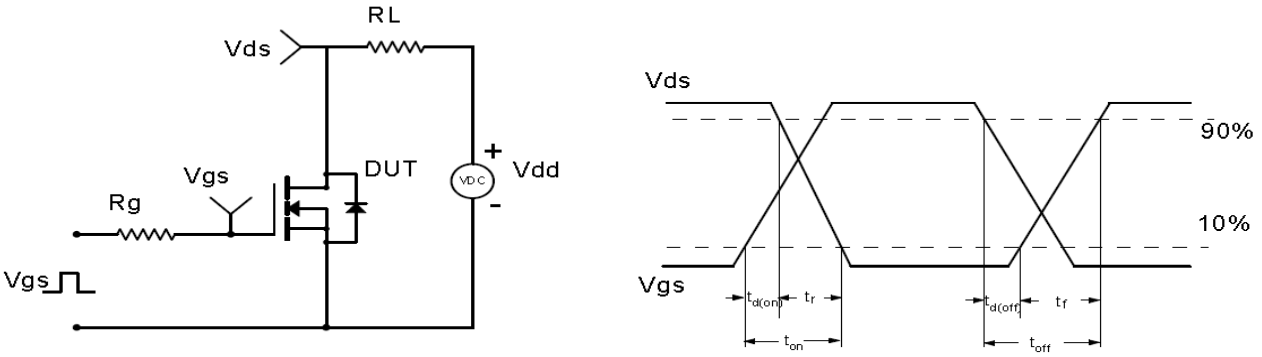
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Test Circuit & Waveform

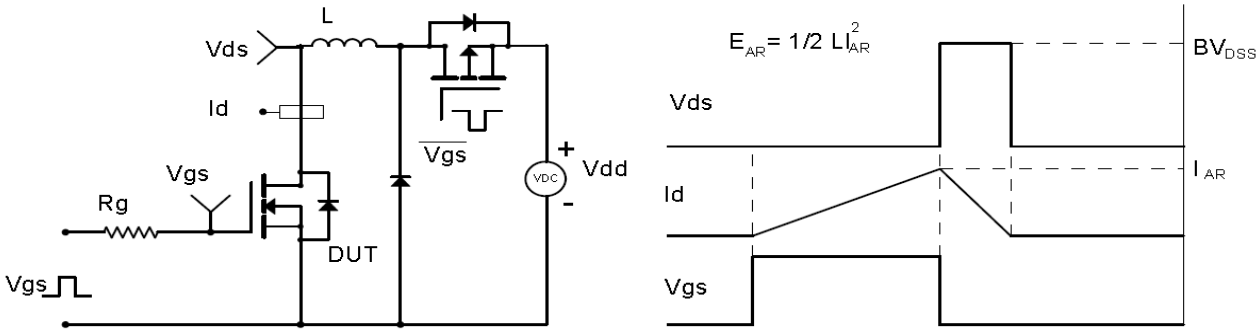
Gate Charge Test Circuit & Waveform



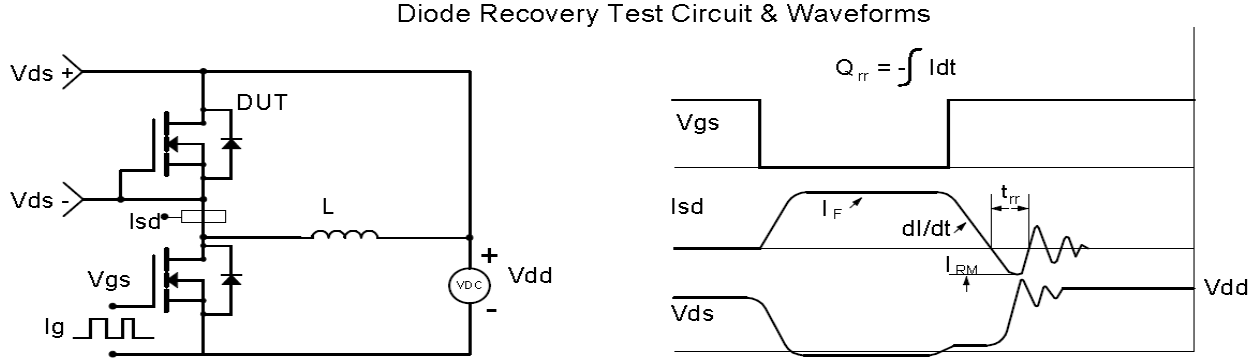
Resistive Switching Test Circuit & Waveforms



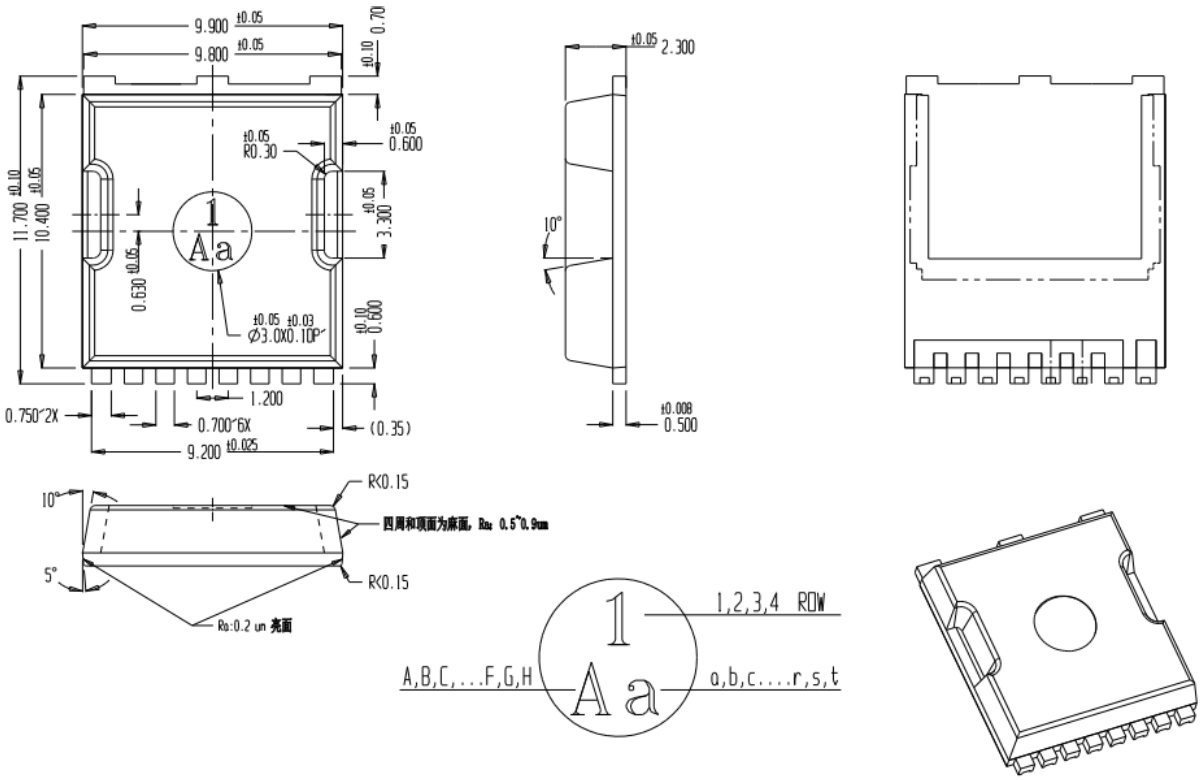
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Outline: TOLL



Revision History

Revision	Date	Major Changes
1.0	2023-12-10	Release of formal version

Disclaimer

Unless otherwise specified in the datasheet, the product is designed and qulified as a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability, such as automotive, aviation/aerospace and life-support devices or systems.

Any and all semicondutor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

Scilicon Electric reserves the right to improve product design,function and reliability without notice.