XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

HC32F052 Series

32-bit ARM® Cortex®-M0+ Microcontroller

Datasheet

Rev1.0 November 2023

Features

- **64MHz Cortex-M0+ 32-bit CPU platform**
- **HC32F052 series has a flexible power management system**
  - 20 μA @ 3 V Deep-sleep mode: all clocks off, power-on reset active, IO state retention, IO interrupt active, all registers, RAM and CPU data save state power consumption
  - 40 μA/ MHz @3 V @64 MHz operating mode: CPU running, running program from FLASH
  - 4 μs wake-up time makes mode switching more flexible and efficient, and the system reacts more quickly
- **128 K/ 64 K bytes Flash memory, with erase and write protection function**
- **16K bytes RAM memory with parity check to enhance system stability**
- **General purpose I/O leg (40 IO/ 48 pin, 26 IO/ 32 pin, 23 IO/ 28 pin)**
- **Clock, crystal**
  - External high-speed crystal oscillator 8 ~ 24 MHz
  - External low-speed crystal 32.768 kHz
  - Internal high-speed clock 12 MHz
  - Internal low-speed clock32.8/ 38.4 kHz
  - PLL clock up to 64 MHz
  - Hardware supports internal and external clock calibration and monitoring
- **Timer/counter**
  - 2 composite 16-bit timers/counters
  - 4 high-performance 16-bit timers/counters
  - 1 low-power 16 -bit timer / counter
  - 1 independent WDT, using 32K oscillator to provide WDT counting
  - 1 window WDT, counting using system clock
- **Communication Interface**
  - 2-channel USART standard communication interface
  - 2-channel LPUART low power communication interface, can work in deep sleep mode
  - 2-channel SPI standard communication interface
  - 2-channel I2C standard communication interface
  - 1 channel I2C Slave communication interface
  - 1 way CAN communication interface
- **Timer as buzzer frequency generator**
- **Hardware perpetual calendar RTC module**
- **Hardware CRC-16/ 32 module**
- **Hardware 32-bit square divider**
- **Globally unique 10-byte ID number**
- **Integrate a 12-bit 1 Msps sampling high-speed and high-precision SARADC with built-in follower to measure weak external signals**
- **Integrated high-precision temperature sensor**
- **2 -way voltage comparator with integrated 64 -level voltage programmable reference input**
- **Integrated low voltage detector LVD, configurable 16-level comparison level, can monitor port voltage and power supply voltage**
- **Integrated 2 op amps**
- **SWD debugging solution, providing a full-featured debugger**
- **Working conditions: -40 ~ 85 °C, 2.0 ~ 5.5V**
- **Package type: LQFP48/32, QFN48/32**

Support Model

HC32F052FAUA-QFN32TR	HC32F052JAUA-QFN48TR
HC32F052JATA-LQ48	HC32F052FATA-LQ32
HC32F052F8UA-QFN32TR	HC32F052J8UA-QFN48TR
HC32F052J8TA-LQ48	HC32F052F8TA-LQ32

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1 Introduction

HC32F052 has a main frequency of 64 MHz, a maximum Flash capacity of 128 KB, and rich digital and analog peripherals. It is an MCU with a wide voltage operating range.

This product integrates USART (compatible with LIN), SPI, I2C, CAN and other rich communication peripherals. It has the characteristics of high anti-interference and high reliability, and can be widely used in the general MCU market.

This product integrates a 12-bit high-precision SAR ADC, 2 OPAs, and 2 comparators. Together with the hardware division square root unit and a high-performance motor-specific PWM timer, it can implement complex high-performance, high-reliability motor control solutions. .

The core of this product adopts the Cortex-M0+ core, cooperates with mature Keil & IAR debugging and development software, supports C language, assembly language, and assembly instructions.

Typical Application

- Internet of Things
- Home appliance master control
- motor control
- smart home
- medical equipment

32-bit CORTEX M0+ core

The ARM® Cortex®-M0+ processor is derived from Cortex-M0 and includes a 32-bit RISC processor with a computing power of 0.95 Dhrystone MIPS/MHz. At the same time, a number of new designs have been added to improve debugging and tracing capabilities, reduce the number of each instruction cycle (IPC) and improve the two-stage pipeline for Flash access, and incorporate energy-saving and consumption-reducing technologies. The Cortex-M0+ processor fully supports the integrated Keil & IAR debugger.

Cortex-M0+ includes a hardware debugging circuit that supports 2-pin SWD debugging interface.

ARM Cortex-M0+ features:

Instruction Set	Thumb / Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark / MHz
Performance efficiency	0.95 DMIPS / MHz in Dhrystone
Interrupt	32 fast interrupts
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Single-cycle 32-bit multiplier
Debugging	Serial-wire debug port, supports 4 hard interrupts (break points) and 2 watch points (watch points)

128 K/ 64 K Byte Flash

The built-in fully integrated Flash controller does not require external high voltage input, and the high voltage is generated by the fully built-in circuit for programming. Support ISP, IAP, ICP functions.

16 K Byte RAM

According to different ultra-low power modes selected by customers, RAM data will be retained. With hardware parity bit, in case the data is accidentally damaged, when the data is read, the hardware circuit will immediately generate an interrupt to ensure the reliability of the system.

Clock system

A high-precision internal clock RCH with a frequency of 12 M. Calibration values are preset at the factory.

An external crystal oscillator XTH with a frequency of 8-24 MHz.

An external crystal oscillator XTL with a frequency of 32.768 kHz mainly provides the RTC real-time clock.

An internal clock RCL with a frequency of 32.768/ 38.4 kHz.

A PLL with 12-64 MHz output frequency.

Operating mode

1) Running mode Active: CPU running, peripheral function modules running.
2) Sleep mode Sleep: The CPU stops running, and the peripheral function modules run.
3) Deep sleep mode Deep sleep: The CPU stops running, the high-speed clock stops, and the low-power function modules run.

Real Time Clock RTC

RTC (Real Time Counter) is a register that supports BCD data. It uses a 32.768kHz crystal oscillator as its clock to realize the perpetual calendar function. The interrupt cycle can be configured as year/month/day/hour/minute/second. 24/12 hour time mode, the hardware automatically corrects leap years. With accuracy compensation function, the highest accuracy is 0.96 ppm. Internal temperature sensor or external temperature sensor can be used for accuracy compensation, software +1/-1 can be used to adjust year/month/day/hour/minute/second, and the minimum adjustable accuracy is 1 second.

The RTC calendar recorder used to indicate time and date does not reset the register when the MCU is reset by external factors.

Port controller GPIO

It can provide up to 40 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by independent control register bits and supports FAST IO. Supports edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU to working mode from various ultra-low power consumption modes. Support position, clear, and clear operations. Support Push-Pull CMOS push-pull output, Open-Drain open-drain output. Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input filter function. The output drive capability is configurable, and the maximum current drive capability is 18mA. 40 general-purpose IOs can support external asynchronous interrupts.

Interrupt Controller NVIC

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs; it has four interrupt priority levels, can handle complex logic, and can perform real-time control and interrupt processing.

Reset controller RESET

This product has 7 reset signal sources, each reset signal can make the CPU run again, most of the registers will be reset again, and the program counter PC will point to the starting address.

DMA controller DMAC

The DMAC (Direct Memory Access Controller) function block can transmit data at high speed without passing through the CPU. Using DMAC can improve system performance.

Timer TIM

Types of	Name	Bit width	Prescaler	Counting direction	PWM	capture	Complementary output
Advanced timer	ATIM0/1/2	16/32	1/2/4/8/16 32/64/256	Up count/ Count down/ Up and down count	2	2	1
	ATIM3	16/32	1/2/4/8/16/ 32/64/256	Up count/ Count down/ Up and down count	6	6	3
Composite timer	CTIM0/1	16	1~32768	Up count	4	4	No

The composite timer CTIM can be configured as a timer that supports 4-way comparison capture function, or it can be configured as 3 basic timers. The basic timer is a timer with only timing and counting functions.

The advanced timer includes two timers ATIM0/ 1/ 2/ 3, whose characteristics are as follows:

- PWM independent output, complementary output
- Capture input
- Dead zone control
- Brake control
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output
- Quadrature code counting function
- Single pulse mode
- External counting function

ATIM0/1/2 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reloading function, or as a 32-bit timer/counter without reloading function. ATIM0/1/2 has 2- way capture compare function, which can generate 2- way PWM independent output or 1 group of PWM complementary output. With dead zone control function.

ATIM3 is a multi-channel general-purpose timer with all the functions of ATIM0. It can generate 3 sets of complementary PWM outputs or 6 independent PWM outputs, and up to 6 input captures. With dead zone control function.

The low-power timer LPTIM is an asynchronous 16-bit timer/counter. After the system clock is turned off, it can still clock/count through the internal low-speed RC or external low-speed crystal oscillator. Wake up the system in low-power mode through interrupts.

Watchdog WDT

IWDT is a configurable 12- bit timer that provides reset when MCU is abnormal; built-in RCL (32kHz/38.4kHz) low-speed clock input as counter clock. In debug mode, you can choose to pause or continue to run; IWDT can only be restarted by writing a specific sequence.

WWDT is a 7 -bit timer. When external interference or unforeseen logic conditions cause the application program to deviate from the normal running sequence, WWDT can detect such software failures and generate interrupts or resets.

Universal synchronous asynchronous transceiver USART0~USART1

2-way Universal Synchronous Asynchronous Receiver/Transmitter, USART.

Its basic functions are as follows:

- Support full--duplex asynchronous communication, full-duplex clock synchronous communication
- Support multi-machine communication
- Support smart card 7816 interface communication
- Supports two infrared modes, 3/16 and 38 K modulation
- LIN support
- Built-in double buffers for full-duplex communication
- Data length: 8 bits/9 bits
- Stop bit: 1 bit/2 bits
- Data order: LSB/MSB shifted first
- Supports frame error, check error, overflow error, receiving data full, sending data empty, sending completed, timeout interrupt
- Support decimal frequency division
- Supports configurable 8x or 16x oversampling, providing the possibility for flexible configuration of speed tolerance and clock tolerance
- Support single-wire half-duplex communication
- DMA support

- Supports TX/RX pin configuration exchangeable
- Support modem hardware flow control
- Support timeout function

Low power synchronous asynchronous transceiver LPUART0~LPUART1

2-channel synchronous asynchronous transceiver (Low Power Universal Asynchronous Receiver/Transmitter) that can work in low power consumption mode, LPUART0/LPUART1.

Basic functions of LPUART:

- Transmission clock SCLK (SCLK can choose XTL, RCL and PCLK)
- Send and receive data in system low power mode
- Half-duplex and full-duplex transmission
- 8/9-Bit transmission data length
- Hardware parity
- 1/1.5/2-Bit stop bit
- Four different transmission modes
- 16-Bit baud rate counter
- Multi-machine communication
- Hardware address recognition
- DMAC hardware transmission handshake
- Hardware flow control

Serial Peripheral Interface SPI

2-channel synchronous serial interface (Serial Peripheral Interface).

Basic characteristics of SPI:

- Can be configured as master or slave, support multi-machine mode
- The maximum frequency division factor of the host mode is PCLK/2, and the maximum communication rate is 20 Mbps
- The maximum frequency division factor of slave mode is PCLK/4, and the maximum communication rate is 16 Mbps
- Multiple communication modes: full-duplex, single-wire half-duplex, simplex
- Two transmission orders: send and receive MSB first or send and receive LSB first
- Various data frame lengths: 4 bit ~ 16 bit
- Two NSS methods: hardware control, software control
- Configurable serial clock polarity and phase
- DMA support

I2C bus

Two-way I2C, using serial synchronous clock, can realize data transmission between devices at different rates.

Basic characteristics of I2C:

- Support four working modes of master sending/receiving and slave sending/receiving
- Support standard (100 Kbps) / fast (400 Kbps) / high speed (1 Mbps) three working rates
- Support 7-bit addressing function
- Support noise filtering function
- Support broadcast address
- Support interrupt status query function

I2C slave module I2C SLV

The I2C slave interface is a 2-wire bidirectional serial bus compatible with the I2C 3.0 bus specification. In high-speed mode, the transmission rate can reach 3.4 Mbps.

- Transmission rate: standard (~100 Kbps), fast (400 Kbps), ultra-fast (1 Mbps) and high speed (3.4 Mbps, the module working clock PCLK must not be less than 24 MHz)
- Only supports slave mode
- Supports clock low-level extension function to interface with faster hosts
- Supports 7-bit slave address and 10-bit slave address
- Support 4 slave addresses
- Support SCL low level timeout
- Support Device ID reading

Clock calibration CTRIM

The clock calibration timer can adjust and calibrate the RC clock frequency, and can also adjust and calibrate the clock frequencies of other RC oscillations. It can also be used as a general timer or an automatic wake-up timer. When RCH real-time calibration is enabled and a precise reference clock exists in the system, the RCH's full working range accuracy can reach 1%.

Device electronic signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information and chip coordinate information. UID Address: 0X0010 1F74 - 0X0010 1F7D.

Cyclic Redundancy Check (CRC)

CRC16 conforms to the polynomial given in ISO/IEC13239 =$X^{16} + X^{12} + X^5 + 1$

CRC32 conforms to the polynomial given in ISO/IEC13239 = $x^{32}+ x^{26}+ x^{23}+ x^{22}+ x^{16}+ x^{12}+ x^{11}+ x^{10}+ x^8 + x^7 + x^5 + x^4+ x^2 + x+ 1$

Analog-to-digital converter ADC

A 12-bit successive approximation analog-to-digital converter with monotonous and no missing codes, when working under a 16 MHz ADC clock, the sampling rate reaches 1 Msps. The reference voltage can be selected from the on-chip precision voltage (1.5 V or 2.5 V) or from an external input or power supply voltage. 19 input channels, including 16 external pin inputs, 1 internal temperature sensor voltage, 1 1/3 supply voltage, and 1 built-in BGR 1.2 V voltage. The built-in voltage follower can measure signals with high output impedance.

Basic characteristics of SAR ADC:

- 12-bit conversion accuracy
- 1 Msps conversion speed
- 4 reference sources: AVCC voltage, ExRef pin, built-in 1.5 V reference voltage, built-in 2.5 V reference voltage
- ADC voltage input range: 0~Vref
- Multiple conversion modes: single conversion, sequential scan single sequence conversion, sequential scan continuous conversion, sequential scan intermittent conversion, queue scanning continuous conversion, sequential scan single sequence conversion accumulation
- Input channel voltage threshold monitoring
- Software can configure ADC conversion rate
- Built-in voltage follower to measure signals with high output impedance
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion

Analog Voltage Comparator VC

Chip pin voltage monitoring / comparison circuit. 11 configurable positive external input channels, 11 configurable negative external input channels; 5 internal negative input channels, including 1 internal temperature sensor voltage, 1 reference voltage configured by the ADC module, and 1 built-in BGR 1.2 V voltage, 1 channel 64-step resistor voltage divider. An asynchronous interrupt can be generated according to the rising/falling edge to wake up the MCU from the low-power mode. Configurable software anti-shake function.

Low voltage detector LVD

Detect the chip power supply voltage or chip pin voltage. 16-shift voltage monitoring values. An asynchronous interrupt or reset can be generated based on the rising/falling edge. With hardware hysteresis circuit and configurable software anti-shake function.

LVD basic characteristics:

- 4 -channel monitoring sources, AVCC, PC13, PB08, PB07
- 16- step threshold voltage, optional
- 8 trigger conditions, combinations of high level, rising edge and falling edge
- 2 trigger results, reset and interrupt
- 8-stage filter configuration to prevent false triggering
- With hysteresis function, strong anti-interference

Operational Amplifier OPA

OPA module can be flexibly configured and is suitable for simple filter and buffer applications.

Extended arithmetic unit EAU

The extended arithmetic unit EAU (Extended Arithmetical Unit) is a coprocessor designed specifically for arithmetic operations. It can efficiently perform signed integer division, unsigned integer division and integer square root operations. It is an effective supplement to the arithmetic instructions of the M0+ core. Extension.

- Supports the square root operation of 32-bit unsigned integers, and can obtain the square root and remainder.
- Supports 32-bit divided 32-bit signed/unsigned integer division operation, and can obtain the quotient and remainder
- Support unsigned division divide by zero flag
- Supports signed division divide-by-zero flag and overflow flag

Controller Area Network CAN

CAN (Controller Area Network) bus is a bus standard that can realize mutual communication between microprocessors or devices without a host.

- Fully support CAN2.0A/ CAN2.0B protocol
- Upward compatible with CAN-FD
- Support the highest communication baud rate 1 Mbit/s
- Support 1~1/256 baud rate prescaler, flexible configuration of baud rate.

- 10 receive buffers
  -FIFO mode
  -Errors or unreceived data will not overwrite stored messages
- 1 high priority main transmit buffer PTB
- 4 secondary transmit buffers STB
  -FIFO mode
  -priority arbitration
- 8 sets of independent filters
  -Support 11-bit standard ID and 29-bit extended ID
  -Programmable ID CODE bits and MASK bits
  -PTB/ STB support single sending mode
- Support silent mode
- Support loopback mode
- Supports capturing transmission error types and locating arbitration failure locations
- Programmable error warning value
- Support ISO11898-4 specified time trigger CAN and receive timestamp

Embedded debugging system

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development software. Support 4 hard breakpoints and multiple soft breakpoints.

Programming mode

Two programming modes are supported: online programming and offline programming.

Support two programming protocols: ISP protocol, SWD protocol.

ISP protocol programming interface: PA13, PA14.

SWD protocol programming interface: PA13, PA14.

When reset, BOOT0 (PD03) pin is high level, the chip works in ISP programming mode, and Flash can be programmed through ISP protocol.

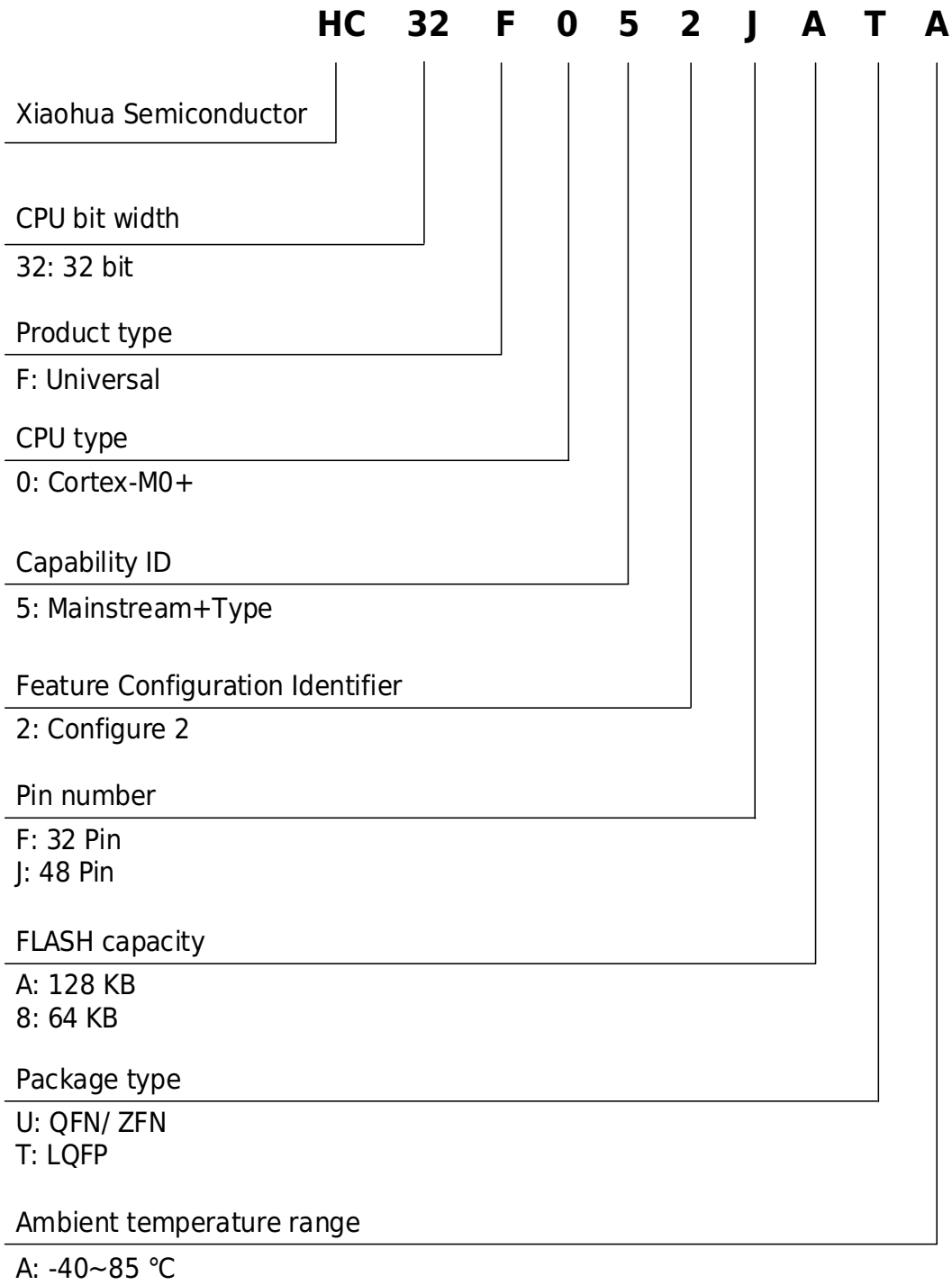
When reset, the BOOT0 (PD03) pin is low level, the chip works in user mode, the chip executes the program code in the Flash, and the Flash can be programmed through the SWD protocol.

High security

Encrypted embedded debugging solution, providing a full-featured real-time debugger.

2 Product lineup

2.1 Product name



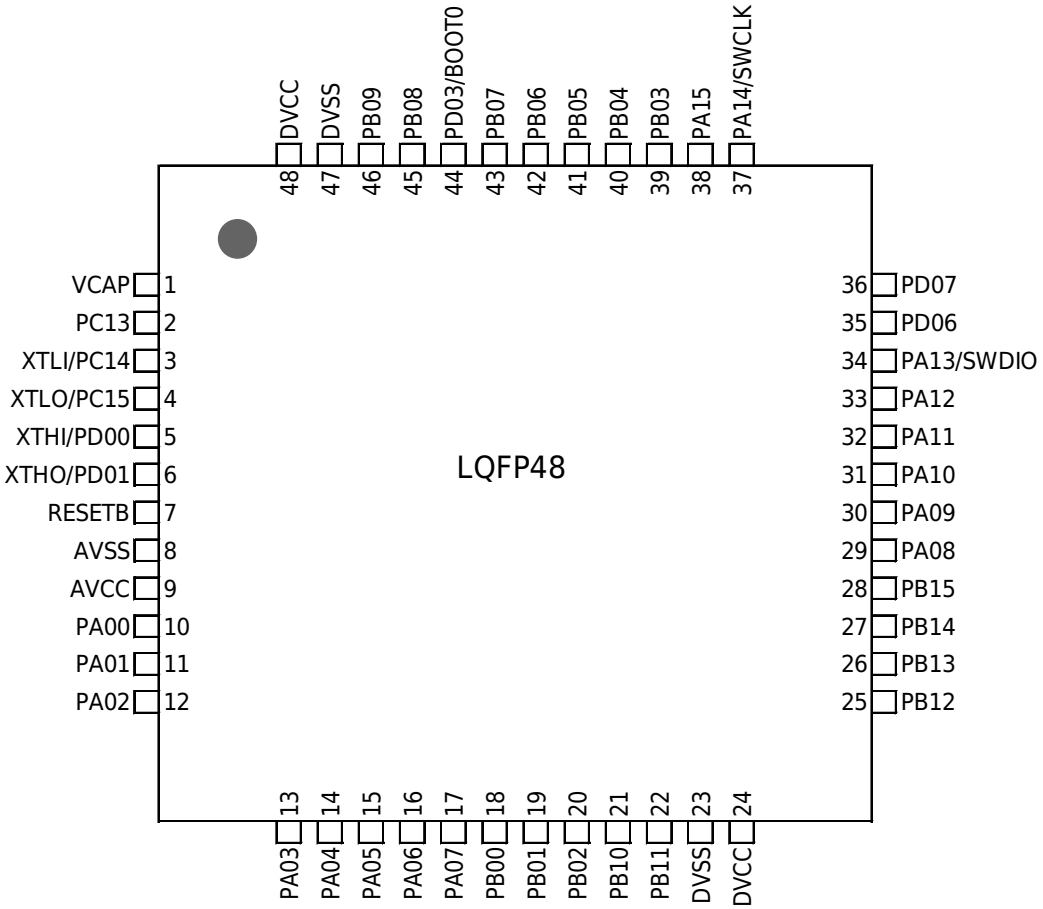
2.2 Function

Product Model		HC32F052 JATA	HC32F052 JAUA	HC32F052 FATA	HC32F052 FAUA	HC32F052 J8TA	HC32F052 J8UA	HC32F052 F8TA	HC32F052 F8UA
Pin number		48		32		48		32	
GPIO		40	40	26	26	40	40	26	26
CPU	Kernel	Cortex-M0+							
	Main frequency	64 MHz							
Flash (KB)		128				64			
RAM (KB)		16				16			
Operating Voltage (V)		2.0~5.5							
Working temperature (℃)		-40~85							
DMA		1*5 ch							
Timer		Low Power Timer LPTIM							
		Basic timer (multiplex) BTIM0/1/2/3/4/5							
		General-purpose timer GTIM0/1							
		Advanced Timer ATIM0/1/2/3							
Real Time Clock		RTC							
Communication Interface	LPUART	LPUART0/1		LPUART1		LPUART0/1		LPUART1	
	USART	USART0/1							
	LIN	Support							
	ISO7816	Support							
	infrared	Support							
	CAN	CAN 1 Unit							
	I2C	I2C 0/ 1							
	I2C SLV	I2C SLV 1Unit							

Product Model		HC32F052 JATA	HC32F052 JAUA	HC32F052 FATA	HC32F052 FAUA	HC32F052 J8TA	HC32F052 J8UA	HC32F052 F8TA	HC32F052 F8UA
	SPI	SPI0/1		SPI0		SPI0/1		SPI0	
Simulation	ADC (12 bit)	1*16 ch		1*10 ch		1*16 ch		1*10 ch	
	OPA	OPA0/1		not support		OPA0/1		not support	
	VC	VC0/ VC1							
	LVD	Support							
CRC		Support							
Extended Arithmetic Unit EAU		Support							

3 Pin configuration and function

3.1 Pin Configuration Diagram

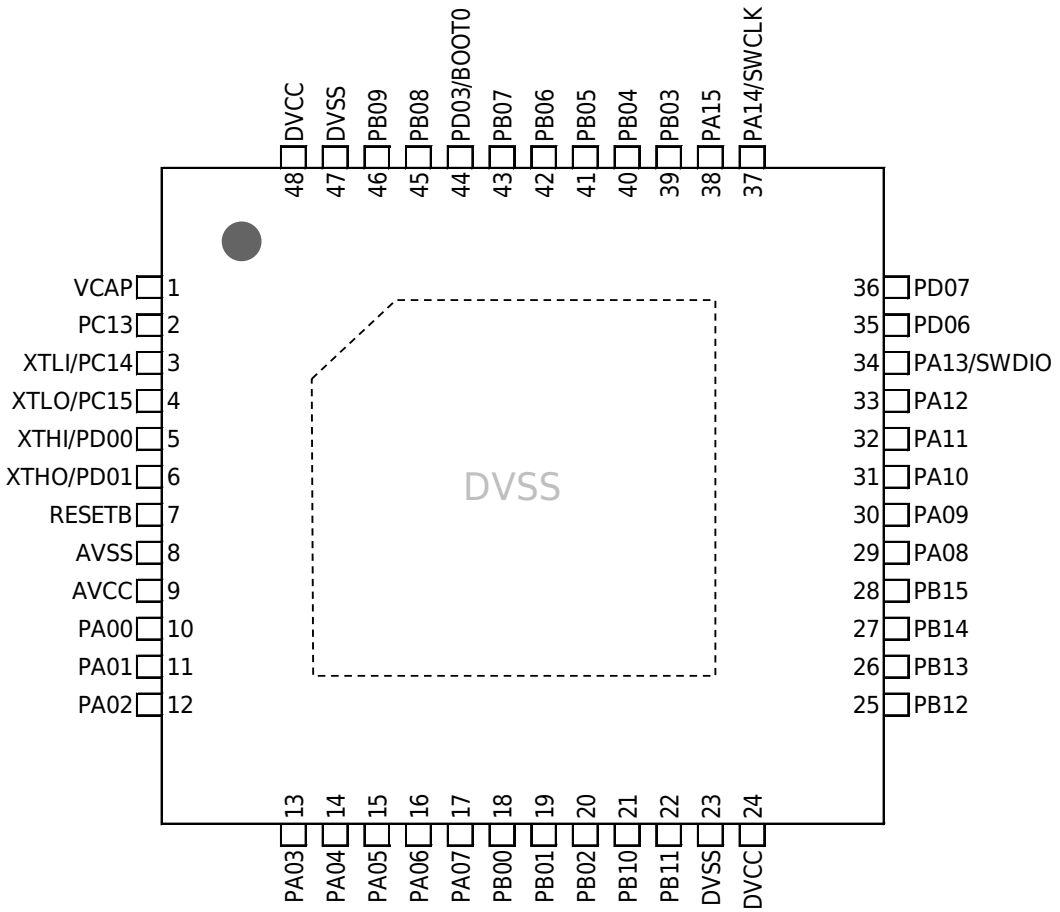


Note:

– *BOOT0 pin is used to control FLASH programming. See [Module signal description] for details.*

Figure 3-1 HC32F052JATA/ HC32F052J8TA pin configuration diagram

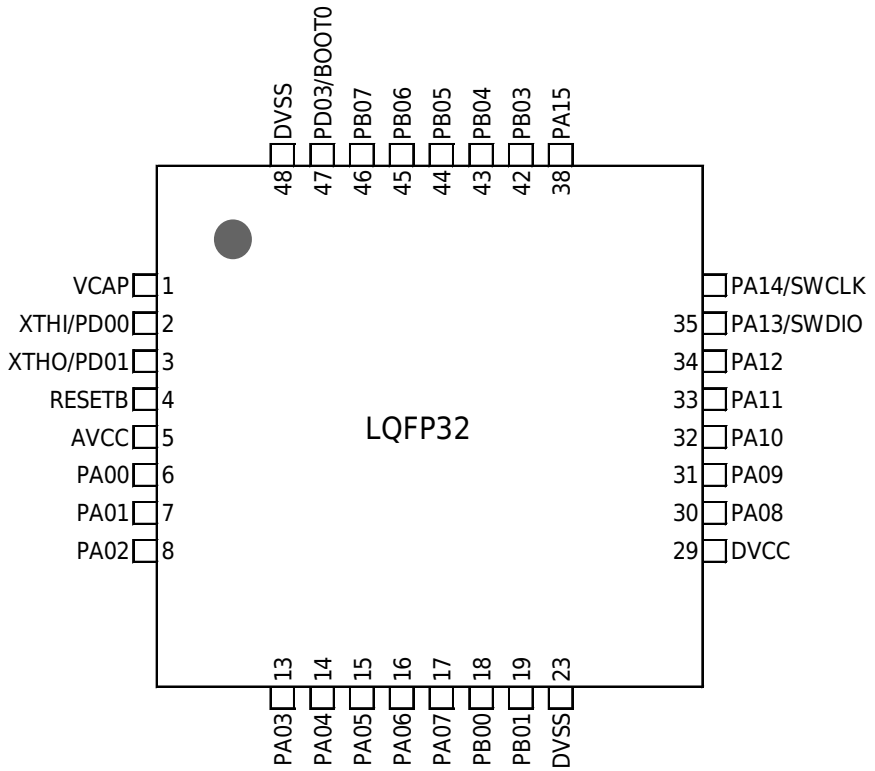
QFN48



Note:

- *BOOT0 pin is used to control FLASH programming. See [Module signal description] for details.*

Figure 3-2 HC32F052JAUA/ HC32F052J8UA pin configuration diagram

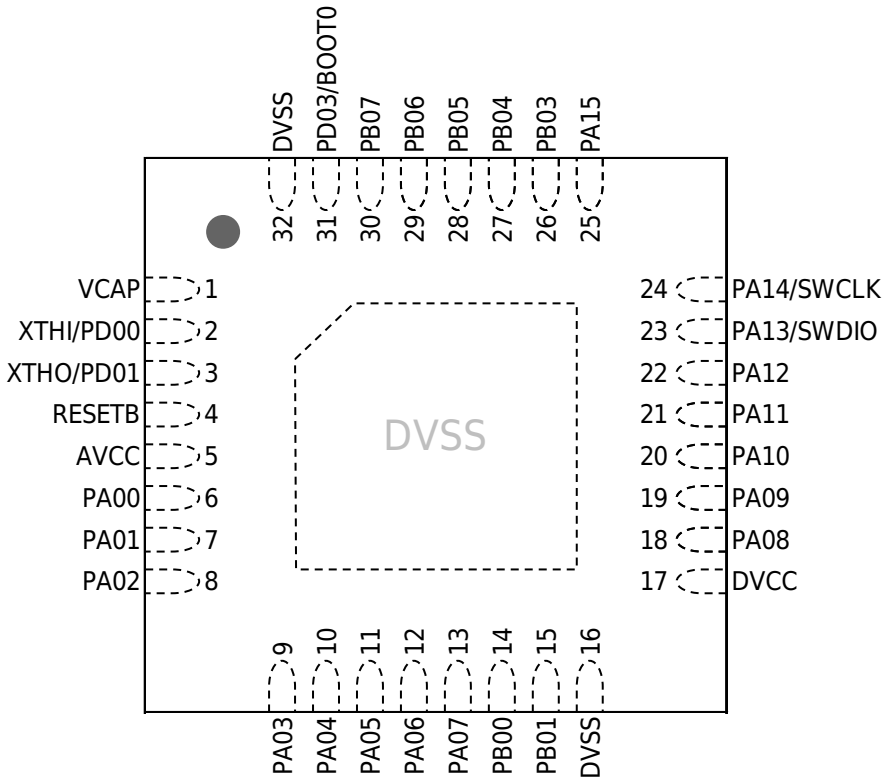


Note:

- *For details about the IOs not exported by this package, see [Pin function description] for details.*
- *BOOT0 pin is used to control FLASH programming. See [Module signal description] for details.*

Figure 3-3 HC32F052FATA/ HC32F052F8TA pin configuration diagram

QFN32



Note:

- *For details about the IOs not exported by this package, see [Pin function description] for details.*
- *BOOT0 pin is used to control FLASH programming. See [Module signal description] for details.*

Figure 3-4 HC32F052FAUA/ HC32F052F8UA pin configuration diagram

3.2 Pin function description

Table 3-1 Function description of each package pin

48 PINs	32 PINs	NAME	DIGITAL	ANALOG
1	1	VCAP	-	-
2	-	PC13	CTIM1_ETR RTC_1HZ ATIM3_CH1B CTIM0_TOG	LVDIN1
3	-	PC14	CTIM1_CH0 CTIM0_TOGN LVD_OUT	XTLI
4	-	PC15	CTIM1_CH0	XTLO
5	2	PD00	I2C0_SDA CTRIM_ETRTOG USART1_TXD CTIM1_CH2 I2CSLV_SCL	XTHI
6	3	PD01	I2C0_SCL ATIM3_CH0B USART1_RXD CTIM1_CH3 I2CSLV_SDA	XTHO
7	4	RESETB	-	-
8	-	AVSS	-	-
9	5	AVCC	-	-
10	6	PA00	USART1_CTS LPUART1_TXD ATIM0_ETR VC0_OUT ATIM1_CHA ATIM3_ETR ATIM0_CHA	AIN0 VCx_INN0 VCx_INP0
11	7	PA01	USART1_RTS LPUART1_RXD ATIM0_CHB ATIM1_ETR ATIM1_CHB HCLK_OUT SPI1_MOSI	AIN1 VCx_INN1 VCx_INP1
12	8	PA02	USART1_TXD ATIM0_CHA VC1_OUT ATIM1_CHA ATIM2_CHA ATIM3_CH0A SPI1_MISO	AIN2 VCx_INN2 VCx_INP2
13	9	PA03	USART1_RXD ATIM0_GATE ATIM1_CHB ATIM2_CHB SPI1_NSS ATIM3_CH0B PCLK_OUT	AIN3 VCx_INN3 VCx_INP3
14	10	PA04	SPI0_NSS	AIN4

48 PINs	32 PINs	NAME	DIGITAL	ANALOG
			USART1_SCK CTIM1_CH0 ATIM2_ETR ATIM3_CH1A USART1_TXD I2CSLV_SCL	VCx_INN4 VCx_INP4
15	11	PA05	SPI0_SCK ATIM0_ETR CTIM0_ETR ATIM0_CHA ATIM3_CH1B XTL_OUT XTH_OUT	AIN5 VCx_INN5 VCx_INP5
16	12	PA06	SPI0_MISO CTIM0_CH0 ATIM3_BK ATIM1_CHA VC0_OUT ATIM3_GATE LPUART0_CTS	AIN6
17	13	PA07	SPI0_MOSI CTIM0_CH1 HCLK_OUT ATIM3_CH2A ATIM2_CHA VC1_OUT CTIM1_TOG	AIN7
18	14	PB00	CTIM0_CH2 CTIM1_TOGN LPUART0_TXD ATIM3_CH2B RCH_OUT RCL_OUT PLL_OUT	AIN8 VCx_INN6 VCx_INP6
19	15	PB01	CTIM0_CH3 PCLK_OUT I2CSLV_SDA ATIM3_CH1B LPUART0_RTS LPTIM_TOGN USART0_SCK	AIN9/EXVREF VCx_INN7 VCx_INP7
20	-	PB02	LPTIM_TOG CTIM0_ETR LPUART1_TXD ATIM3_CH0B ATIM1_BK ATIM0_BK ATIM2_BK	AIN10 OP2_INN
21	-	PB10	I2C1_SCL SPI1_SCK ATIM1_CHA LPUART0_TXD ATIM3_CH2A LPUART1_RTS USART1_RTS	AIN11 OP2_INP
22	-	PB11	I2C1_SDA ATIM1_CHB LPUART0_RXD ATIM2_GATE ATIM3_CH1A LPUART1_CTS	AIN12 OP2_OUT

48 PINs	32 PINs	NAME	DIGITAL	ANALOG
			USART1_CTS	
23	16	DVSS	-	-
24	17	DVCC	-	-
25	-	PB12	SPI1_NSS ATIM3_BK LPUART0_TXD ATIM0_BK LPUART0_RTS ATIM3_CH0A	AIN13 VCx_INN8 VCx_INP8 OP1_INN
26	-	PB13	SPI1_SCK I2C1_SCL ATIM3_CH0B LPUART0_CTS ATIM1_CHA ATIM1_GATE	AIN14 OP1_INP
27	-	PB14	SPI1_MISO I2C1_SDA ATIM3_CH1B ATIM0_CHA ATIM3_CH2A LPUART0_RTS ATIM1_BK	AIN15 OP1_OUT
28	-	PB15	SPI1_MOSI ATIM3_CH2B ATIM0_CHB ATIM0_GATE RTC_1HZ CTIM0_TOG LPUART1_RXD	-
29	18	PA08	USART0_SCK ATIM3_CH0A USART0_TXD CAN_STBY ATIM1_GATE CTIM0_TOGN ATIM3_BK	-
30	19	PA09	USART0_TXD ATIM3_CH1A ATIM0_BK I2C0_SCL MCO_OUT HCLK_OUT I2CSLV_SCL	-
31	20	PA10	USART0_RXD ATIM3_CH2A ATIM2_BK I2C0_SDA ATIM2_GATE PCLK_OUT I2CSLV_SDA	-
32	21	PA11	USART0_CTS ATIM3_GATE I2C1_SCL CAN_TX VC0_OUT SPI0_MISO ATIM3_CH1B	-

48 PINs	32 PINs	NAME	DIGITAL	ANALOG
33	22	PA12	USART0_RTS ATIM3_ETR I2C1_SDA CAN_RX VC1_OUT SPI0_MOSI CTIM1_ETR	-
34	23	PA13	USART1_SCK USART0_RXD LVD_OUT ATIM3_ETR RTC_1HZ CTIM1_CH1 CTRIM_ETRTOG	-
35	-	PD06	I2C1_SCL LPUART1_CTS USART0_CTS RTC_OUT ATIM3_BK CTIM1_CH2	-
36	-	PD07	I2C1_SDA LPUART1_RTS USART0_RTS RTC_TS ATIM3_ETR CTIM1_CH3	-
37	24	PA14	USART1_TXD USART0_TXD ATIM3_CH2A LVD_OUT RCH_OUT RCL_OUT PLL_OUT	-
38	25	PA15	SPI0_NSS USART1_RXD LPUART1_RTS ATIM0_ETR ATIM0_CHA ATIM3_CH1A CAN_STBY	-
39	26	PB03	SPI0_SCK ATIM0_CHB ATIM1_GATE ATIM3_CH0A LPTIM_GATE XTL_OUT XTH_OUT	-
40	27	PB04	SPI0_MISO CTIM0_CH0 ATIM2_BK USART0_CTS ATIM2_GATE ATIM3_CH0B LPTIM_ETR	VCx_INN9 VCx_INP9
41	28	PB05	SPI0_MOSI ATIM3_BK ATIM1_BK CTIM0_CH1 LPTIM_GATE CTRIM_ETRTOG USART0_RTS	VCx_INN10 VCx_INP10

48 PINs	32 PINs	NAME	DIGITAL	ANALOG
42	29	PB06	I2C0_SCL USART0_TXD ATIM1_CHB ATIM0_CHA LPTIM_ETR ATIM3_CH0A LPTIM_TOG	-
43	30	PB07	I2C0_SDA USART0_RXD ATIM2_CHB LPUART1_CTS ATIM0_CHB LPTIM_TOGN ATIM3_ETR	LVDIN3
44	31	PD03	BOOT0	-
45	-	PB08	I2C0_SCL ATIM1_CHA CAN_RX ATIM2_CHA ATIM0_GATE ATIM3_CH2A USART0_TXD	LVDIN2
46	-	PB09	I2C0_SDA USART0_SCK SPI1_NSS ATIM2_CHA CAN_TX ATIM2_CHB USART0_RXD	-
47	32	DVSS	-	-
48	-	DVCC	-	-

The digital function of each pin is controlled by the PSEL bit field, as shown in the table below.

Table 3-2 Pin digital function multiplexing

Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC13	CTIM1_ETR	RTC_1HZ	ATIM3_CH1B	CTIM0_TOG	-	-	-
PC14	CTIM1_CH0	CTIM0_TOGN	LVD_OUT	-	-	-	-
PC15	CTIM1_CH0	-	-	-	-	-	-
PD00	I2C0_SDA	CTRIM_ETRTOG	USART1_TXD	CTIM1_CH2	I2CSLV_SCL	-	-
PD01	I2C0_SCL	ATIM3_CH0B	USART1_RXD	CTIM1_CH3	I2CSLV_SDA	-	-
PA00	USART1_CTS	LPUART1_TXD	ATIM0_ETR	VC0_OUT	ATIM1_CHA	ATIM3_ETR	ATIM0_CHA
PA01	USART1_RTS	LPUART1_RXD	ATIM0_CHB	ATIM1_ETR	ATIM1_CHB	HCLK_OUT	SPI1_MOSI
PA02	USART1_TXD	ATIM0_CHA	VC1_OUT	ATIM1_CHA	ATIM2_CHA	ATIM3_CH0A	SPI1_MISO
PA03	USART1_RXD	ATIM0_GATE	ATIM1_CHB	ATIM2_CHB	SPI1_NSS	ATIM3_CH0B	PCLK_OUT
PA04	SPI0_NSS	USART1_SCK	CTIM1_CH0	ATIM2_ETR	ATIM3_CH1A	USART1_TXD	I2CSLV_SCL
PA05	SPI0_SCK	ATIM0_ETR	CTIM0_ETR	ATIM0_CHA	ATIM3_CH1B	XTL_OUT	XTH_OUT
PA06	SPI0_MISO	CTIM0_CH0	ATIM3_BK	ATIM1_CHA	VC0_OUT	ATIM3_GATE	LPUART0_CTS
PA07	SPI0_MOSI	CTIM0_CH1	HCLK_OUT	ATIM3_CH2A	ATIM2_CHA	VC1_OUT	CTIM1_TOG
PB00	CTIM0_CH2	CTIM1_TOGN	LPUART0_TXD	ATIM3_CH2B	RCH_OUT	RCL_OUT	PLL_OUT
PB01	CTIM0_CH3	PCLK_OUT	I2CSLV_SDA	ATIM3_CH1B	LPUART0_RTS	LPTIM_TOGN	USART0_SCK
PB02	LPTIM_TOG	CTIM0_ETR	LPUART1_TXD	ATIM3_CH0B	ATIM1_BK	ATIM0_BK	ATIM2_BK
PB10	I2C1_SCL	SPI1_SCK	ATIM1_CHA	LPUART0_TXD	ATIM3_CH2A	LPUART1_RTS	USART1_RTS
PB11	I2C1_SDA	ATIM1_CHB	LPUART0_RXD	ATIM2_GATE	ATIM3_CH1A	LPUART1_CTS	USART1_CTS
PB12	SPI1_NSS	ATIM3_BK	LPUART0_TXD	ATIM0_BK	-	LPUART0_RTS	ATIM3_CH0A
PB13	SPI1_SCK	I2C1_SCL	ATIM3_CH0B	LPUART0_CTS	ATIM1_CHA	ATIM1_GATE	-
PB14	SPI1_MISO	I2C1_SDA	ATIM3_CH1B	ATIM0_CHA	ATIM3_CH2A	LPUART0_RTS	ATIM1_BK
PB15	SPI1_MOSI	ATIM3_CH2B	ATIM0_CHB	ATIM0_GATE	RTC_1HZ	CTIM0_TOG	LPUART1_RXD
PA08	USART0_SCK	ATIM3_CH0A	USART0_TXD	CAN_STBY	ATIM1_GATE	CTIM0_TOGN	ATIM3_BK
PA09	USART0_TXD	ATIM3_CH1A	ATIM0_BK	I2C0_SCL	MCO_OUT	HCLK_OUT	I2CSLV_SCL
PA10	USART0_RXD	ATIM3_CH2A	ATIM2_BK	I2C0_SDA	ATIM2_GATE	PCLK_OUT	I2CSLV_SDA
PA11	USART0_CTS	ATIM3_GATE	I2C1_SCL	CAN_TX	VC0_OUT	SPI0_MISO	ATIM3_CH1B
PA12	USART0_RTS	ATIM3_ETR	I2C1_SDA	CAN_RX	VC1_OUT	SPI0_MOSI	CTIM1_ETR
PA13	USART1_SCK	USART0_RXD	LVD_OUT	ATIM3_ETR	RTC_1HZ	CTIM1_CH1	CTRIM_ETRTOG
PD06	I2C1_SCL	LPUART1_CTS	USART0_CTS	RTC_OUT	ATIM3_BK	CTIM1_CH2	-
PD07	I2C1_SDA	LPUART1_RTS	USART0_RTS	RTC_TS	ATIM3_ETR	CTIM1_CH3	-
PA14	USART1_TXD	USART0_TXD	ATIM3_CH2A	LVD_OUT	RCH_OUT	RCL_OUT	PLL_OUT
PA15	SPI0_NSS	USART1_RXD	LPUART1_RTS	ATIM0_ETR	ATIM0_CHA	ATIM3_CH1A	CAN_STBY
PB03	SPI0_SCK	ATIM0_CHB	ATIM1_GATE	ATIM3_CH0A	LPTIM_GATE	XTL_OUT	XTH_OUT
PB04	SPI0_MISO	CTIM0_CH0	ATIM2_BK	USART0_CTS	ATIM2_GATE	ATIM3_CH0B	LPTIM_ETR
PB05	SPI0_MOSI	ATIM3_BK	ATIM1_BK	CTIM0_CH1	LPTIM_GATE	CTRIM_ETRTOG	USART0_RTS
PB06	I2C0_SCL	USART0_TXD	ATIM1_CHB	ATIM0_CHA	LPTIM_ETR	ATIM3_CH0A	LPTIM_TOG

Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB07	I2C0_SDA	USART0_RXD	ATIM2_CHB	LPUART1_CTS	ATIM0_CHB	LPTIM_TOGN	ATIM3_ETR
PD03	-	-	-	-	-	-	-
PB08	I2C0_SCL	ATIM1_CHA	CAN_RX	ATIM2_CHA	ATIM0_GATE	ATIM3_CH2A	USART0_TXD
PB09	I2C0_SDA	USART0_SCK	SPI1_NSS	ATIM2_CHA	CAN_TX	ATIM2_CHB	USART0_RXD

3.3 Module signal description

Table 3-3 Module signal description

Modules	Pin name	Description
Power supply	DVCC	Digital power supply
	AVCC	Analog power
	DVSS	Digitally
	AVSS	Analog ground
	VCAP	LDO core power supply output (only for internal circuit use)
ISP	BOOT0	When reset, the BOOT0 (PD03) pin is high, the chip works in ISP programming mode, and FLASH can be programmed through the ISP protocol When reset, the BOOT0 (PD03) pin is low, the chip works in user mode, the chip executes the program code in the FLASH, and the FLASH can be programmed through the SWD protocol
ADC y=0 - 15	AINy	ADC input channel
	ADC_ExRef	ADC external reference voltage
VC x=0,1 y=0 - 7	VCx_INNy	VCx negative input
	VCx_INPy	VCx positive input
	VCx_OUT	VCx compare output
OPA x=0,1	OPx_INN	OPA negative input
	OPx_INP	OPA positive input
	OPx_OUT	OPA output
LVD y=0, 1, 2	LVD_INy	Voltage detection input
	LVD_OUT	Voltage detection output
USART	USART_TXD	USART data transmitter
	USART_RXD	USART data receiver
	USART_CTS	USART CTS
	USART_RTS	USART RTS
	USART_SCK	USART clock input and output
LPUART x=0,1	LPUARTx_TXD	LPUART data transmitter
	LPUARTx_RXD	LPUART data receiver
	LPUARTx_CTS	LPUART CTS
	LPUARTx_RTS	LPUART RTS
CTRIM	CTRIM_ETR/TOG	CTRIM external sync signal/toggle output signal
SPI x=0,1	SPIx_MISO	SPI module host input and slave output data signal
	SPIx_MOSI	SPI module master output slave input data signal
	SPIx_SCK	SPI module clock signal
	SPIx_NSS	SPI chip select
I2C x=0,1	I2Cx_SDA	I2C module data signal
	I2Cx_SCL	I2C module clock signal
I2CSLV	I2CSLV_SDA	I2CSLV module data signal

Modules	Pin name	Description
	I2CSLV_SCL	I2CSLV module clock signal
CAN	CAN_TX	CAN sending pin
	CAN_RX	CAN receiving pin
	CAN_STBY	CAN transceiver standby control pin
RTC	RTC_1Hz	RTC 1Hz output
	RTC_OUT	RTC interrupt flag output
	RTC_TS	RTC timestamp input
Composite timer CTIM x=0,1 y=0~3	GTIMx_CHy	GTIM capture input compare output/BTIM flip output signal
	GTIMx_ETR	GTIM's external counting input signal
	GTIMx_TOGP/TOGN	GTIM/BTIM flip output signal
Advanced timer ATIMx x=0,1,2	ATIMx_CHA	ATIM capture input compare output A
	ATIMx_CHB	ATIM capture input compare output B
	ATIMx_ETR	ATIM's external counting input signal
	ATIMx_BK	ATIM's external brake input signal
	ATIMx_GATE	ATIM gate control signal
Advanced timer ATIM3 y=0,1,2	ATIM3_CHyA	ATIM3 capture input compare output A
	ATIM3_CHyB	ATIM3 capture input compare output B
	ATIM3_ETR	ATIM3 external counting input signal
	ATIM3_BK	ATIM3 external brake input signal
	ATIM3_GATE	ATIM3 gate control signal

Note:

- *Most IO ports are reset to the analog input state, and sleep mode and deep sleep mode maintain the previous port state.*

4 Block diagram

Functional module

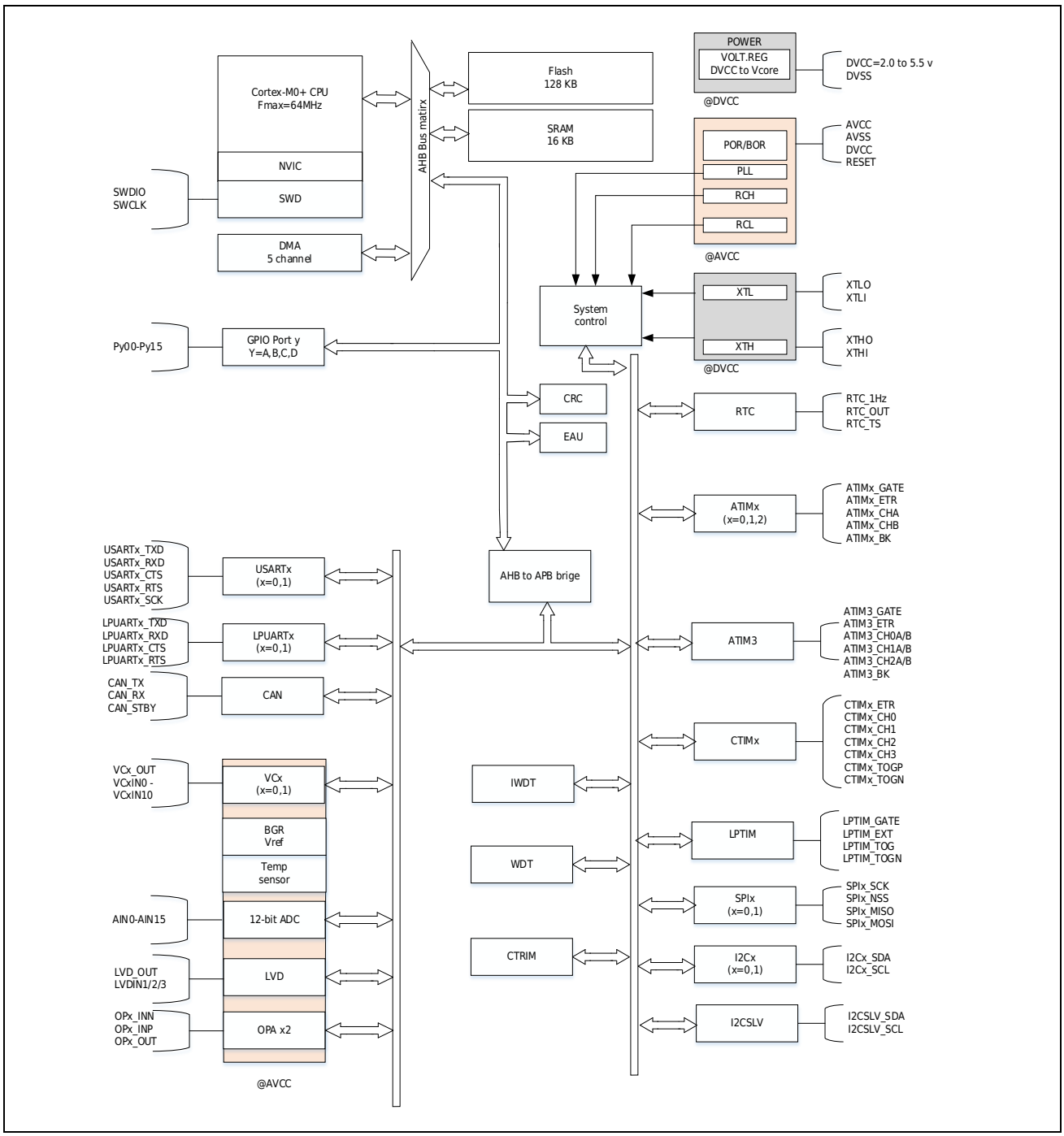


Figure 4-1 Functional module

5 Storage area map

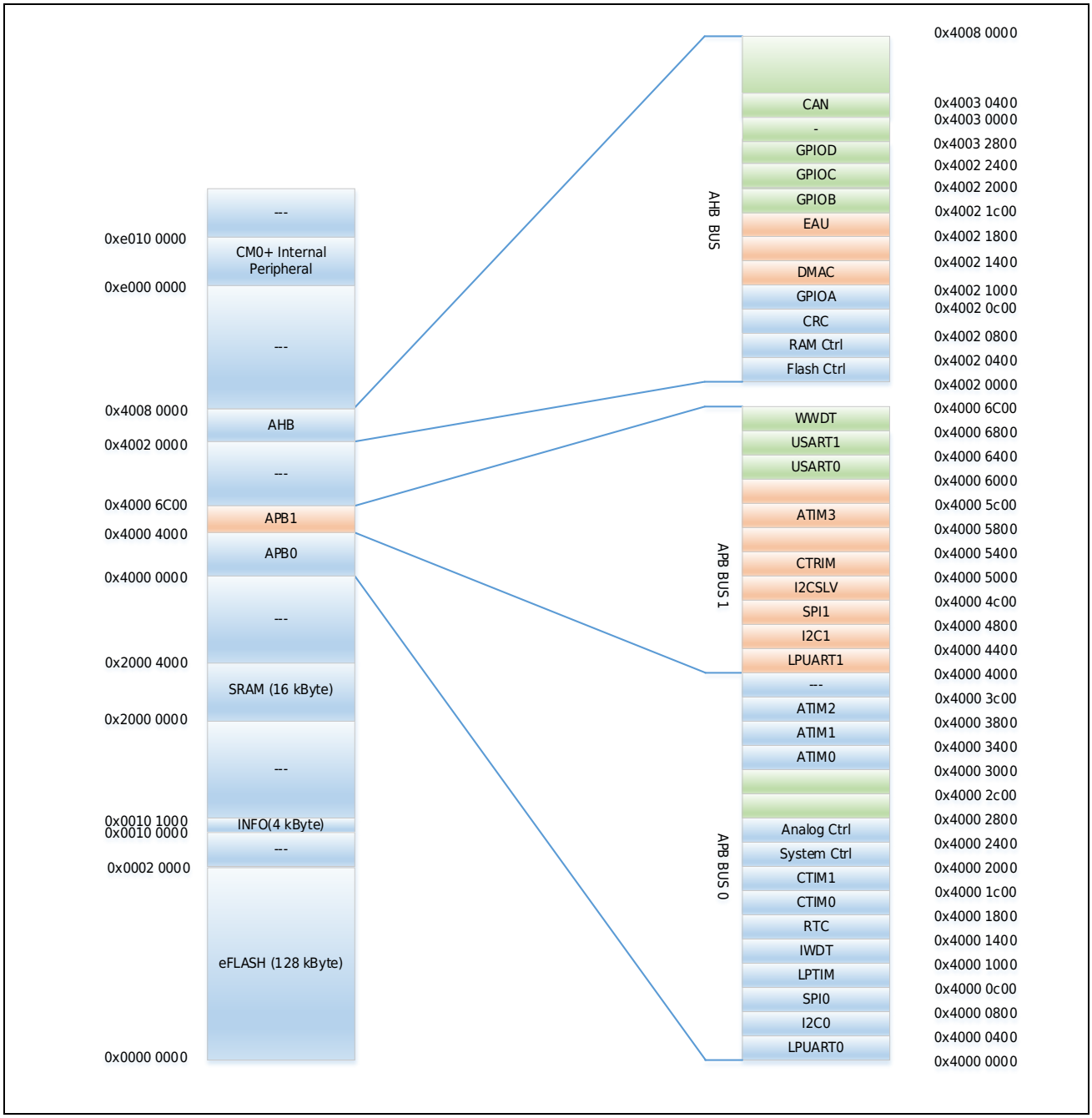


Figure 5-1 Module address mapping diagram

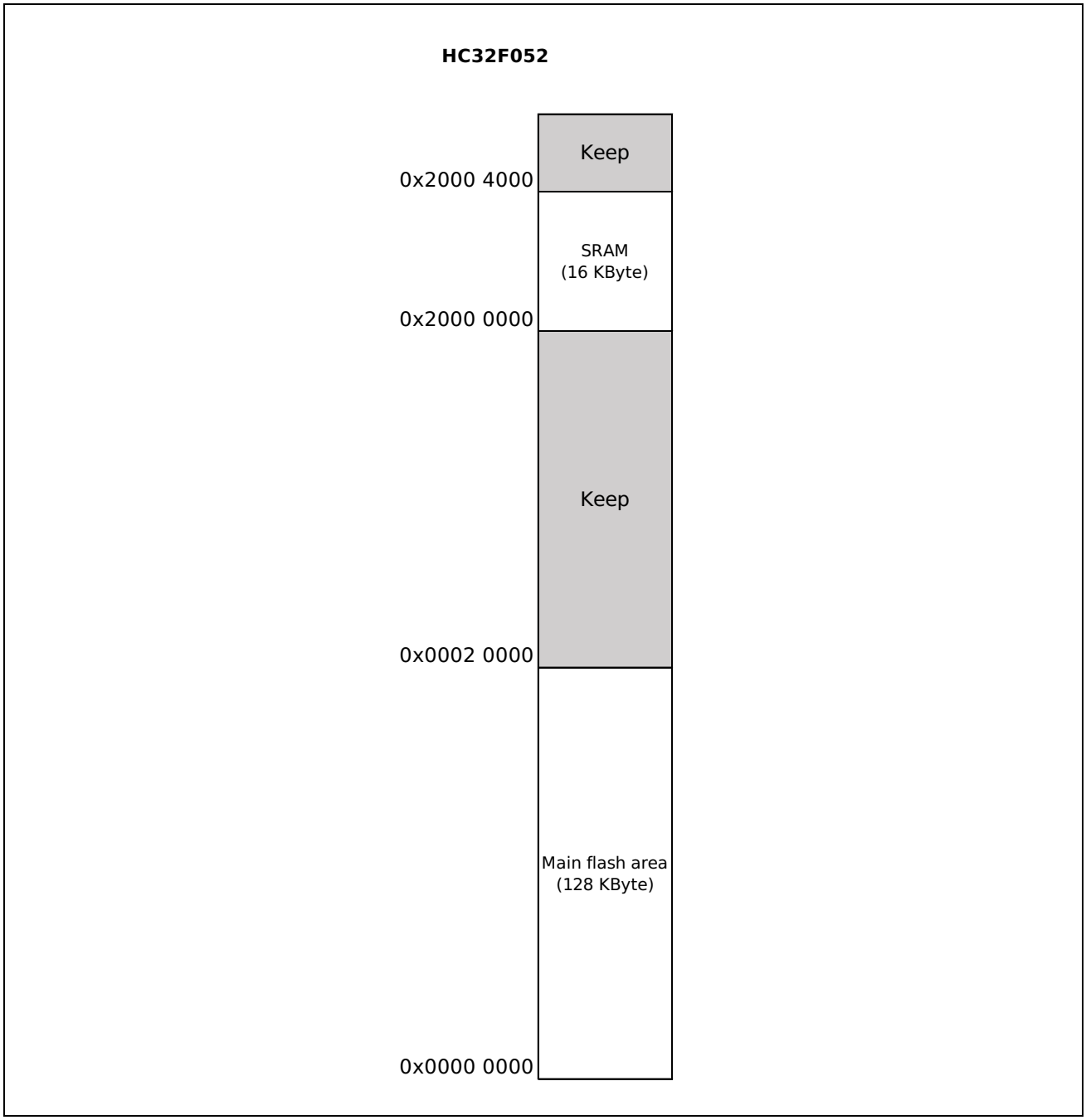


Figure 5-2 Storage map

6 Typical application circuit diagram

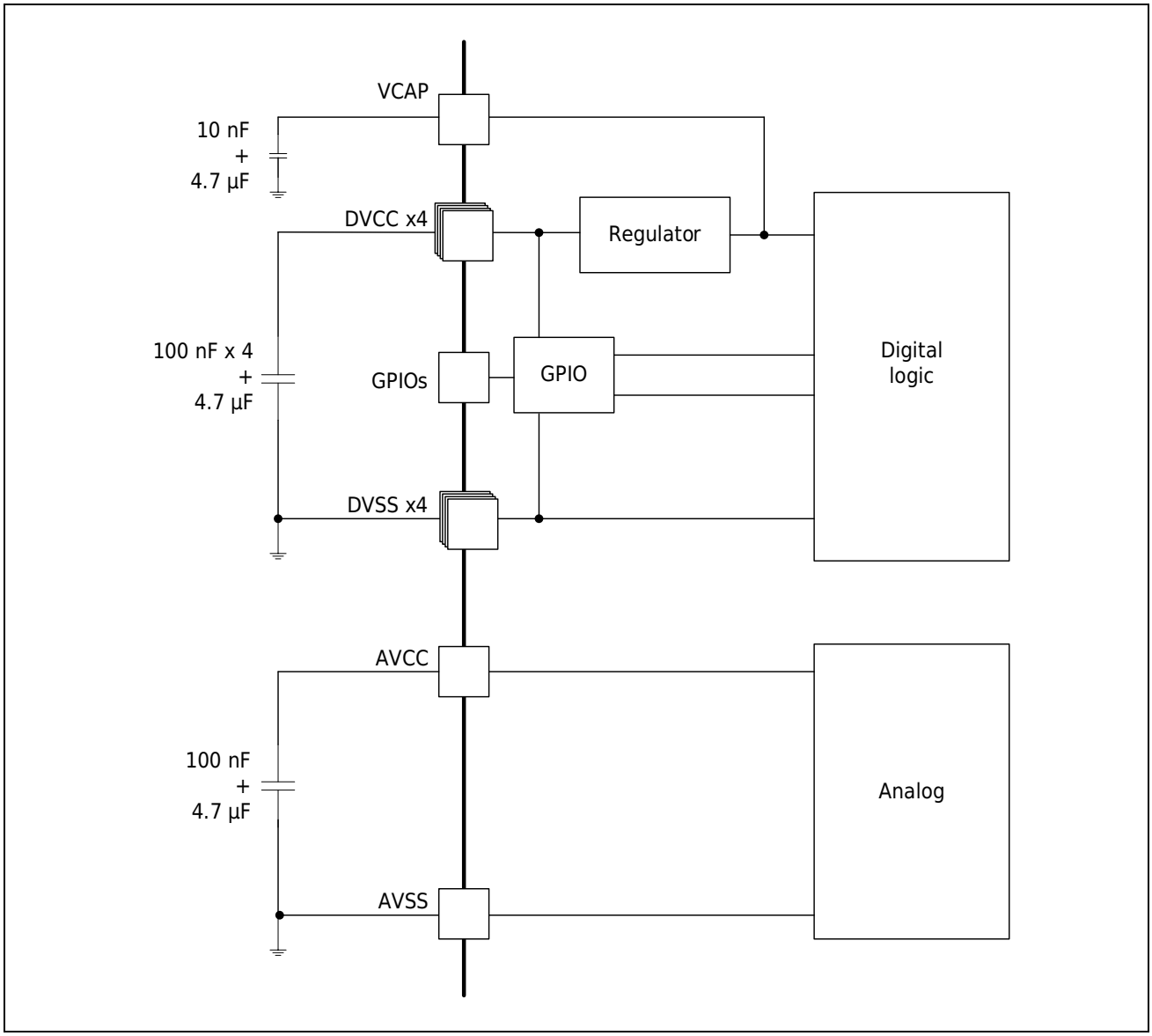


Figure 6-1 Typical application circuit diagram

Note:

- *AVCC and DVCC voltage must be the same.*
- *Each power supply requires a decoupling capacitor, and the decoupling capacitor should be as close as possible to the corresponding power pin.*

7 Electrical characteristics

7.1 Test Conditions

Unless otherwise stated, all voltages are referenced to VSS.

7.1.1 Minimum and maximum values

Unless otherwise specified, all minimum and maximum values will be in the worst environment through the test performed on 100% of the products in the production line at ambient temperature T_A=25 ℃ and T_A=T_A max ($T_A$max matches the selected temperature range) Guaranteed over temperature, supply voltage, and clock frequency.

The notes at the bottom of each table indicate data obtained through comprehensive evaluation, design simulation and/or process characteristics, and will not be tested on the production line; on the basis of comprehensive evaluation, the minimum and maximum values are after sample testing. Take the average value and add or subtract three times the standard distribution (mean ±3δ).

7.1.2 Typical value

Unless otherwise specified, typical data is based on T_A=25 ℃ and VCC=3.3 V (2.0 V ≤ VCC ≤ 5.5 V voltage range). These data are only used for design guidance and not tested.

7.2 Absolute maximum ratings

If the load on the device exceeds the value given in the "Absolute Maximum Ratings" list, it may cause permanent damage to the device. This only gives the maximum load that can be withstood, and does not mean that the functional operation of the device under this condition is correct. Long-term operation of the device under the maximum condition will affect the reliability of the device.

Table 7-1 Voltage Characteristics

Symbol	Description	Minimum Value	Maximum Value	Unit
VCC - VSS	External main supply voltage (includes AVCC and DVCC)(1)	-0.3	5.5	V
V_{IN}	Input voltage on other pins(2)	VSS-0.3	VCC + 0.3	V
| ΔVCCx |	Voltage difference between different power supply pins	-	50	mV
| VSSx - VSS |	Voltage difference between different ground pins	-	50	mV
V_{ESD}(HBM)	ESD electrostatic discharge voltage (human body model)	Refer to absolute maximum electrical parameters		V

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.
2. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When $V_{IN}>V_{CC}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current.

Table 7-2 Voltage Characteristics

Symbol	Description	Max (1)	Unit
I_{VCC}	The total current (supply current) through the DVCC/AVCC power cord (1)	100	mA
I_{VSS}	The total current through the VSS ground wire (outflow current) (1)	100	mA
I_{IO}	Output sink current on any I/O and control pin	18	mA
	Output current on any I/O and control pin	-18	mA
$I_{INJ(PIN)}$ (2) (3)	Injection current of RESETB pin	+/-5	mA
	Injection current of XTHI pin of XTH and XTLI pin of XTL	+/-5	mA
	Injection current of other pins (4)	+/-5	mA
$\sum I_{INJ(PIN)}$ (2)	Total injection current on all I/O and control pins (4)	+/-25	mA

1. All power (DVCC, AVCC) and ground (DVCC, AVCC) pins must always be connected to the external power supply system within the allowable range.
2. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When $V_{IN}>V_{CC}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.

4. When several I/O ports have injection current at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute value of the forward injection current and the reverse injection current. This result is based on the characteristics of the maximum $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 7-3 temperature characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-60 ~ + 150	℃
T_J	Maximum junction temperature	105	℃

7.3 Operating conditions

7.3.1 General working conditions

Table 7-4 General Operating Conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	64	MHz
f_{PCLK0}	Internal APB0 clock frequency	-	0	64	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	64	MHz
DVCC	Working voltage of digital part	-	2.0	5.5	V
AVCC(1)	Analog part working voltage	Must be the same as DVCC(2)	2.0	5.5	V
P_D	Power dissipation T_A=85℃	LQFP48	-	296	mW
	Power dissipation T_A=85℃	LQFP32	-	277	mW
	Power dissipation T_A=85℃	QFN48	-	740	mW
	Power dissipation T_A=85℃	QFN32	-	419	mW
T_A	Ambient temperature	Maximum power consumption	-40	85	℃
		Low power consumption (3)	-40	105	℃
T_J	Junction temperature range	-	-40	105	℃

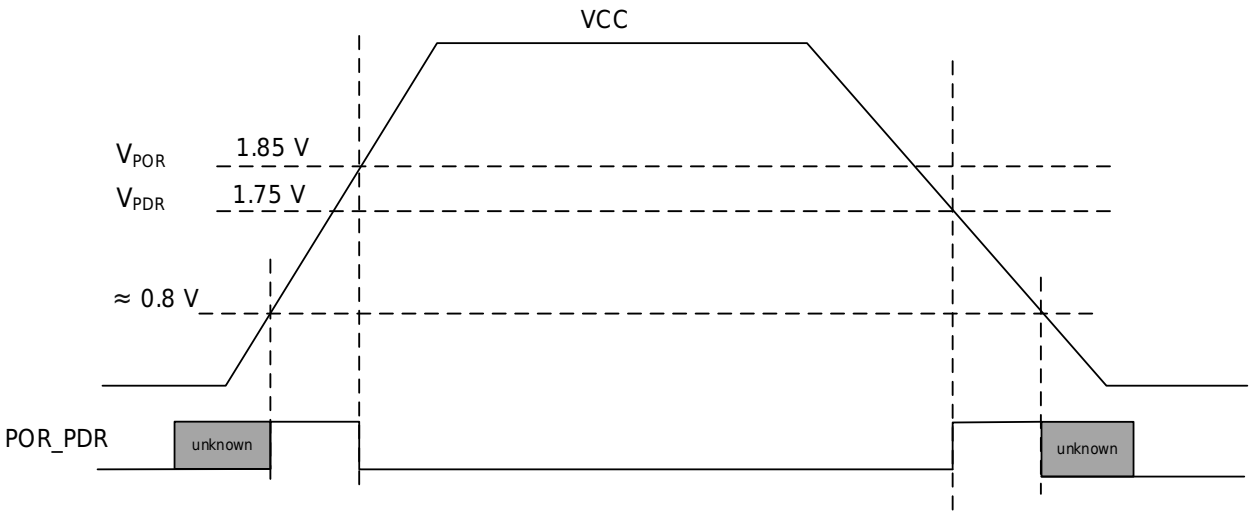
1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300mV difference between DVCC and AVCC during power-up and normal operation.
3. In a state of lower power dissipation, as long as T_J does not exceed T_{Jmax}, T_A can be extended to this range.

7.3.2 Working conditions at power-up and power-down

Table 7-5 Power-up and power-down operating conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{Vcc}	VCC rising rate	-	1	∞	μs/V
t_{Vcc}	VCC falling rate	-	10	∞	μs/V

7.3.3 Embedded reset and LVD module features



1. Guaranteed by design, not tested in production.

Figure 7-1 POR/Brown Out Diagram

Table 7-6 POR/Brown Out

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{POR}	POR release voltage (power-on process)	-	-	1.85	-	V
V_{PDR}	PDR detection voltage (power-down process)	-	-	1.75	-	V

Table 7-7 LVD module characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vex	External input voltage range	-	0	-	VCC	V
Vlevel	Detection threshold	LVD_CR.VTDS=0000 LVD_CR.VTDS=0001 LVD_CR.VTDS=0010 LVD_CR.VTDS=0011 LVD_CR.VTDS=0100 LVD_CR.VTDS=0101 LVD_CR.VTDS=0110 LVD_CR.VTDS=0111 LVD_CR.VTDS=1000 LVD_CR.VTDS=1001 LVD_CR.VTDS=1010 LVD_CR.VTDS=1011 LVD_CR.VTDS=1100 LVD_CR.VTDS=1101 LVD_CR.VTDS=1110 LVD_CR.VTDS=1111	1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2	1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3	1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4	V
Tresponse	Response time	Choose to detect the GPIO pin voltage, VCC=3.3V, LVD_CR.VTDS=1000, the detection voltage changes from (Vlevel+100mV) to (Vlevel-100mV), the change slope is$2\times10^5V/us$	-	28	-	μs
Tsetup	Establishment time	Choose to detect the GPIO pin voltage, VCC=3.3V, LVD_CR.VTDS=1000, the detection voltage is lower than Vlevel 100mV	-	50	-	μs
Vhyste	Hysteresis voltage	-	-	40	-	mV
Tfilter	Filter time	LVD_debounce = 000 LVD_debounce = 001 LVD_debounce = 010 LVD_debounce = 011 LVD_debounce = 100 LVD_debounce = 101 LVD_debounce = 110 LVD_debounce = 111	-	7 14 28 112 450 1800 7200 28800	-	μs

7.3.4 Built-in reference voltage

Table 7-8 Built-in reference voltage characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{REF25}	Internal 2.5V Reference Voltage	Room temperature 25°C 3.3V	2.475	2.5	2.525	V
V_{REF25}	Internal 2.5V Reference Voltage	-40~85°C 2.8~5.5V	2.45	2.5	2.55	V[1]
V_{REF15}	Internal 1.5V Reference Voltage	Room temperature 25°C 3.3V	1.485	1.5	1.515	V
V_{REF15}	Internal 1.5V Reference Voltage	-40~85°C 2~5.5V	1.47	1.5	1.53	V[1]
T_{Coeff}	Internal 2.5V 1.5V temperature coefficient	-40~85°C	-	-	120	ppm/°C
$T_{stable (BGR)}$	BGR stable time	Room temperature 25°C 3.3V	-	60	-	us

1. The data is based on the assessment results and is not tested in production.

7.3.5 Supply Current characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and program in memory The location in and executed code, etc.

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level——VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 wait cycle for 0~24 MHz, 1 wait cycle for 24~48 MHz).
- When the peripheral is turned on: $f_{PCLK0} = f_{HCLK}$, $f_{PCLK1} = f_{HCLK}$.

Table 7-9 Operating Current Characteristics

Symbol	Pameter	Conditions			Typ(1)	Max(2)	Unit
I_{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	V_{CAP}=1.2V V_{CC}=3.3V T_A=2x℃	RCH clock source	3M	520	-	μA
				4M	590	-	
				6M	730	-	
				12M	1150	-	
			PLL RCH12M to xxM clock source	16M	2000	-	
				24M	2600	-	
				32M	3280	-	
				64M	5830	-	
	All peripherals clock OFF, Run while(1) in RAM	V_{CAP}=1.2V V_{CC}=3.3V T_A=2x℃	RCH clock source	3M	380	-	μA
				4M	400	-	
				6M	460	-	
				12M	610	-	
			PLL RCH12M to xxM clock source	16M	1280	-	
				24M	1520	-	
				32M	1820	-	
				64M	2920	-	
I_{DD} (Run CoreMark)	All peripherals clock OFF, Run while(1) in Flash	V_{CAP}=1.2V V_{CC}=3.3V T_A=2x℃	RCH clock source	3M	763	-	μA
				4M	903	-	
				6M	1175	-	
				12M	1775	-	
			PLL RCH12M to xxM clock source	16M	2338	-	
				24M Flash Wait=1	2549	-	
				32M Flash Wait=1	2835	-	

Symbol	Pameter	Conditions			Typ(1)	Max(2)	Unit
				64M Flash Wait=2	4310	-	
I_{DD} (Run mode)	All peripherals clock ON, Run while(1) in Flash	V_{CAP}=1.2V V_{CC}=2.0V~5.5V T_A=-40℃~85℃	RCH clock source	3M	492	-	μA
				4M	557	-	
				6M	685	-	
				12M	1071	-	
			PLL RCH12M to xxM clock source	16M	1894	-	
				24M Flash Wait=1	2445	-	
				32M Flash Wait=1	3070	-	
				64M Flash Wait=2	5425	-	
	All peripherals clock OFF, Run while(1) in Flash	V_{CAP}=1.2V V_{CC}=2.0V~5.5V T_A=-40℃~85℃	RCH clock source	3M	356	-	μA
				4M	375	-	
				6M	414	-	
				12M	528	-	
			PLL RCH12M to xxM clock source	16M	1171	-	
				24M Flash Wait=1	1366	-	
				32M Flash Wait=1	1615	-	
				64M Flash Wait=2	2518	-	
I_{DD} (Sleep mode)	All peripherals clock ON, Run while(1) in Flash	V_{CAP}=1.2V V_{CC}=2.0V~5.5V T_A=-40℃~85℃	RCH clock source	3M	460	-	μA
				4M	514	-	
				6M	621	-	
				12M	944	-	
			PLL RCH12M to xxM clock source	16M	1725	-	
				24M Flash Wait=1	2191	-	
				32M Flash Wait=1	2727	-	
				64M Flash Wait=2	4741	-	
	All peripherals clock OFF, Run while(1) in Flash	V_{CAP}=1.2V V_{CC}=2.0V~5.5V T_A=-40℃~85℃	RCH clock source	3M	323	-	μA
				4M	332	-	
				6M	348	-	
				12M	398	-	
			PLL RCH12M to xxM clock source	16M	998	-	
				24M Flash Wait=1	1106	-	
				32M Flash Wait=1	1267	-	
				64M Flash Wait=2	1824	-	
I_{DD} (LP Run)	All peripherals clock ON, Run while(1) in Flash	V_{CAP}=1.2V V_{CC}=2.0V~5.5V TA=-40℃~85℃	32K clock source	RCL32K	113	-	μA
				XTL32K Driver=2	112	-	
				RCL32K	112	-	

Symbol	Pameter	Conditions			Typ(1)	Max(2)	Unit
	All peripherals clock OFF, Run while(1) in Flash			XTL32K Driver=2	111	-	
I_{DD} (LP Sleep)	All peripherals clock ON, Run while(1) in Flash	V_{CAP}=1.2V V_{CC}=2.0V~5.5V TA=-40℃~85℃	32K clock source	RCL32K	113	-	μA
				XTL32K Driver=2	113	-	
	All peripherals clock OFF, Run while(1) in Flash			RCL32K	111	-	
				XTL32K Driver=2	111	-	
I_{DD} (DeepSleep)	All peripherals clock OFF	V_{CAP}=1.2V V_{CC}=2.0V~5.5V TA=-40℃~85℃	NO CLK	-	21	-	μA
	All peripherals clock OFF		RCL32K	-	22	-	
	All peripherals clock OFF		XTL32K	-	21	-	
	Other peripherals clock OFF		RCL32K	WDT	22	-	
	Other peripherals clock OFF		RCL32K	LVD	22	-	
	Other peripherals clock OFF		RCL32K	WDT+LVD	22	-	

1. If there are no other specified conditions, the value of this Typ is measured at 25 ℃ & VCC = 3.3 V.
2. If there are no other specified conditions, the value of Max is the maximum value in the range of VCC = 2.0-5.5 & Temperature = -40 °C – 85 °C.
3. The data is based on the assessment results and is not tested in production.

7.3.6 Time to wake up from low power mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- RCH oscillator when entering deep sleep

Table 7-10 Low Power Mode Wake Up Time

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{wu}	Sleep mode wake-up time	-	-	1.8	-	μs
	Deep sleep wake-up time	F_{MCLK} = 4 MHz	-	13	-	μs
		F_{MCLK} = 6 MHz	-	11	-	μs
		F_{MCLK} = 12 MHz	-	9	-	μs
		F_{MCLK} = 12 MHz (Flash does not enter low power mode)	-	4	-	μs

1. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

7.3.7 External timer characteristic

7.3.7.1 External input high-speed clock

Table 7-11 External input high-speed clock characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTH_ext}	User external clock frequency (1)	-	8	-	24	MHz
V_{XTHH}	Input pin high level voltage	-	0.7VCC	-	VCC	V
V_{XTHL}	Input pin low voltage	-	VSS	-	0.3VCC	V
$T_{r(XTH)}$	Rise time (1)	-	-	-	20	ns
$T_{f(XTH)}$	Falling time (1)	-	-	-	20	ns
$T_{w(XTH)}$	Enter high or low time (1)	-	16	-	-	ns
$C_{in(XTH)}$	Input capacitive reactance (1)	-	-	5	-	pF
Duty	Duty ratio	-	40	-	60	%
I_L	Input leakage current	-	-	-	±1	μA

1. Guaranteed by design, not tested in production.

7.3.7.2 External input low-speed clock

Table 7-12 External input low-speed clock characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTL_ext}	User external clock frequency (1)	-	0	32.768	1000	kHz
V_{XTLH}	Input pin high level voltage	-	0.7VCC	-	VCC	V
V_{XTLL}	Input pin low voltage	-	VSS	-	0.3VCC	V
$T_{r(XTL)}$	Rise time (1)	-	-	-	50	ns
$T_{f(XTL)}$	Falling time (1)	-	-	-	50	ns
$T_{w(XTL)}$	Enter high or low time (1)	-	450	-	-	ns
$C_{in(XTL)}$	Input capacitive reactance (1)	-	-	5	-	pF
Duty	Duty ratio	-	30	-	70	%
I_L	Input leakage current	-	-	-	±1	μA

1. Guaranteed by design, not tested in production.

7.3.7.3 High-speed external clock XTH

The high-speed external clock (XTH) can be generated using a 8~24 MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

External XTH crystal oscillator (1) (2)

Table 7-13 High speed external clock XTH

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{CLK}	Oscillation frequency	-	8	-	24	MHz
ESR_{CLK}	Supported crystal oscillator ESR range	24M	-	-	60	Ohm
		16M	-	-	80	
		8M	-	-	120	
CLX(3)	Load capacitance	Both pins have load capacitance, including parasitic capacitance	4	12	20	pF
gm	transconductance	SYSCTRL_XTHCR[3:0] = 0b1111	-	11	-	mS
		SYSCTRL_XTHCR[3:0] = 0b1110	-	6.286	-	
		SYSCTRL_XTHCR[3:0] = 0b1101	-	4.411	-	
		SYSCTRL_XTHCR[3:0] = 0b1100	-	3.42	-	
		SYSCTRL_XTHCR[3:0] = 0b1011	-	6.963	-	
		SYSCTRL_XTHCR[3:0] = 0b1010	-	3.98	-	
		SYSCTRL_XTHCR[3:0] = 0b1001	-	2.794	-	
		SYSCTRL_XTHCR[3:0] = 0b1000	-	2.167	-	
		SYSCTRL_XTHCR[3:0] = 0b0111	-	2.42	-	
		SYSCTRL_XTHCR[3:0] = 0b0110	-	1.369	-	
		SYSCTRL_XTHCR[3:0] = 0b0101	-	0.955	-	
		SYSCTRL_XTHCR[3:0] = 0b0100	-	0.738	-	
		SYSCTRL_XTHCR[3:0] = 0b0011	-	1.177	-	
		SYSCTRL_XTHCR[3:0] = 0b0010	-	0.670	-	
		SYSCTRL_XTHCR[3:0] = 0b0001	-	0.469	-	
		SYSCTRL_XTHCR[3:0] = 0b0000	-	0.363	-	
Duty	Duty ratio	-	40	50	60	%
Idd(4)	Current	SYSCTRL_XTHCR[3:0] = 0b1111	-	1200	-	uA
		SYSCTRL_XTHCR[3:0]=1110, Freq=24M, VCC=3.3V, Temp=25C	-	750	-	uA
		SYSCTRL_XTHCR[3:0] = 0b0000	-	150	-	uA
T_{start}(5)	Start time	24M, CL=16pF@ SYSCTRL_XTHCR[3:0] =	-	300	-	us

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
		0b1110				
		16 MHz, CL=16pF@ SYSCTRL_XTHCR[3:0] = 0b1010	-	400	-	us
		8MHz, CL=16pF@ SYSCTRL_XTHCR[3:0] = 0b0110	-	1	-	ms

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Resulted from comprehensive evaluation, not tested in production.
3. C_{LX} refers to the two pin load capacitors C_{L1} and C_{L2} of XTAL. For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors designed for high-frequency applications, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually specify the load capacitance as a serial combination of C_{L1} and C_{L2}. When selecting C_{L1} and C_{L2}, it should be based on parameters such as the frequency of the crystal oscillator and ESR, and the capacitive reactance of the PCB and MCU pins should be taken into consideration.
4. Current varies with frequency and drive configuration.
5. T_{start} is the start-up time, which is the period of time from when the software enables XTH until a stable frequency output is obtained. This value is measured using a standard crystal resonator with the SYSCTRL_XTHCR[5:4]=10 setting. It may vary greatly depending on the crystal manufacturer and model.

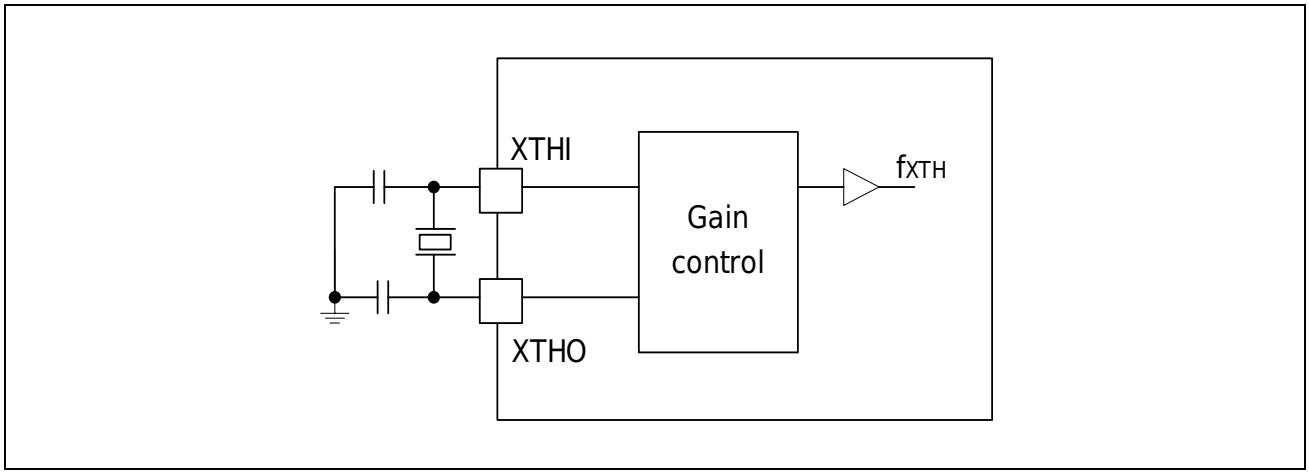


Figure 7-2 Schematic diagram of external high-speed clock

7.3.7.4 Low-speed external clock XTL

The low-speed external clock (XTL) can be generated using a 32.768 kHz crystal/ceramic resonator oscillator. The information given in this section is based on typical external components and the results obtained through comprehensive characteristic evaluation. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 7-14 Low-speed external clock XTL(1)

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{CLK}	Oscillation frequency	-	-	32.768	-	kHz
ESR_{CLK}	Supported crystal oscillator ESR range	-	-	-	60	kΩ
C_{LX}(2)	Load capacitance	Configure as required by the crystal manufacturer. (Including parasitic capacitance)	8	12	20	pF
DC_{ACLK}	Duty ratio	-	30	50	70	%
Idd(3)	Current	SYSCTRL_XTLCR[3:0]=1111	-	2000	-	nA
		SYSCTRL_XTLCR[3:0]=0000	-	400	-	nA
g_m	transconductance	SYSCTRL_XTLCR[3:0]=1111	-	20.1	-	uS
		SYSCTRL_XTLCR[3:0]=1110	-	10.1	-	
		SYSCTRL_XTLCR[3:0]=1101	-	6.6	-	
		SYSCTRL_XTLCR[3:0]=1100	-	4.9	-	
		SYSCTRL_XTLCR[3:0]=1011	-	18.1	-	
		SYSCTRL_XTLCR[3:0]=1010	-	9.1	-	
		SYSCTRL_XTLCR[3:0]=1001	-	5.9	-	
		SYSCTRL_XTLCR[3:0]=1000	-	4.4	-	
		SYSCTRL_XTLCR[3:0]=0111	-	16.2	-	
		SYSCTRL_XTLCR[3:0]=0110	-	8.1	-	
		SYSCTRL_XTLCR[3:0]=0101	-	5.2	-	
		SYSCTRL_XTLCR[3:0]=0100	-	3.9	-	
		SYSCTRL_XTLCR[3:0]=0011	-	14.1	-	
		SYSCTRL_XTLCR[3:0]=0010	-	7.0	-	
		SYSCTRL_XTLCR[3:0]=0001	-	4.6	-	
		SYSCTRL_XTLCR[3:0]=0000	-	3.4	-	
$T_{start(4)}$	Start time	ESR=30 kΩ C_L=12 pF 40% - 60% duty cycle has been reached	-	1000	-	ms

1. Resulted from comprehensive evaluation, not tested in production.
2. C_{LX} refers to the load capacitance of the two pins of XTAL. The user must select the capacitance value of this capacitor according to the requirements of the crystal manufacturer.

If the crystal manufacturer gives the value of the load capacitor, the matching capacitor should be twice the value of the load capacitor given by the crystal manufacturer.

If the crystal manufacturer gives the capacitance value of the matching capacitor, you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.

Example: When the crystal manufacturer gives the load capacitance of the crystal as 8 pF, the capacitance of the matching capacitor should be 16 pF. Considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 15 pF or 12 pF.

The crystal manufacturer gives the matching capacitance of the crystal as 12 pF, the matching capacitance should be 12 pF. Considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 10 pF or 8 pF.

3. Choose a high-quality oscillator with a small ESR value (such as MSIV-TIN32.768 kHz), and you can optimize the current consumption by adjusting the SYSCTRL_XTLCR[3:0] setting value. Current consumption is proportional to the transconductance (gm) provided by the circuit.
4. T_{start} is the start-up time, which is the time from the software enabling XTL to start measuring until a stable 32768 Hz oscillation is obtained. This value is measured using a standard crystal resonator with the settings SYSCTRL_XTLCR[3:0]=1001 and SYSCTRL_XTLCR[5:4]=10. It may vary greatly depending on the crystal manufacturer and model.

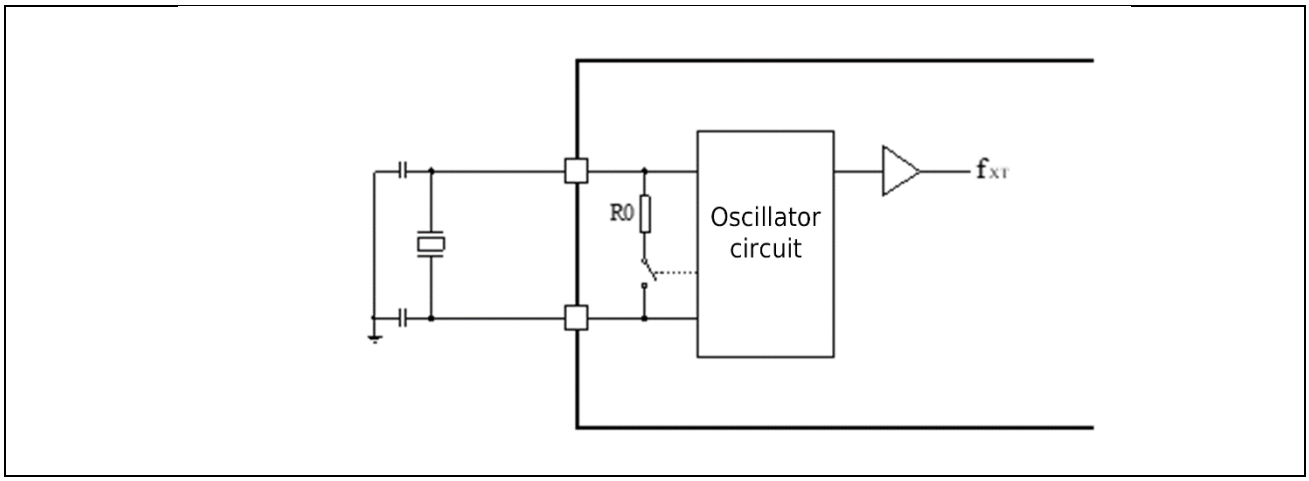


Figure 7-3 Schematic diagram of external low-speed clock

Note:

– *The feedback resistor R0 has been integrated in the chip.*

7.3.8 Internal timer characteristics

7.3.8.1 Internal RCH oscillator

Table 7-15 Internal high-speed clock RCH oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dev	RCH oscillator accuracy	User trimming step for given VCC and T_A conditions	-	0.25	-	%
		VCC = 2 ~ 5.5V T_{AMB} = -40 ~ 85°C	-1.5	0.25	1.5	%
		VCC = 2 ~ 5.5V T_{AMB} = -20 ~ 50°C	-1	0.25	1	%
F_{CLK}	Oscillation frequency	-	-	12	-	MHz
I_{clk}	Current	F_{MCLK} = 12MHz	-	120	-	μA
DC_{CLK}	Duty Cycle (1)	-	45	50	55	%

1. Resulted from comprehensive evaluation, not tested in production.

7.3.8.2 Internal RCL oscillator

Table 7-16 Internal low-speed clock RCL oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dev	RCL oscillator accuracy	User trimming step for given VCC and T_A conditions	-	0.5	-	%
		VCC = 2 ~ 5.5V T_{AMB} = -40 ~ 85°C	-2	-	2	%
		VCC = 2 ~ 5.5V T_{AMB} = -20 ~ 50°C	-1.5	-	1.5	%
F_{CLK}	Oscillation frequency	-	-	38.4	-	KHz
			-	32.768	-	KHz
T_{CLK}	Start time	-	-	150	-	μs
DC_{CLK}	Duty Cycle (1)	-	25	50	75	%
I_{CLK}	Power consumption	-	-	0.9	-	μA

1. Resulted from comprehensive evaluation, not tested in production.

7.3.9 PLL Characteristic

Table 7-17 PLL Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{in} (1)	Input clock	-	4	4	24 注	MHz
$Duty_{in}$	Input clock duty cycle	-	40	-	60	%
F_{out}	Output frequency	-	12	-	64	MHz
$Duty_{out}$ (1)	Output duty cycle	-	48%	-	52%	-

Note: *The maximum PLL input source clock is 24 MHz, and the maximum input clock is 12 MHz after prescaling.*

7.3.10 Memory Characteristics

Table 7-18 Memory characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
EC_{Flash}	Erase times	Regulator voltage=1.5V, T_{AMB} = 25℃	20	-	-	kcycles
RET_{Flash}	Data retention period	T_{AMB} = 85℃, after 20 kcycles	20	-	-	Years
T_{b_prog}	Programming time (bytes)	-	22	-	30	μs
T_{w_prog}	Programming time (words)	-	40	-	52	μs
T_{p_erase}	Page erase time	-	4	-	5	ms
T_{m_erase}	Whole chip erase time	-	30	-	40	ms

7.3.11 EFT Characteristic

A chip reset can restore the system to normal operation.

Table 7-19 EFT Characteristics

Symbol	Level/Type
EFT to IO (IEC61000-4-4)	TBD
EFT to Power (IEC61000-4-4)	TBD

Software recommendations

The software process must include control to deal with program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data is destroyed (control registers, etc.)

During the EFT test, interference that exceeds the application requirements can be directly applied to the chip power supply or IO. When an unexpected action is detected, the software part is strengthened to prevent unrecoverable errors.

7.3.12 ESD Characteristic

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Table 7-20 ESD Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$VESD_{HBM}$	ESD @ Human Body Mode	-	-	4	-	KV
$VESD_{CDM}$	ESD @ Charge Device Mode	-	-	1	-	KV
Ilatchup	Latch up current	-	-	200	-	mA

7.3.13 I/O port characteristics

7.3.13.1 Output characteristics——ports

Table 7-21 Port output characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
V_{OH}	High level output voltage Low driving strenth	Driving Current 4 mA, VCC = 3.3 V (see Note 1)	VCC-0.25	-	V
		Driving Current 8 mA, VCC = 3.3 V (see Note 2)	VCC-0.60	-	V
V_{OL}	Low level output voltage Low driving strenth	Driving Current 4 mA, VCC = 3.3 V (see Note 1)	-	VSS+0.25	V
		Driving Current 8 mA, VCC = 3.3 V (see Note 2)	-	VSS+0.70	V
V_{OHD}	High level output voltage High driving strenth	Driving Current 8 mA, VCC = 3.3 V (see Note 1)	VCC-0.25	-	V
		Driving Current 18 mA, VCC = 3.3V (see Note 2)	VCC-0.60	-	V
V_{OLD}	Low level output voltage High driving strenth	Driving Current 8 mA, VCC = 3.3 V (see Note 1)	-	VSS+0.25	V
		Driving Current 18 mA, VCC = 3.3 V (see Note 2)	-	VSS+0.60	V

NOTES:1. The maximum total current, I_{OH}(max) and I_{OL}(max), for all outputs combined, should not exceed 40 mA to satisfy the maximum specified voltage drop.

2. The maximum total current, I_{OH}(max) and I_{OL}(max), for all outputs combined, should not exceed 100 mA to satisfy the maximum specified voltage drop.

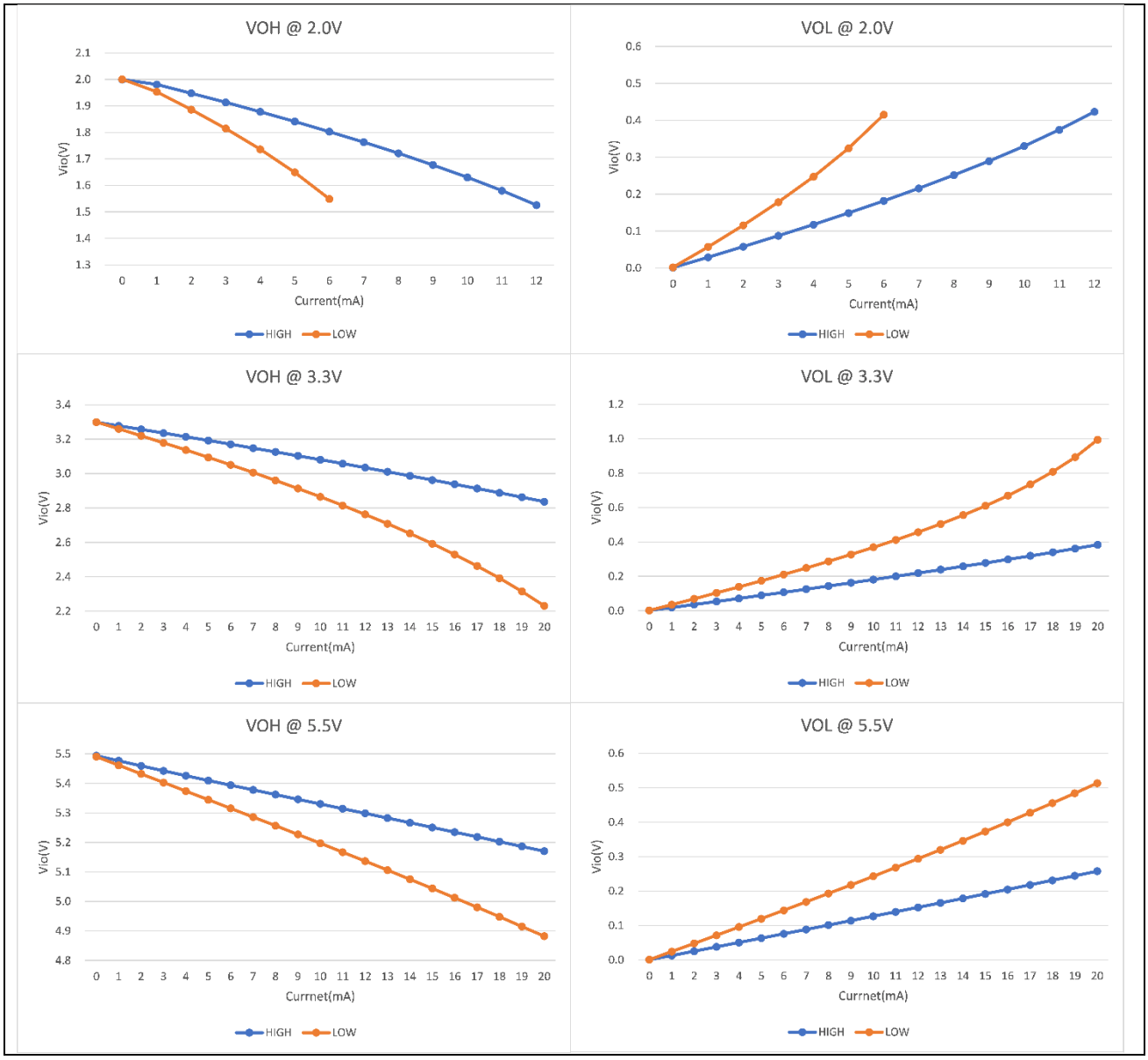


Figure 7-4 Output port VOH/VOL measured curve

7.3.13.2 Input Characteristics - Ports PA, PB, PC, PD

Table 7-22 PA/PB/PC/PD port input characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{IH}	Positive-going input threshold voltage	VCC=2.0V	0.7VCC	-	-	V
		VCC=3.3V	0.7VCC	-	-	V
		VCC=5.5V	0.7VCC	-	-	V
V_{IL}	Negative-going input threshold voltage	VCC=2.0V	-	-	0.3VCC	V
		VCC=3.3V	-	-	0.3VCC	V
		VCC=5.5V	-	-	0.3VCC	V
$V_{hys(1)}$	Input voltage hysteresis (V_{IH} - V_{IL})	VCC=2.0V	-	0.14	-	V
		VCC=3.3V	-	0.22	-	V
		VCC=5.5V	-	0.34	-	V
$R_{pullhigh}$	Pullup resistor	Pullup enabled VCC=3.3V	-	55	-	kΩ
$R_{pulllow}$	Pulldown resistor	Pulldown enabled VCC=3.3V	-	55	-	kΩ
C_{input}	Input capacitance	-	-	5	-	pf

1. Resulted from comprehensive evaluation, not tested in production.

7.3.13.3 Port external input sampling requirements——Timer Gate/Timer Clock

Table 7-23 Timer Gate/Timer Clock external input sampling requirements

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$t_{(int)}$	External interrupt timing	External trigger signal for the interrupt flag(1)	-	30	-	ns
$t_{(cap)}$	Timer capture timing	Timer capture pulse width	-	0.5	-	μs
$t_{(clk)}$	Timer clock frequency applied to pin	Timer external clock input fHCLK = 4MHz	-	-	PCLK/2	MHz

NOTES: 1.The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

2. Resulted from comprehensive evaluation, not tested in production.

7.3.13.4 Port leakage characteristics - PA, PB, PC, PD

Table 7-24 PA/PB/PC/PD port leakage characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$I_{lkg(Px.y)}$	Leakage current	$V_{(Px.y)}$ (see Note 1,2)	-	±50	-	nA

NOTES:1.The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.

2.The port pin must be selected as input.

7.3.14 RESETB pin characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

Table 7-25 RESETB pin characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$V_{IL(RESETB)}$ (1)	Input low level voltage	-	-0.3	-	0.3VCC	V
$V_{IH(RESETB)}$	Input high level voltage	-	0.7VCC	-	VCC+0.3	V
$V_{hys(RESETB)}$	Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistance	$V_{IN} = V_{SS}$	-	55	-	KΩ
$T_{F(RESETB)}$ (1)	Input filter pulse	-	-	-	2	us
$T_{NF(RESETB)}$ (1)	Input unfiltered pulse	-	10	-	-	us

1. Guaranteed by design, not tested in production.

7.3.15 ADC Characteristic

Table 7-26 ADC Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{ADCIN}	Input voltage range of ADC	-	0	-	V_{REF+}	V
V_{REF+}(1)	Positive reference voltage	-	1.5	-	AVCC	V
V_{REF-}	Negative reference voltage	-	-	AVSS	-	V
$DEV_{AVCC/3}$	Accuracy of AVCC/3	-	-	±3	-	%
V_{INBUF}(1)	Input voltage range of the input buffer within which the accuracy is guaranteed	(AVCC-0.1V) < V_{REF+}	0.1	-	AVCC-0.1	V
		(AVCC-0.1V) ≥ V_{REF+}	0.1	-	V_{REF+}	
I_{ADC1}	Active current including reference generator and buffer	200Ksps	-	2.0	-	mA
I_{ADC2}	Active current without reference generator and buffer	1Msps	-	1.0	-	mA
C_{ADCIN}(1)	ADC input capacitance	-	-	19	-	pF
R_{ADC}(1)	ADC sampling switch impedance	-	-	1.2	-	kΩ
R_{AIN}(1)	ADC external input resistor(2)	-	-	-	100	kΩ
f_{ADCCLK}	ADC clock Frequency	-	-	-	16M	Hz
$T_{ADCSTART}$(1)	Startup time of reference generator and ADC core	-	-	20	-	μs
T_S	Sampling time	-	4	-	10	1/ f_{ADCCLK}
$T_{ADCCONV}$	Total conversion time (including sampling time)	-	-	T_S+12	-	1/ f_{ADCCLK}
ENOB(1)	Effective Bits	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=2.0V REF=EXREF	-	10.7	-	Bit
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=2.0V REF=VCC	-	10.8	-	Bit
		200Ksps@VCC>=2.0V REF=internal 1.5V	-	10.0	-	Bit
		200Ksps@VCC>=2.8V REF=internal 2.5V	-	10.2	-	Bit
SNR(1)	Signal to Noise Ratio	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=2.0V REF=EXREF	-	70.0	-	dB
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=2.0V REF=VCC	-	70.3	-	dB
		200Ksps@VCC>=2.0V REF=internal 1.5V	-	61.8	-	dB
		200Ksps@VCC>=2.8V REF=internal 2.5V	-	64.5	-	dB
DNL(1)	Differential non-linearity	200KSps; VREF=EXREF/AVCC	-1	-0.9/+1.2	+2.5	LSB

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
INL(1)	Integral non-linearity	200KSps; VREF=EXREF/AVCC	-4.5	-2.1/+1.6	+3	LSB
E_o(1)	Offset error	VREF=EXREF/AVCC	-	-3/+3	-	LSB
E_g(1)	Gain error	VREF=EXREF/AVCC	-	-3/+3	-	LSB
E_T(1)	Total unadjusted error	VREF=EXREF/AVCC	-	-5/+5	-	LSB

1. Guaranteed by design, not tested in production.
2. The typical application of ADC is shown in the figure below:

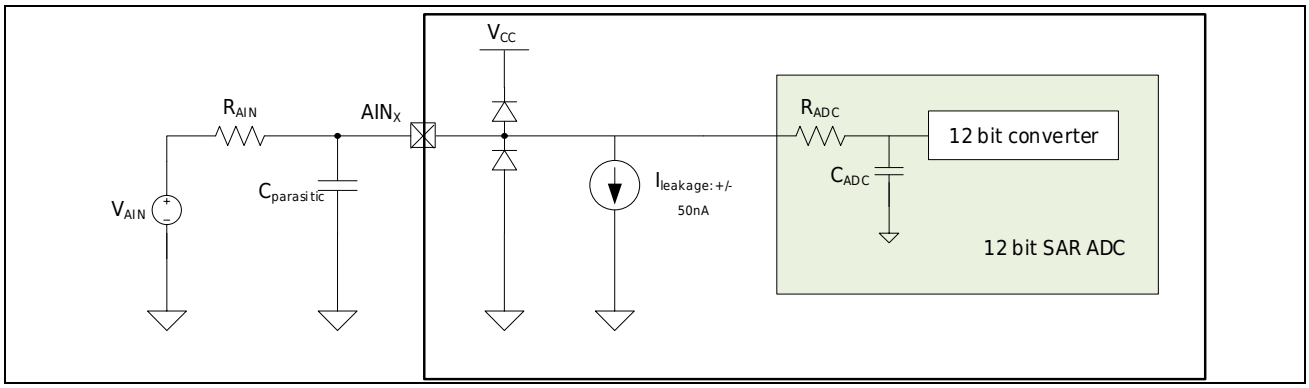


Figure 7-5 ADC typical application diagram

For the requirement of ≤0.5 LSB sampling error, the external input impedance is calculated as follows:

$$R_{AIN} \leq \frac{T_S}{C_{ADC} * (N+1) * \ln(2)} - R_{ADC} = \frac{M}{f_{ADCCLK} * C_{ADC} * (N+1) * \ln(2)} - R_{ADC}$$

whereT_S is the sampling time, N is the ADC bit number 12, $f_{ADCCLK}$is the ADC clock frequency, and M is the number of sampling cycles (the sampling time occupies M ADC clock cycles).

Register ADC_CR0<3:1> can setf_{ADCCLK} the relationship with PCLK frequencyf_{PCLK}, as shown in the following table:

Table 7-27 Relationship between ADC clock frequencyf_{ADCCLK} and PCLK division ratio

ADC_CR0<3:1>	f_{PCLK}/f_{ADCCLK}
000	2
001	4
010	6
011	8
100	10
101	12
110	14
111	1

Register ADC_CR0<13:12> can set the number of sampling periods M, as shown in the following table:

Table 7-28 The relationship between the number of ADC sampling periods M and the ADC clock frequencyf_{ADCCLK}

ADC_CR0<13:12>	M
00	4
01	6
10	9
11	10

The following table lists the correspondence between several typical external input impedance values and the minimum sampling timeT_S. For other special external input impedance values, the corresponding minimum sampling time requirements can also be calculated through the external input impedance calculation formula given above.

Table 7-29 Relationship between ADC minimum sampling time and external resistanceR_{AIN}

(Under the condition of sampling error 0.5 LSB):

R_{AIN} (Ω)	Minimum sampling timeT_S (ns)
10	218
47	224
68	228
100	234
150	243
220	255
330	275
470	301
680	338
1000	396
1500	486
2200	612
3300	811
4700	1063
6800	1441
10000	2018
15000	2919

For the above typical applications, you should pay attention to:

- Minimize the ADC input port AIN_X parasitic capacitance $C_{parasitic}$;
- In addition to consideringR_{AIN}value, if the internal resistance of signal sourceV_{AIN}, it also needs to be considered.

3. Measure ambient temperature using a temperature sensor

When the measurement channel of the ADC selects the output voltage of the temperature

sensor, the current ambient temperature can be calculated through the output result of the ADC and the calibration value stored in the Flash memory.

Table 7-30 Temperature sensor parameters

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Temp	Temp Sensor working environment	-	-40	-	85	°C
Offset	Calculated Temp offset	-	-	±5	-	°C

7.3.16 VC Characteristic

Table 7-31 VC Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vin	Input voltage range	-	0	-	5.5	V
Vincom	Input common mode range	-	0.2	-	VCC-0.2	V
Voffset	Input offset	Normal temperature 25°C 3.3V VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11	-	 ±20 ±20 ±15 ±10	-	mV
Icomp	Comparator's current	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11	-	1 4 18 36	-	μA
Tresponse	Comparator's response time when one input cross another	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11	-	20 5 1 0.2	-	μs
Tsetup	Comparator's setup time when ENABLE. Input signals unchanged.	-	-	1	-	μs
Vhysteresis	Comparator's hysteresis voltage	VCx_HYS_SEL=00 VCx_HYS_SEL=01 VCx_HYS_SEL=10 VCx_HYS_SEL=11	-	0 10 20 30	-	mV
Rin	Equivalent input resistance of signal at Positive input	-	-	-	350	Ohm
Voffset_DAC	Comparator's inner DAC's offset	VCx_NSEL=1011	-	±40	-	mV
Twarmup	From main bandgap enable to 1.2V BGR reference, Temp sensor voltage, ADC internal 1.5V, 2.5V reference stable	-	-	60	-	μs
Tfilter	Digital filter time (When the filter clock is RC150K)	VC_debounce = 000 VC_debounce = 001 VC_debounce = 010 VC_debounce = 011 VC_debounce = 100 VC_debounce = 101 VC_debounce = 110 VC_debounce = 111	-	7 14 28 112 450 1800 7200 28800	-	μs

7.3.17 OPA Characteristic

Table 7-32 OPA Characteristics

(AVCC=2.0V ~ 5.5 V, AVSS=0 V, Ta=- 40℃ ~ +85℃)

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vi	Input voltage	-	0.2	-	AVCC-0.2	V
Vo	Output voltage (1)	-	0.2	-	AVCC-0.2	V
Io	Output current (1)	-	-	-	0.3	mA
RL	Load resistance (1)	-	5	-	-	KΩ
Tstart	Initialization time (2)	-	-	3	-	μs
Vio	Input offset voltage	Vic=AVCC/2, Vo=AVCC/2, RL=5kΩ, Rs=50Ω, AZ function off;	-	±3.5	-	mV
		Vic=AVCC/2, Vo=AVCC/2, RL=5kΩ, Rs=50Ω, AZ function on, after calibration;	-	±1.5	-	mV
UGBW	Unity gain bandwidth (1)	RL=5kΩ	-	10	-	MHz
SR	Slew rate (1)	RL=5kΩ	-	5.5	-	V/μs

1. Guaranteed by design, not tested in production.
2. Need to set BGR_CR<0>=1 at the same time.

7.3.18 TIM timer features

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 7-33 Advanced Timer (ATIM) Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=64 MHz	15.6	-	ns
f_{ext}	External clock frequency	f_{TIMCLK}=64 MHz	0	32	MHz
Res_{Tim}	Timer resolution	Mode 0 free counting	-	32	Bit
		-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter	-	1	65536	t_{TIMCLK}
	When the internal clock is selected, the 32-bit counter	-	1	4294967296	t_{TIMCLK}

1. Guaranteed by design, not tested in production.

Table 7-34 Composite Timer (CTIM) Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=64 MHz	15.6	-	ns
f_{ext}	External clock frequency	f_{TIMCLK}=64 MHz	0	32	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter	-	1	65536	t_{TIMCLK}

1. Guaranteed by design, not tested in production.

Table 7-35 Low Power Timer Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=64 MHz	15.6	-	ns
f_{ext}	External clock frequency	f_{TIMCLK}=64 MHz	0	32	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter	-	1	65536	t_{TIMCLK}

1. Guaranteed by design, not tested in production.

Table 7-36 IWDT Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	IWDT overflow time	f_{WDTCLK}=32 kHz	0.125	65000	ms

1. Guaranteed by design, not tested in production.

7.3.19 Communication Interface

7.3.19.1 I2C features

I2C interface characteristics are as follows:

Table 7-37 I2C Interface Characteristics

Symbol	Parameter	Standard mode (100K)		Fast mode (400K)		High speed mode (1M)		Unit
		Minimum Value	Maximum Value	Minimum Value	Maximum Value	Minimum Value	Maximum Value	
t_{SCLL}	SCL clock low time	4.7	-	1.25	-	0.5	-	μs
t_{SCLH}	SCL clock high time	4.0	-	0.6	-	0.26	-	μs
$t_{SU.SDA}$	SDA establishment time	250	-	100	-	50	-	ns
$t_{HD.SDA}$	SDA hold time	0	-	0	-	0	-	μs
$t_{HD.STA}$	Start condition hold time	2.5	-	0.625	-	0.25	-	μs
$t_{SU.STA}$	Repeated start condition establishment time	2.5	-	0.6	-	0.25	-	μs
$t_{SU.STO}$	Stop condition establishment time	0.25	-	0.25	-	0.25	-	μs
t_{BUF}	Bus idle (stop condition to start condition)	4.7	-	1.3	-	0.5	-	μs

1. Guaranteed by design, not tested in production.

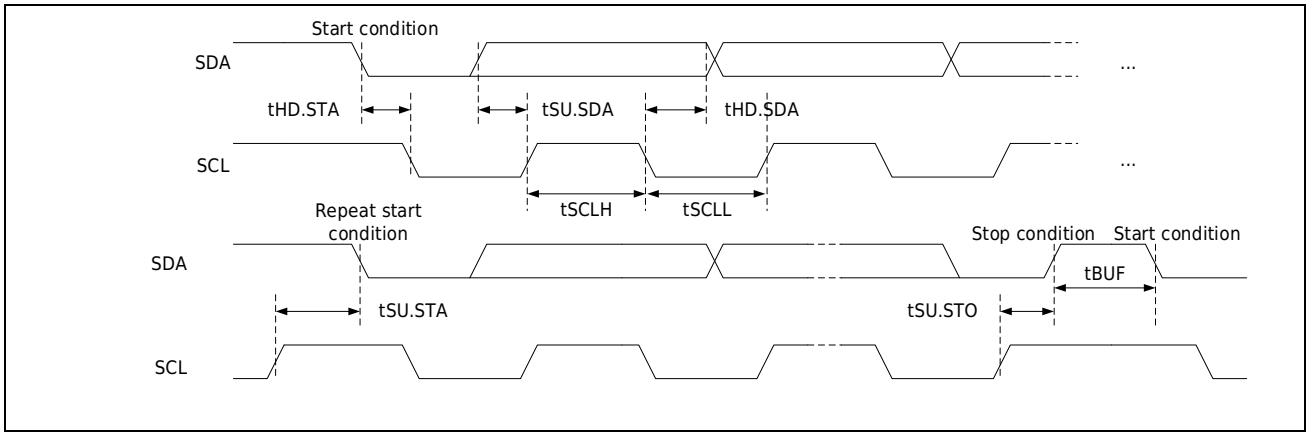


Figure 7-6 I2C Interface Timing

7.3.19.2 SPI features

Table 7-38 SPI Interface Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
$t_{c(SCK)}$	Serial clock period	Host mode	62.5	-	ns
		Slave mode f_{PCLK} = 16 MHz	250	-	ns
$t_{w(SCKH)}$	High level time of serial clock	Host mode	0.5 × $t_{c(SCK)}$	-	ns
		Slave mode	0.5 × $t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Host mode	0.5 × $t_{c(SCK)}$	-	ns
		Slave mode	0.5 × $t_{c(SCK)}$	-	ns
$t_{su(SSN)}$	Setup time selected by slave	Slave mode	0.5 × $t_{c(SCK)}$	-	ns
$t_{h(SSN)}$	Hold time selected by slave	Slave mode	0.5 × $t_{c(SCK)}$	-	ns
$t_{v(MO)}$	Effective time of host data output	f_{PCLK} = 32 MHz	-	3	ns
$t_{h(MO)}$	Hold time of host data output	f_{PCLK} = 32 MHz	2	-	ns
$t_{v(SO)}$	Effective time of slave data output	f_{PCLK} = 16 MHz	-	148	ns
$t_{h(SO)}$	Hold time of slave data output	f_{PCLK} = 16 MHz	47	-	ns
$t_{su(MI)}$	Setup time of host data input	-	25	-	ns
$t_{h(MI)}$	Hold time of host data input	-	2	-	ns
$t_{su(SI)}$	Setup time of slave data input	-	2	-	ns
$t_{h(SI)}$	Hold time of slave data input	-	95	-	ns

1. Guaranteed by design, not tested in production.

The waveform and timing parameters of the SPI interface signal are as follows:

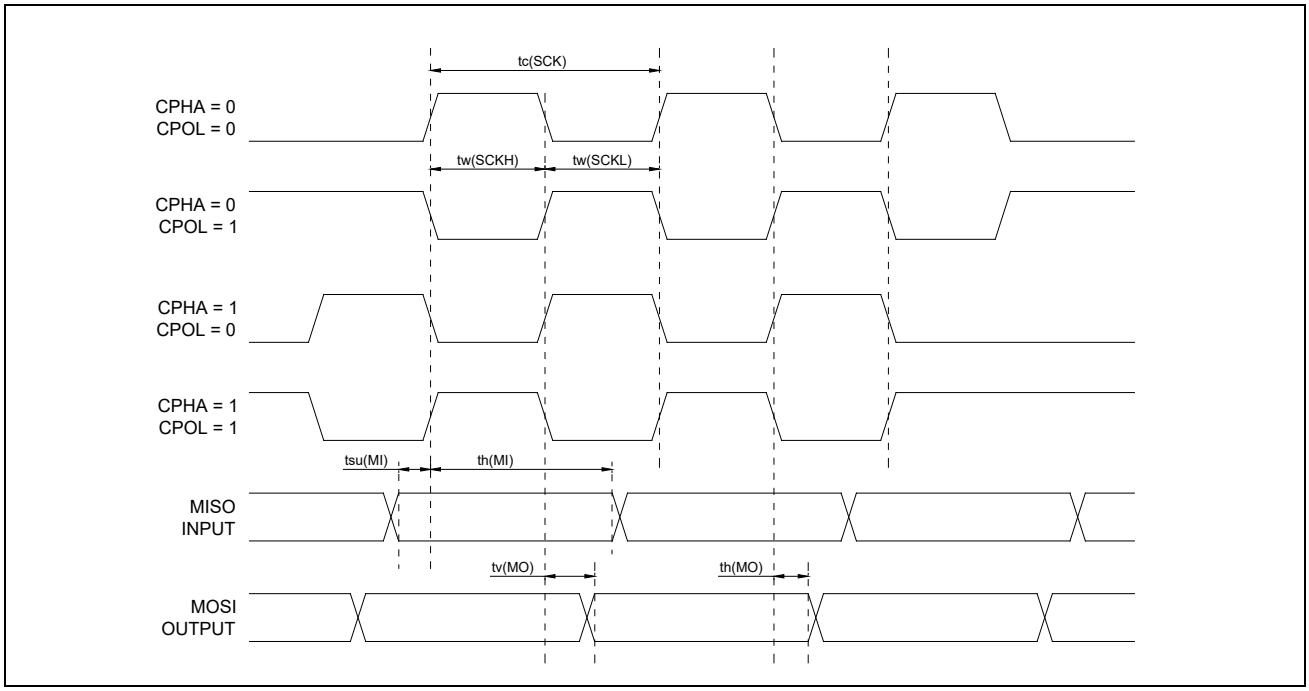


Figure 7-7 SPI Timing Diagram (Master mode)

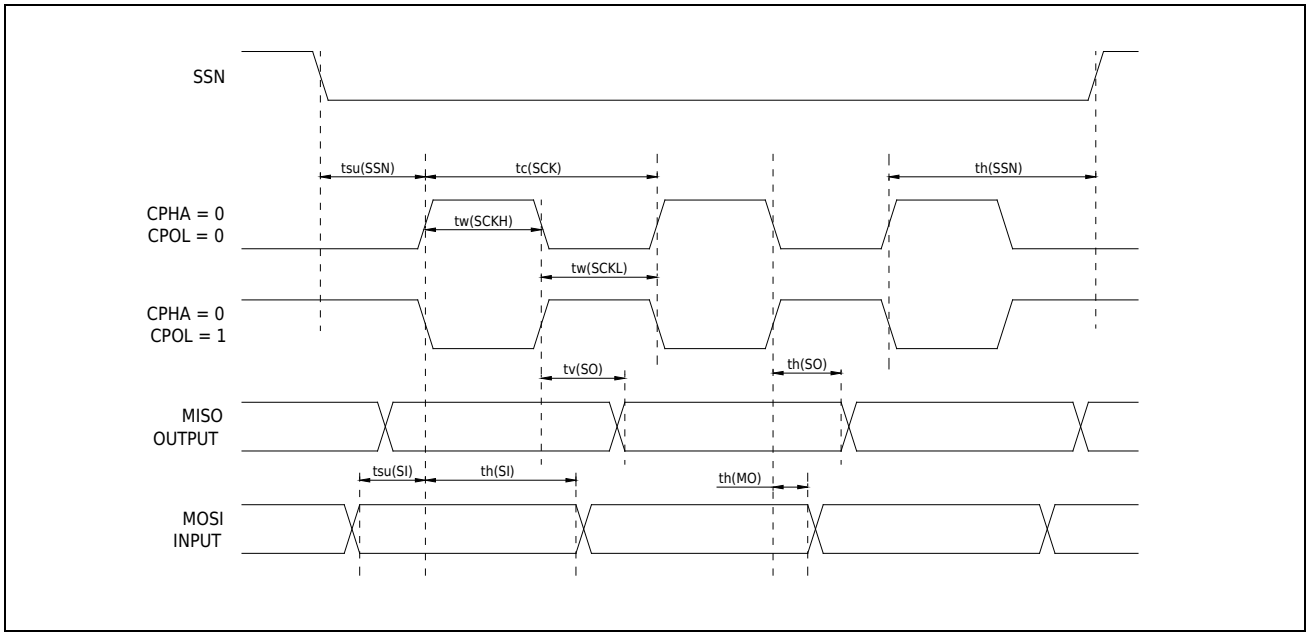


Figure 7-8 SPI Timing Diagram (slave mode cpha=0)

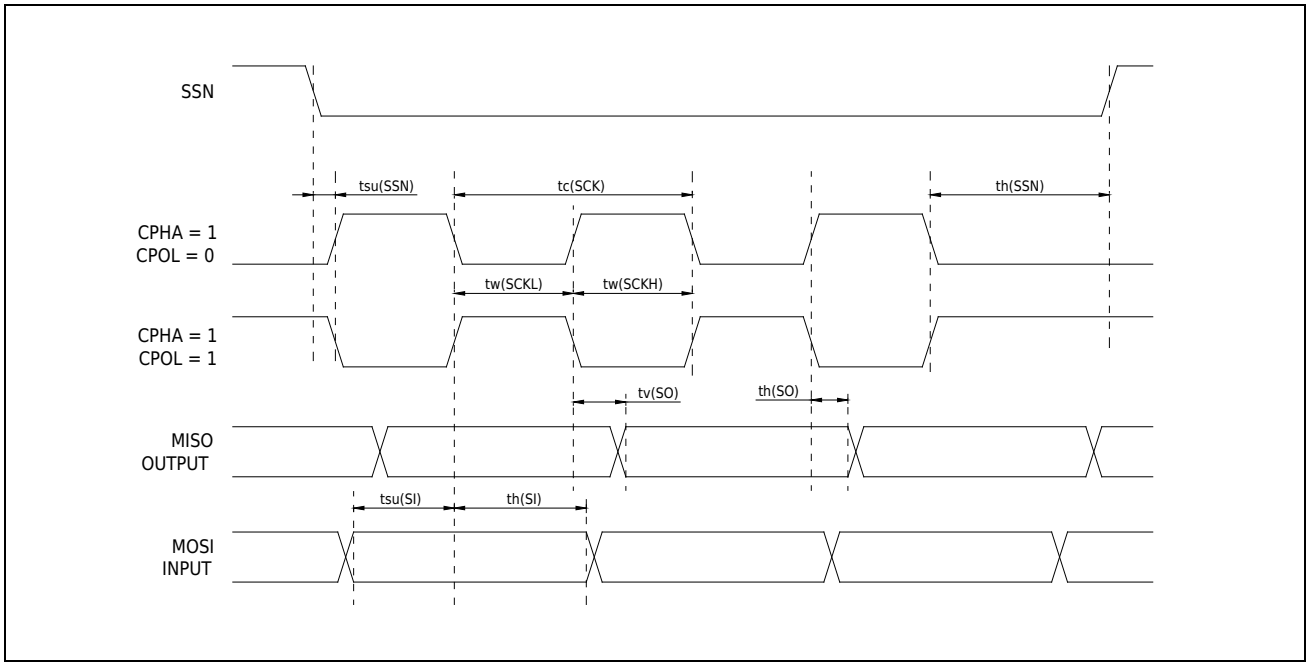
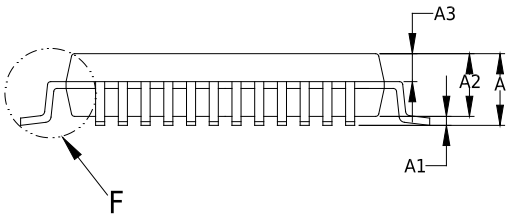


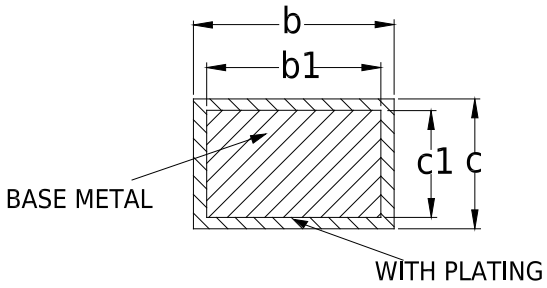
Figure 7-9 SPI Timing Diagram (slave mode cpha=1)

8 Packaging Information

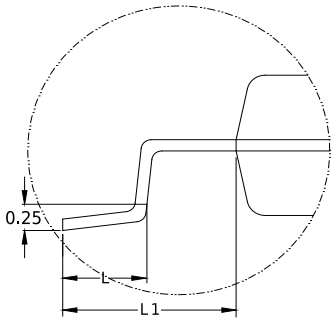
8.1 Packaging Size

LQFP48 packaging

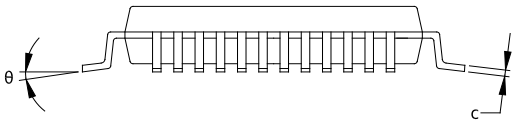


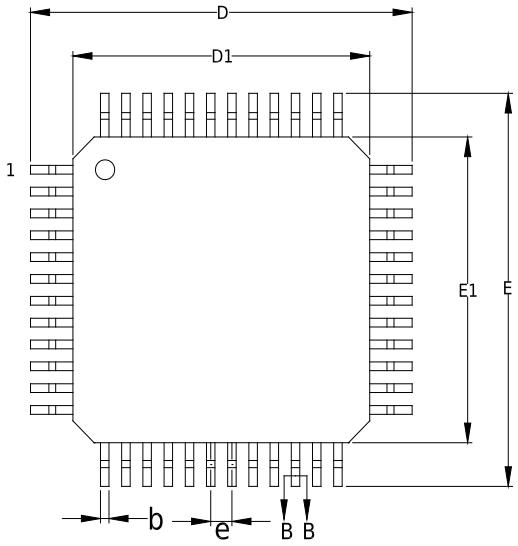


SECTION B-B



DETAIL: F



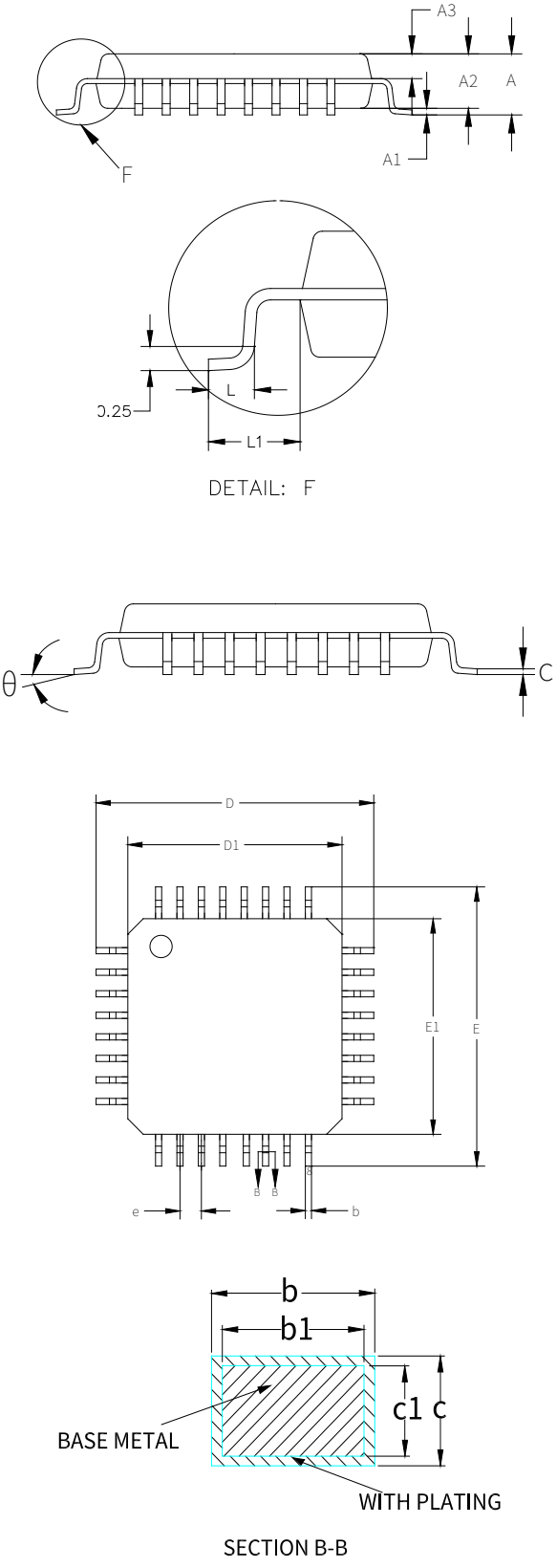


Symbol	7x7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	--	0.27
b1	0.17	0.20	0.23
c	0.10	--	0.2
c1	0.10	0.13	0.16
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

NOTE:

– *Dimensions "D1" and "E1" do not include mold flash.*

LQFP32 packaging

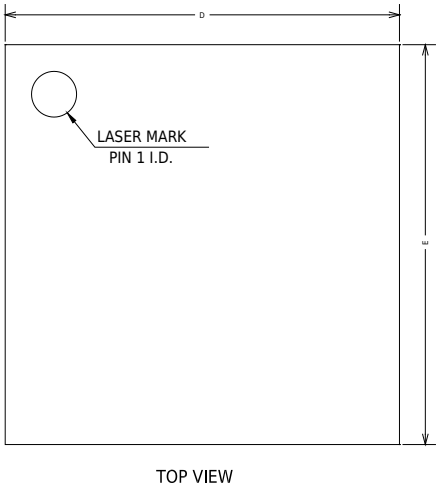


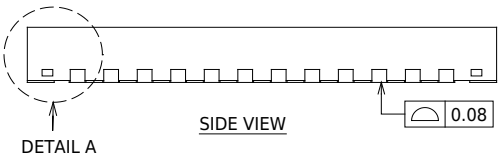
Symbol	7x7 Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.30	-	0.45
b1	0.30	0.35	0.40
c	0.10	-	0.20
c1	0.10	0.13	0.16
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.80BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	-	7°

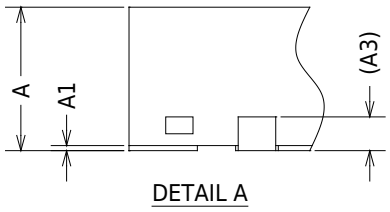
NOTE:

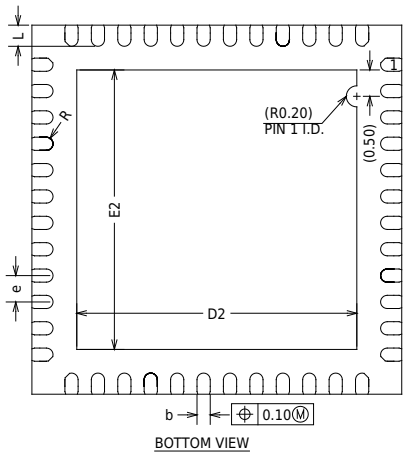
– *Dimensions "D1" and "E1" do not include mold flash.*

QFN48 packaging



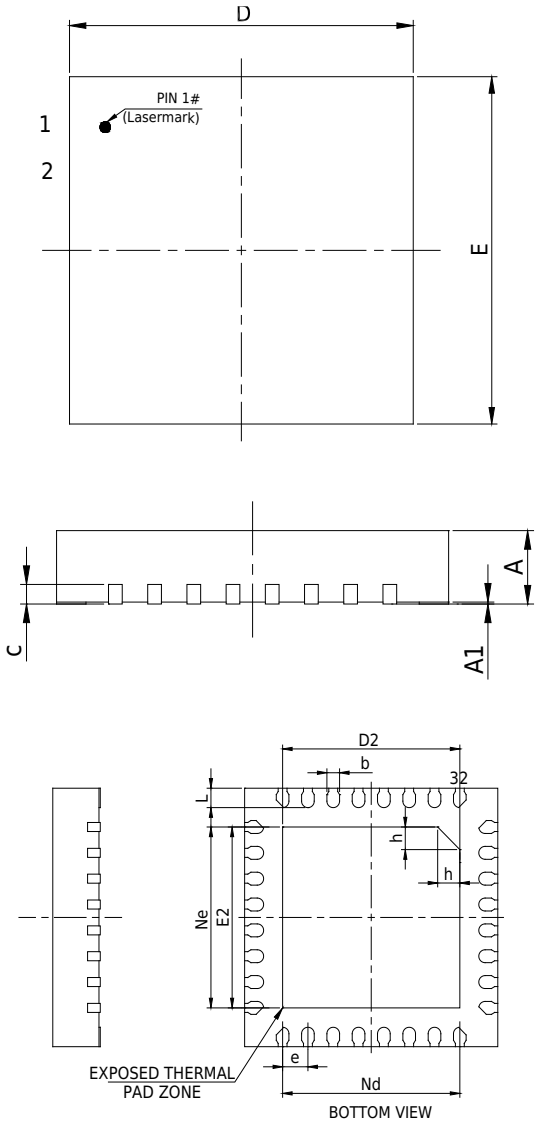






Symbol	7x7 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.18	0.25	0.30
D	6.90	7.00	7.10
D2	5.20	5.35	5.50
E	6.90	7.00	7.10
E2	5.20	5.35	5.50
e	0.40	0.50	0.60
L	0.30	0.40	0.50
R	0.09	--	--

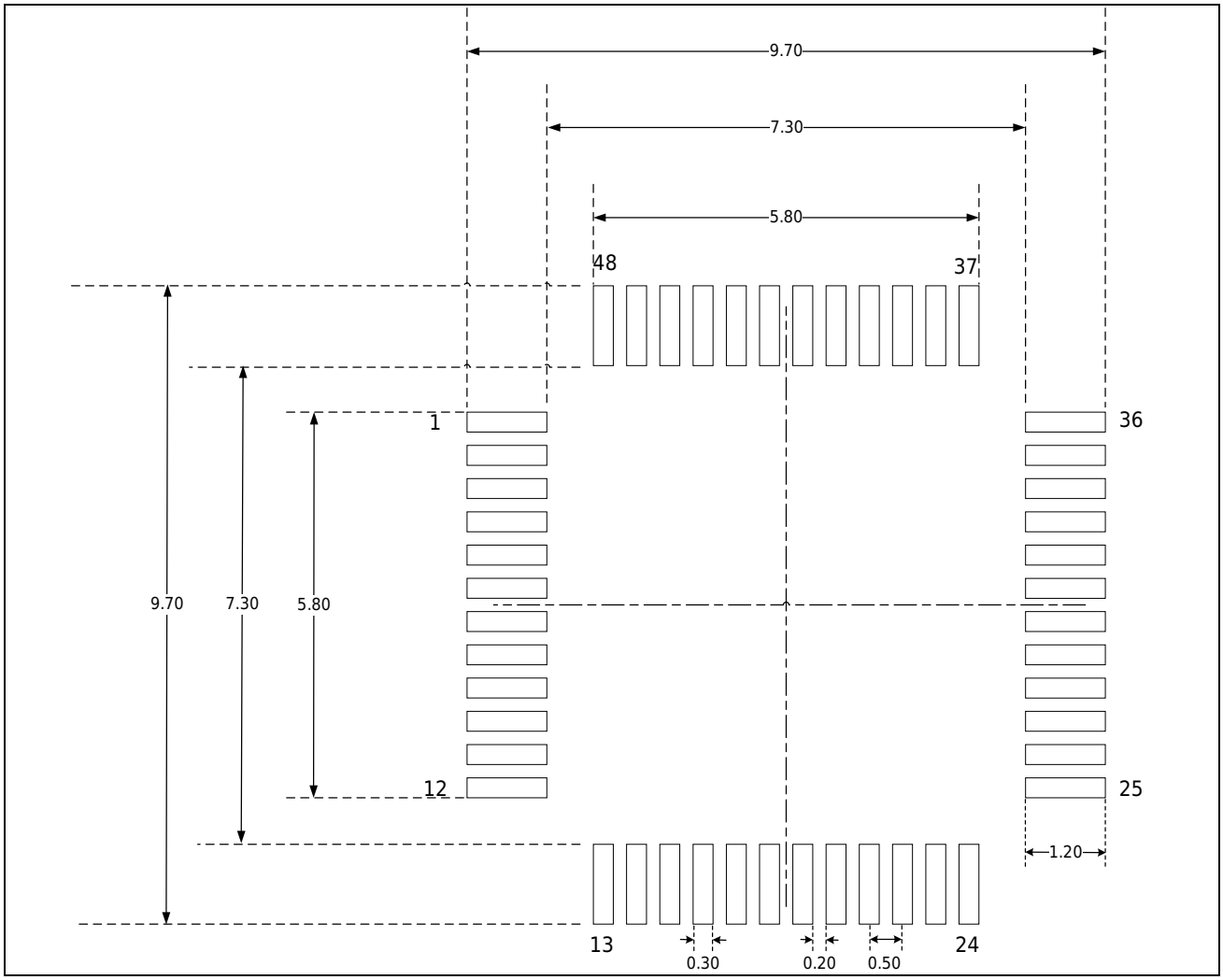
QFN32 packaging



Symbol	4x4 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.75	2.90
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.75	2.90
Ne	2.80BSC		
L	0.2	0.33	0.45
h	0.25	0.33	0.40

8.2 Schematic diagram of pad

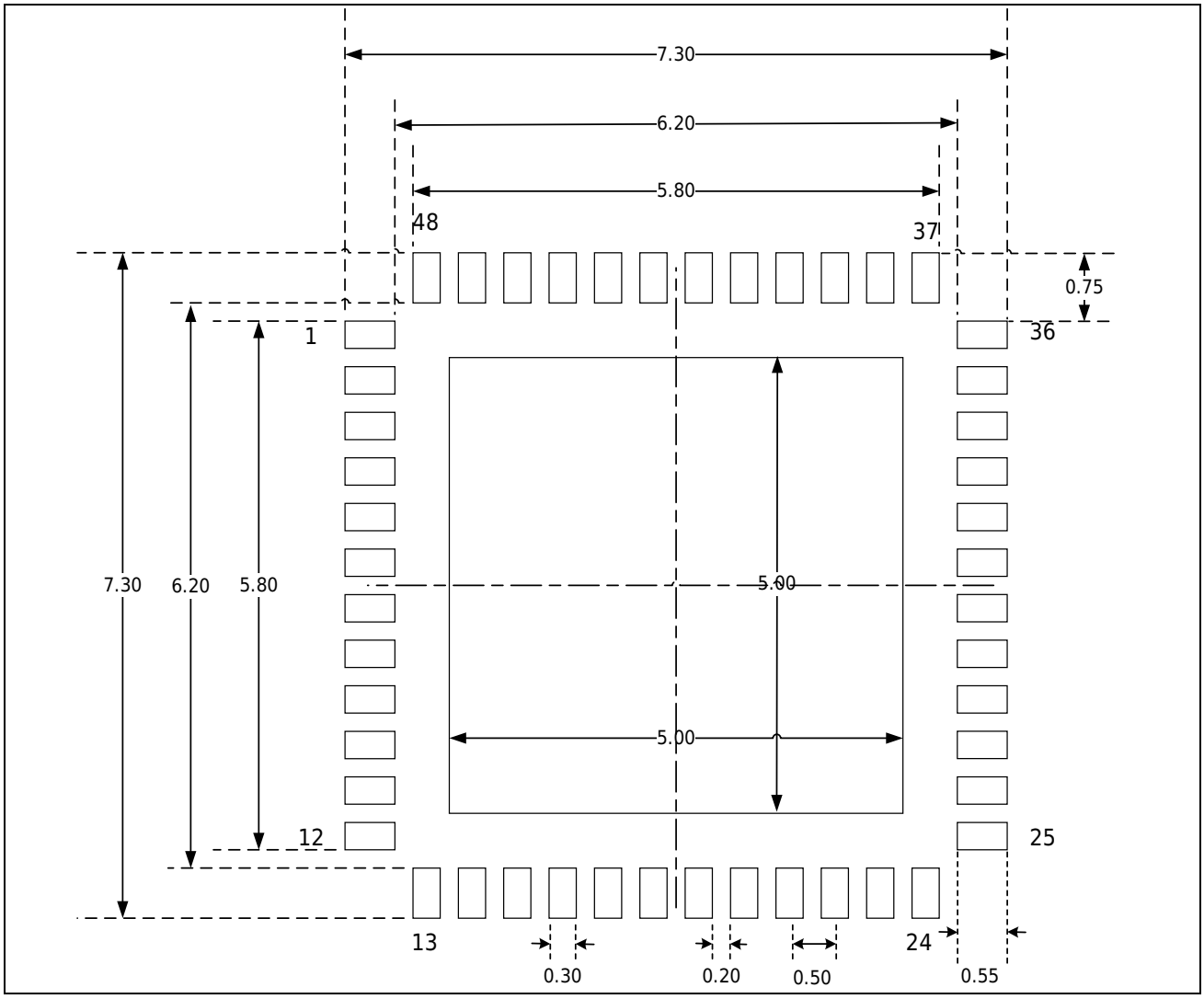
LQFP48 package (7mm x 7mm)



NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

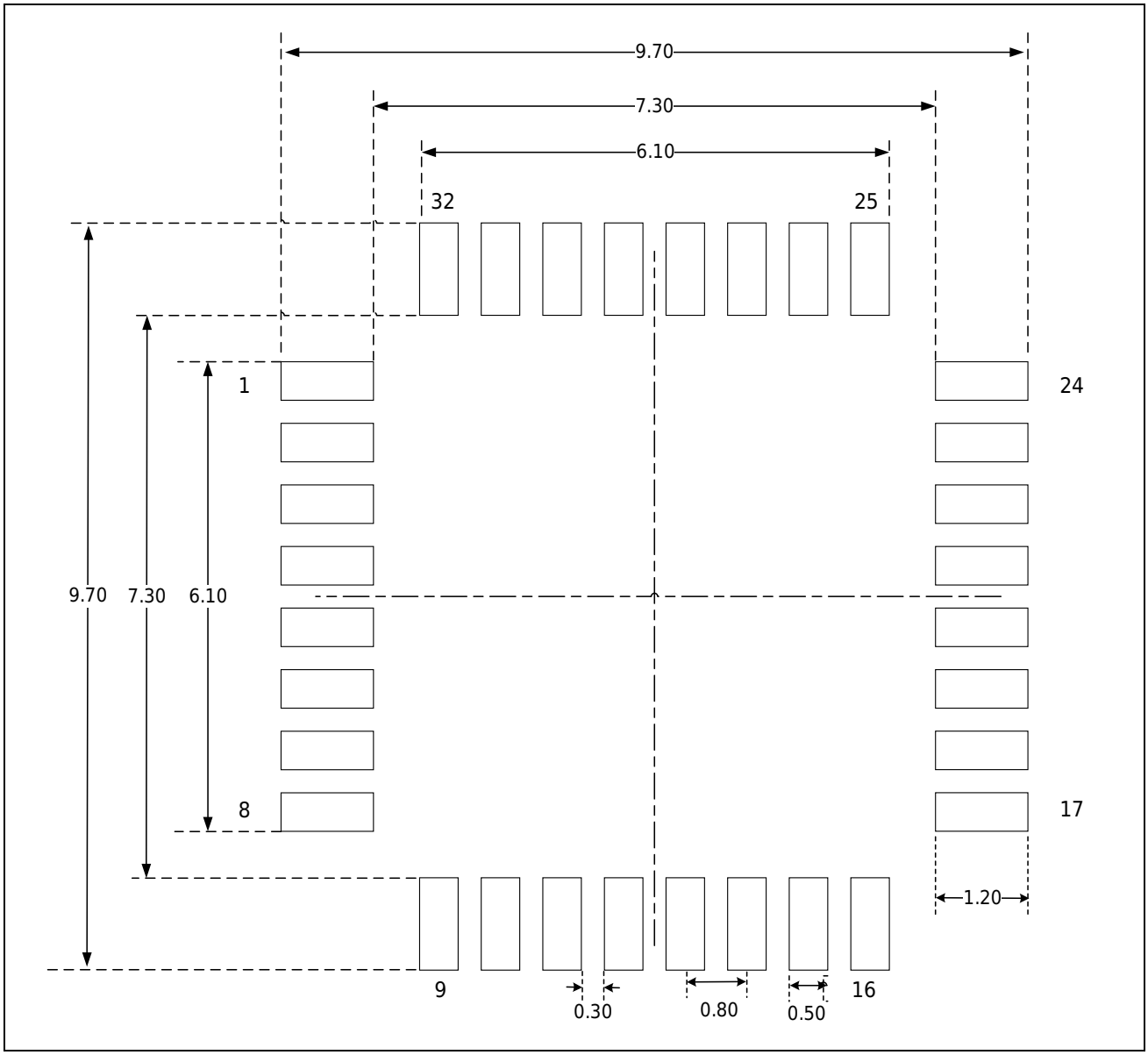
QFN48 package (7mm x 7mm)



NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

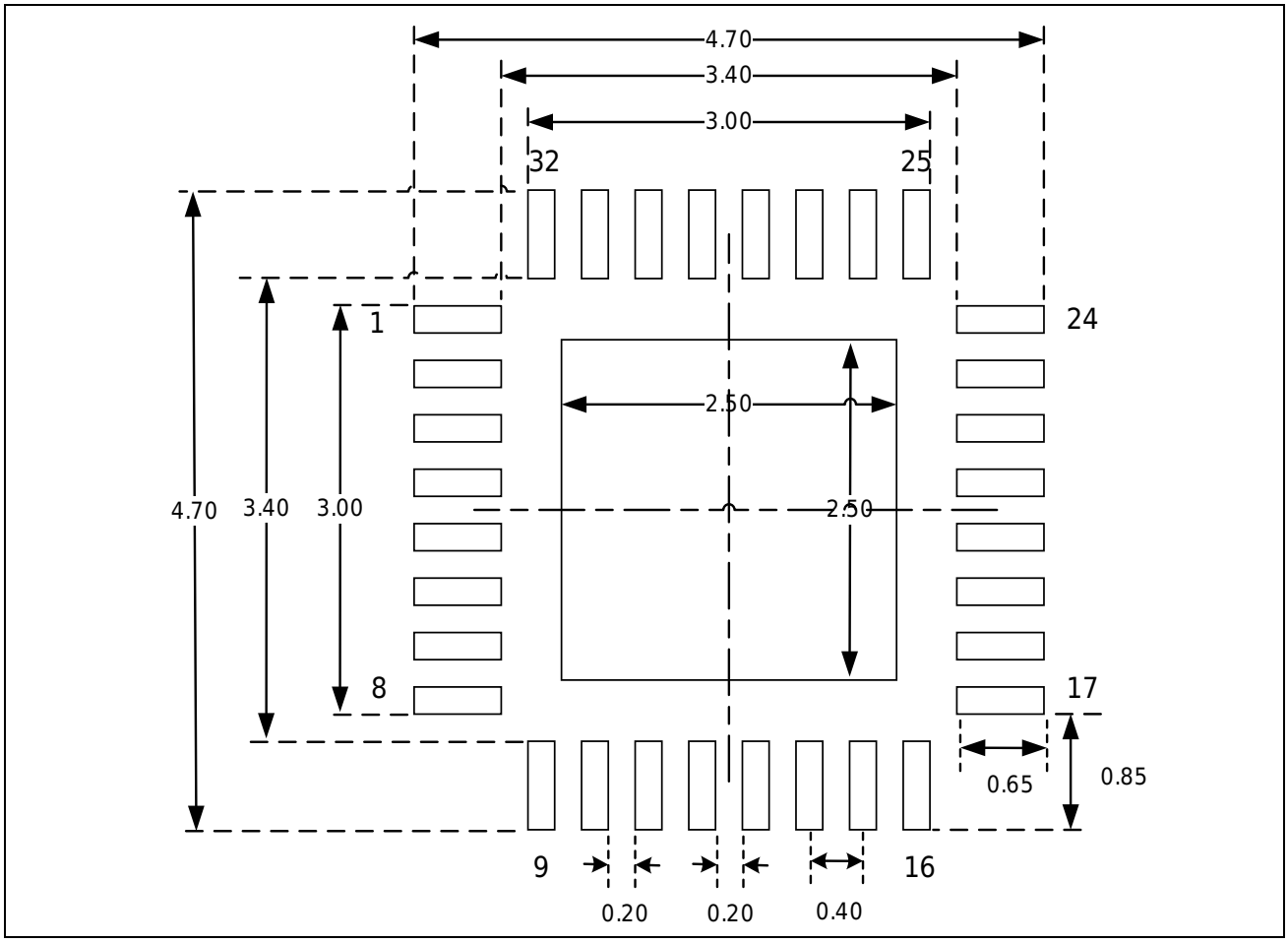
LQFP32 package (7mm x 7mm)



NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

QFN32 package (4mm x 4mm)



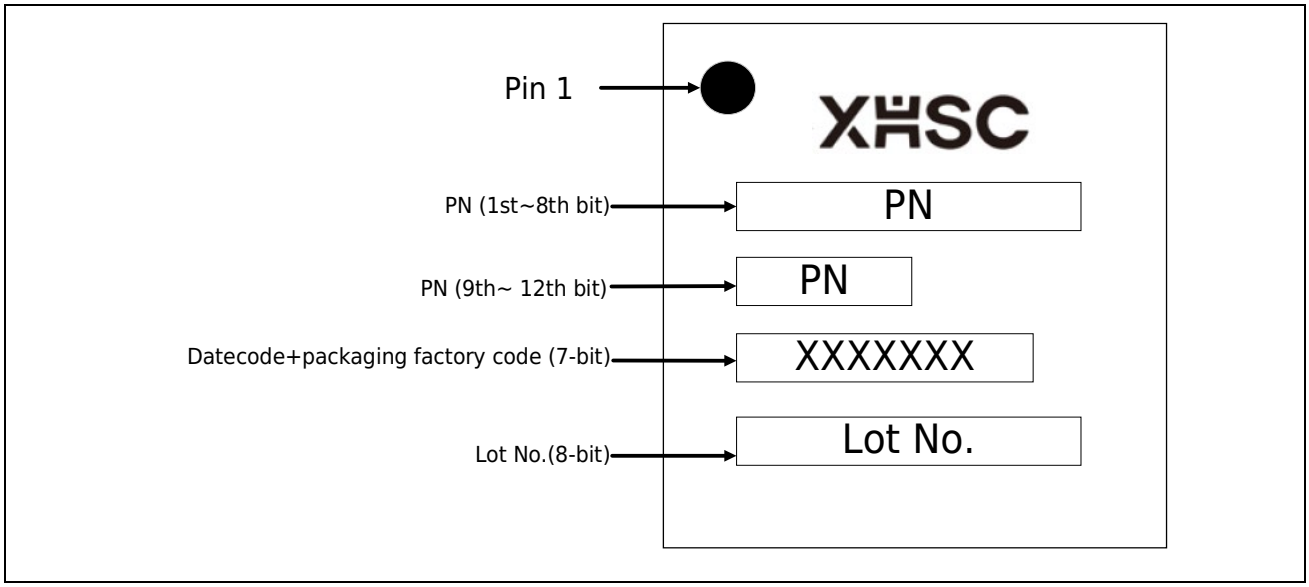
NOTE:

- *Dimensions are expressed in millimeters.*
- *Dimensions are for reference only.*

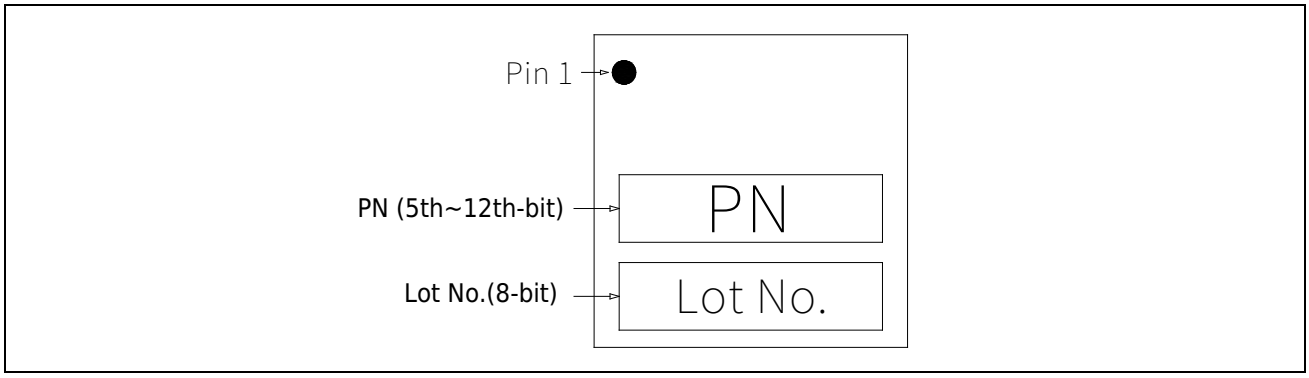
8.3 Silkscreen instructions

The position and information of Pin 1 printed on the front of each package are given below.

LQFP32/48 and QFN48 package (7mm x 7mm)



QFN32 package (4mm x 4mm)



Note:

– *The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.*

8.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j (℃) of the chip surface can be calculated according to the following formula:

$$T_j = T_{amb} + (P_D \times \theta_{JA})$$

- T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D is equal to the sum of internal power consumption of the chip and I/O power consumption, and the unit is W. The internal power consumption of the chip is the product's I_{DD} x V_{DD}. I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually this part of the value is very small and can be ignored.

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 8-1 Thermal resistance coefficient table for each package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP48 7 mm x 7 mm / 0.5 mm pitch	75 +/- 10%	℃/W
LQFP32 7 mm x 7 mm / 0.8 mm pitch	80 +/- 10%	℃/W
QFN48 7 mm x 7 mm / 0.5 mm pitch	30 +/- 10%	℃/W
QFN32 4 mm x 4 mm / 0.4 mm pitch	53 +/- 10%	℃/W

9 Ordering Information

Product Model	HC32F052 JATA-LQ48	HC32F052 JAUA-QFN48TR	HC32F052 FATA-LQ32	HC32F052 FAUA-QFN32TR	HC32F052 J8TA-LQ48	HC32F052 J8UA-QFN48TR	HC32F052 F8TA-LQ32	HC32F052 F8UA-QFN32TR
Main frequency (MHz)	64	64	64	64	64	64	64	64
Kernel	M0+	M0+	M0+	M0+	M0+	M0+	M0+	M0+
Flash (KB)	128	128	128	128	64	64	64	64
RAM (KB)	16	16	16	16	16	16	16	16
GPIO	40	40	26	26	40	40	26	26
Operating Voltage (V)	2.0~5.5	2.0~5.5	2.0~5.5	2.0~5.5	2.0~5.5	2.0~5.5	2.0~5.5	2.0~5.5
DMA	1*5 ch	1*5 ch	1*5 ch	1*5 ch	1*5 ch	1*5 ch	1*5 ch	1*5 ch
Low power timer	1	1	1	1	1	1	1	1
Basic timer (multiplexed)	6	6	6	6	6	6	6	6
Universal timer	2	2	2	2	2	2	2	2
Advanced timer	4	4	4	4	4	4	4	4
Real time clock timer	1	1	1	1	1	1	1	1
LPUART	2	2	1	1	2	2	1	1
USART	2	2	2	2	2	2	2	2
LIN	✓	✓	✓	✓	✓	✓	✓	✓
ISO7816	✓	✓	✓	✓	✓	✓	✓	✓
CAN	1	1	1	1	1	1	1	1
I2C	2	2	2	2	2	2	2	2
I2C SLV	1	1	1	1	1	1	1	1
SPI	2	2	1	1	2	2	1	1
ADC(12bit)	1*16 ch	1*16 ch	1*10 ch	1*10 ch	1*16 ch	1*16 ch	1*10 ch	1*10 ch

Product Model	HC32F052 JATA-LQ48	HC32F052 JAUA-QFN48TR	HC32F052 FATA-LQ32	HC32F052 FAUA-QFN32TR	HC32F052 J8TA-LQ48	HC32F052 J8UA-QFN48TR	HC32F052 F8TA-LQ32	HC32F052 F8UA-QFN32TR
OPA	2	2	0	0	2	2	0	0
VC	2	2	2	2	2	2	2	2
CRC	1	1	1	1	1	1	1	1
LVD	1	1	1	1	1	1	1	1
Working temperature (℃)	-40~85	-40~85	-40~85	-40~85	-40~85	-40~85	-40~85	-40~85
Encapsulation Form:	LQFP48(7*7)	QFN48(7*7)	LQFP32(7*7)	QFN32(4*4)	LQFP48(7*7)	QFN48(7*7)	LQFP32(7*7)	QFN32(4*4)
Foot Spacing	0.5 mm	0.5 mm	0.5 mm	0.4 mm	0.5 mm	0.5 mm	0.5 mm	0.4 mm
Product Thickness	1.6 mm	0.75 mm	1.6 mm	0.75 mm	1.6 mm	0.75 mm	1.6 mm	0.75 mm
Packing	Tray	Tape & Reel	Tray	Tape & Reel	Tray	Tape & Reel	Tray	Tape & Reel

Before ordering, please contact the sales window for the latest mass production information.

Version Revision History

Version Number	Revision Date	Modify the content
Rev1.0	2023/11/15	First edition release.