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**PART NUMBER****EP610LC-15-G-ROCV**

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**Rochester Electronics****Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

**Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level

**Qualified Suppliers List of Distributors (QSLD)**

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

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*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

## EP610-910-1810

### *Classic EPLD Family*

The Altera Classic™ device family offers a solution to high-speed, low-power logic integration. Fabricated on advanced CMOS technology, Classic devices also have a Turbo-only version, which is described in the data sheet.

Classic devices support 100% TTL emulation and can easily integrate multiple PAL- and GAL-type devices with densities ranging from 300 to 900 usable gates. The Classic family provides pin-to-pin logic delays as low as 10 ns and counter frequencies as high as 100 MHz. Classic devices are available in a wide range of packages, including ceramic dual in-line package (CerDIP), plastic dual in-line package (PDIP), plastic J-lead chip carrier (PLCC), ceramic J-lead chip carrier JLCC), pin-grid array (PGA), and small-outline integrated circuit (SOIC) packages.

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#### **FOR REFERENCE ONLY**

## **General Description**

The Altera Classic™ device family offers a solution to high-speed, low-power logic integration. Fabricated on advanced CMOS technology, Classic devices also have a Turbo-only version, which is described in this data sheet.

Classic devices support 100% TTL emulation and can easily integrate multiple PAL- and GAL-type devices with densities ranging from 300 to 900 usable gates. The Classic family provides pin-to-pin logic delays as low as 10 ns and counter frequencies as high as 100 MHz. Classic devices are available in a wide range of packages, including ceramic dual in-line package (CerDIP), plastic dual in-line package (PDIP), plastic J-lead chip carrier (PLCC), ceramic J-lead chip carrier (JLCC), pin-grid array (PGA), and small-outline integrated circuit (SOIC) packages.

EPROM-based Classic devices can reduce active power consumption without sacrificing performance. This reduced power consumption makes the Classic family well suited for a wide range of low-power applications.

Classic devices are 100% generically tested devices in windowed packages and can be erased with ultra-violet (UV) light, allowing design changes to be implemented quickly.

Classic devices use sum-of-products logic and a programmable register. The sum-of-products logic provides a programmable-AND/fixed-OR structure that can implement logic with up to eight product terms. The programmable register can be individually programmed for D, T, SR, or JK flipflop operation or can be bypassed for combinatorial operation. In addition, macrocell registers can be individually clocked either by a global clock or by any input or feedback path to the AND array. Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in both active-high and active-low modes. These features make it possible to implement a variety of logic functions simultaneously.

Classic devices are supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations. These devices also contain on-board logic test circuitry to allow verification of function and AC specifications during standard production flow.

# EP610-910-1810

## Rochester Ordering Guide

*\*Most products can also be offered as RoHS compliant, designated by a -G suffix. Please contact factory for more information.*

| Rochester Part Number | Altera Part Number | Package          | Temperature    |
|-----------------------|--------------------|------------------|----------------|
| EP600DI-25            | EP600DI-25         | CDIP-24          | -40° to +85°C  |
| EP600DI-25T           | EP600DI-25T        | CDIP-24          | -40° to +85°C  |
| EP600DI-30            | EP600DI-30         | CDIP-24          | -40° to +85°C  |
| EP600DI-35            | EP600DI-35         | CDIP-24          | -40° to +85°C  |
| EP600DI-45            | EP600DI-45         | CDIP-24          | -40° to +85°C  |
| EP600DM-25/B          | EP600DM-25/B       | CDIP-24          | -55° to +125°C |
| EP600DM-25T/B         | EP600DM-25T/B      | CDIP-24          | -55° to +125°C |
| EP600DM-30/B          | EP600DM-30/B       | CDIP-24          | -55° to +125°C |
| EP600DM-35/B          | EP600DM-35/B       | CDIP-24          | -55° to +125°C |
| EP600DM-45/B          | EP600DM-45/B       | CDIP-24          | -55° to +125°C |
| EP600IDC-25           | EP600IDC-25        | CDIP-24          | 0° to +70°C    |
| EP600IDC-30           | EP600IDC-30        | CDIP-24          | 0° to +70°C    |
| EP600IDC-35           | EP600IDC-35        | CDIP-24          | 0° to +70°C    |
| EP600IDC-45           | EP600IDC-45        | CDIP-24          | 0° to +70°C    |
| EP600ILC-45           | EP600ILC-45        | LDCC-28, Plastic | 0° to +70°C    |
| EP600IPC-25           | EP600IPC-25        | PDIP-24          | 0° to +70°C    |
| EP600IPC-30           | EP600IPC-30        | PDIP-24          | 0° to +70°C    |
| EP600IPC-35           | EP600IPC-35        | PDIP-24          | 0° to +70°C    |
| EP600IPC-45           | EP600IPC-45        | PDIP-24          | 0° to +70°C    |
| EP600IPC-45           | EP600IPC-45        | PDIP-24          | 0° to +70°C    |
| EP600IPC-45AB         | EP600IPC-45AB      | PDIP-24          | 0° to +70°C    |
| EP610DC-25            | EP610DC-25         | CDIP-24          | 0° to +70°C    |
| EP610DC-30            | EP610DC-30         | CDIP-24          | 0° to +70°C    |
| EP610DC-35            | EP610DC-35         | CDIP-24          | 0° to +70°C    |
| EP610DC-35AA          | EP610DC-35AA       | CDIP-24          | 0° to +70°C    |
| EP610DC-45            | EP610DC-45         | CDIP-24          | 0° to +70°C    |
| EP610DI-15            | EP610DI-15         | CDIP-24          | -40° to +85°C  |
| EP610DI-20            | EP610DI-20         | CDIP-24          | -40° to +85°C  |
| EP610DI-25            | EP610DI-25         | CDIP-24          | -40° to +85°C  |
| EP610DI-25T           | EP610DI-25T        | CDIP-24          | -40° to +85°C  |
| EP610DI-30            | EP610DI-30         | CDIP-24          | -40° to +85°C  |
| EP610DI-35            | EP610DI-35         | CDIP-24          | -40° to +85°C  |
| EP610DM-25            | EP610DM-25         | CDIP-24          | -55° to +125°C |
| EP610DM-25T           | EP610DM-25T        | CDIP-24          | -55° to +125°C |
| EP610DM-30            | EP610DM-30         | CDIP-24          | -55° to +125°C |
| EP610DM-35            | EP610DM-35         | CDIP-24          | -55° to +125°C |
| EP610DM-35/B          | EP610DM-35/B       | CDIP-24          | -55° to +125°C |
| EP610DM-25/R          | EP610DM-25/R       | CDIP-24          | -55° to +125°C |
| EP610DM-25T/R         | EP610DM-25T/R      | CDIP-24          | -55° to +125°C |
| EP610DM-30/R          | EP610DM-30/R       | CDIP-24          | -55° to +125°C |
| EP610DM-35/R          | EP610DM-35/R       | CDIP-24          | -55° to +125°C |
| EP610LC-15            | EP610LC-15         | LDCC-28, Plastic | 0° to +70°C    |
| EP610LC-20            | EP610LC-20         | LDCC-28, Plastic | 0° to +70°C    |
| EP610LC-20T           | EP610LC-20T        | LDCC-28, Plastic | 0° to +70°C    |
| EP610LC-25            | EP610LC-25         | LDCC-28, Plastic | 0° to +70°C    |
| EP610LC-35            | EP610LC-35         | LDCC-28, Plastic | 0° to +70°C    |
| EP610LC-45            | EP610LC-45         | LDCC-28, Plastic | 0° to +70°C    |

# EP610-910-1810

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| Rochester Part Number | Altera Part Number | Package          | Temperature   |
|-----------------------|--------------------|------------------|---------------|
| EP610LI-15            | EP610LI-15         | LDCC-28, Plastic | -40° to +85°C |
| EP610LI-20            | EP610LI-20         | LDCC-28, Plastic | -40° to +85°C |
| EP610LI-20T           | EP610LI-20T        | LDCC-28, Plastic | -40° to +85°C |
| EP610LI-25            | EP610LI-25         | LDCC-28, Plastic | -40° to +85°C |
| EP610LI-35            | EP610LI-35         | LDCC-28, Plastic | -40° to +85°C |
| EP610LI-45            | EP610LI-45         | LDCC-28, Plastic | -40° to +85°C |
| EP610PC-15            | EP610PC-15         | PDIP-24          | 0° to +70°C   |
| EP610PC-20            | EP610PC-20         | PDIP-24          | 0° to +70°C   |
| EP610PC-20T           | EP610PC-20T        | PDIP-24          | 0° to +70°C   |
| EP610PC-25            | EP610PC-25         | PDIP-24          | 0° to +70°C   |
| EP610PC-25T           | EP610PC-25T        | PDIP-24          | 0° to +70°C   |
| EP610PC-30            | EP610PC-30         | PDIP-24          | 0° to +70°C   |
| EP610PC-35            | EP610PC-35         | PDIP-24          | 0° to +70°C   |
| EP610PC-45            | EP610PC-45         | PDIP-24          | 0° to +70°C   |
| EP610PI-15            | EP610PI-15         | PDIP-24          | -40° to +85°C |
| EP610PI-20            | EP610PI-20         | PDIP-24          | -40° to +85°C |
| EP610PI-25            | EP610PI-25         | PDIP-24          | -40° to +85°C |
| EP610PI-30            | EP610PI-30         | PDIP-24          | -40° to +85°C |
| EP610PI-35            | EP610PI-35         | PDIP-24          | -40° to +85°C |
| EP610PI-45            | EP610PI-45         | PDIP-24          | -40° to +85°C |
| EP610SC-15            | EP610SC-15         | SOP-24, Plastic  | 0° to +70°C   |
| EP610SC-20            | EP610SC-20         | SOP-24, Plastic  | 0° to +70°C   |
| EP610SC-25            | EP610SC-25         | SOP-24, Plastic  | 0° to +70°C   |
| EP610SI-25            | EP610SI-25         | SOP-24, Plastic  | -40° to +85°C |
| EP610SI-30            | EP610SI-30         | SOP-24, Plastic  | -40° to +85°C |
| EP610SI-35            | EP610SI-35         | SOP-24, Plastic  | -40° to +85°C |
| EP610SI-45            | EP610SI-45         | SOP-24, Plastic  | -40° to +85°C |
| EP900ILC-50           | EP900ILC-50        | LDCC-44, Plastic | 0° to +70°C   |
| EP900ILC-50H          | EP900ILC-50H       | LDCC-44, Plastic | 0° to +70°C   |
| EP900IPC-50           | EP900IPC-50        | PDIP-40          | 0° to +70°C   |
| EP910DC-25            | EP910DC-25         | CDIP-40          | 0° to +70°C   |
| EP910DC-30            | EP910DC-30         | CDIP-40          | 0° to +70°C   |
| EP910DC-35            | EP910DC-35         | CDIP-40          | 0° to +70°C   |
| EP910DC-45            | EP910DC-45         | CDIP-40          | 0° to +70°C   |
| EP910DI-12            | EP910DI-12         | CDIP-40          | -40° to +85°C |
| EP910DI-15            | EP910DI-15         | CDIP-40          | -40° to +85°C |
| EP910DI-25            | EP910DI-25         | CDIP-40          | -40° to +85°C |
| EP910DI-30            | EP910DI-30         | CDIP-40          | -40° to +85°C |
| EP910DI-35            | EP910DI-35         | CDIP-40          | -40° to +85°C |
| EP910DI-40            | EP910DI-40         | CDIP-40          | -40° to +85°C |
| EP910DI-50            | EP910DI-50         | CDIP-40          | -40° to +85°C |
| EP910IDC-15           | EP910IDC-15        | CDIP-40          | 0° to +70°C   |
| EP910IDI-15           | EP910IDI-15        | CDIP-40          | -40° to +85°C |
| EP910ILC-12           | EP910ILC-12        | LDCC-44, Plastic | 0° to +70°C   |
| EP910ILC-12H          | EP910ILC-12H       | LDCC-44, Plastic | 0° to +70°C   |
| EP910ILC-15           | EP910ILC-15        | LDCC-44, Plastic | 0° to +70°C   |

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| Rochester Part Number | Altera Part Number | Package          | Temperature   |
|-----------------------|--------------------|------------------|---------------|
| EP910ILC-15H          | EP910ILC-15H       | LDCC-44, Plastic | 0° to +70°C   |
| EP910ILI-12           | EP910ILI-12        | LDCC-44, Plastic | -40° to +85°C |
| EP910IPC-12           | EP910IPC-12        | PDIP-40          | 0° to +70°C   |
| EP910IPC-25           | EP910IPC-25        | PDIP-40          | 0° to +70°C   |
| EP910LC-30            | EP910LC-30         | LDCC-44, Plastic | 0° to +70°C   |
| EP910LC-30T           | EP910LC-30T        | LDCC-44, Plastic | 0° to +70°C   |
| EP910LC-35            | EP910LC-35         | LDCC-44, Plastic | 0° to +70°C   |
| EP910LC-35H           | EP910LC-35H        | LDCC-44, Plastic | 0° to +70°C   |
| EP910LC-40            | EP910LC-40         | LDCC-44, Plastic | 0° to +70°C   |
| EP910LC-40H           | EP910LC-40H        | LDCC-44, Plastic | 0° to +70°C   |
| EP910LI-12            | EP910LI-12         | LDCC-44, Plastic | -40° to +85°C |
| EP910LI-15            | EP910LI-15         | LDCC-44, Plastic | -40° to +85°C |
| EP910LI-25            | EP910LI-25         | LDCC-44, Plastic | -40° to +85°C |
| EP910LI-30            | EP910LI-30         | LDCC-44, Plastic | -40° to +85°C |
| EP910LI-35            | EP910LI-35         | LDCC-44, Plastic | -40° to +85°C |
| EP910LI-40            | EP910LI-40         | LDCC-44, Plastic | -40° to +85°C |
| EP910LI-50            | EP910LI-50         | LDCC-44, Plastic | -40° to +85°C |
| EP910PC-30            | EP910PC-30         | PDIP-40          | 0° to +70°C   |
| EP910PI-12            | EP910PI-12         | PDIP-40          | -40° to +85°C |
| EP910PI-15            | EP910PI-15         | PDIP-40          | -40° to +85°C |
| EP910PI-25            | EP910PI-25         | PDIP-40          | -40° to +85°C |
| EP910PI-30            | EP910PI-30         | PDIP-40          | -40° to +85°C |
| EP910PI-35            | EP910PI-35         | PDIP-40          | -40° to +85°C |
| EP910PI-40            | EP910PI-40         | PDIP-40          | -40° to +85°C |
| EP910PI-50            | EP910PI-50         | PDIP-40          | -40° to +85°C |
| EP1810GC-35           | EP1810GC-35        | PGA-68, Ceramic  | 0° to +70°C   |
| EP1810GC-45           | EP1810GC-45        | PGA-68, Ceramic  | 0° to +70°C   |
| EP1810GC-70           | EP1810GC-70        | PGA-68, Ceramic  | 0° to +70°C   |
| EP1810GI-35           | EP1810GI-35        | PGA-68, Ceramic  | -40° to +85°C |
| EP1810GI-45           | EP1810GI-45        | PGA-68, Ceramic  | -40° to +85°C |
| EP1810GI-70           | EP1810GI-70        | PGA-68, Ceramic  | -40° to +85°C |
| EP1810LC-45           | EP1810LC-45        | LDCC-68, Plastic | 0° to +70°C   |
| EP1810LC-45AA         | EP1810LC-45AA      | LDCC-68, Plastic | 0° to +70°C   |
| EP1810LC-45H          | EP1810LC-45H       | LDCC-68, Plastic | 0° to +70°C   |
| EP1810LC-70           | EP1810LC-70        | LDCC-68, Plastic | 0° to +70°C   |
| EP1810LI-35           | EP1810LI-35        | LDCC-68, Plastic | -40° to +85°C |
| EP1810LI-45           | EP1810LI-45        | LDCC-68, Plastic | -40° to +85°C |
| EP1810LI-70           | EP1810LI-70        | LDCC-68, Plastic | -40° to +85°C |

## Functional Description

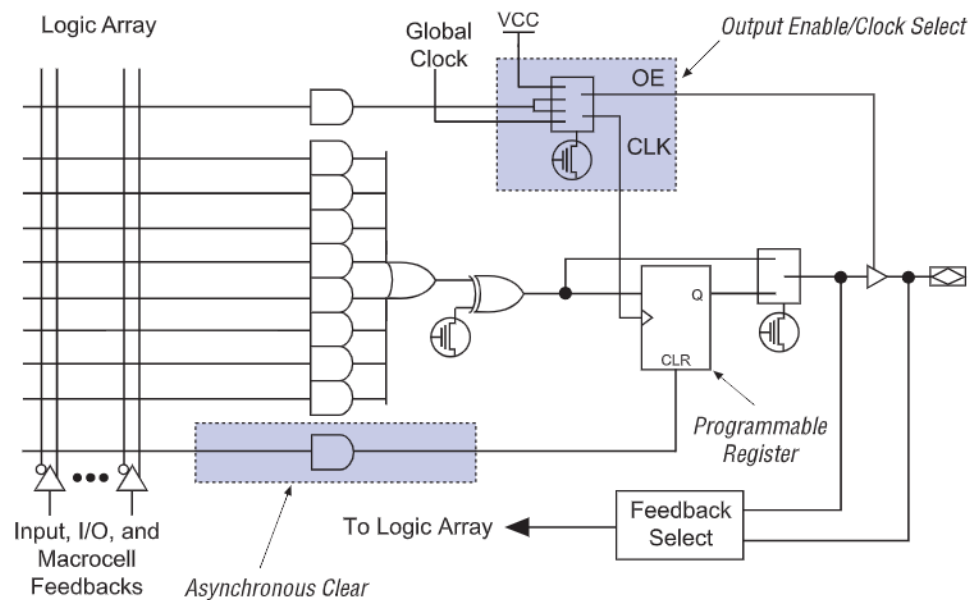
The Classic architecture includes the following elements:

- Macrocells
- Programmable registers
- Output enable/clock select
- Feedback select

### Macrocells

Classic macrocells, shown in [Figure 1](#), can be individually configured for both sequential and combinatorial logic operation. Eight product terms form a programmable-AND array that feeds an OR gate for combinatorial logic implementation. An additional product term is used for asynchronous clear control of the internal register; another product term implements either an output enable or a logic-array-generated clock. Inputs to the programmable-AND array come from both the true and complement signals of the dedicated inputs, feedbacks from I/O pins that are configured as inputs, and feedbacks from macrocell outputs. Signals from dedicated inputs are globally routed and can feed the inputs of all device macrocells. The feedback multiplexer controls the routing of feedback signals from macrocells and from I/O pins.

**Figure 1. Classic Device Macrocell**



The eight product terms of the programmable-AND array feed the 8-input OR gate, which then feeds one input to an XOR gate. The other input to the XOR gate is connected to a programmable bit that allows the array output to be inverted. Altera's MAX+PLUS II software uses the XOR gate to implement either active-high or active-low logic, or De Morgan's inversion to reduce the number of product terms needed to implement a function.

### Programmable Registers

To implement registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation. If necessary, the register can be bypassed for combinatorial operation. During design compilation, the MAX+PLUS II software selects the most efficient register operation for each registered function to minimize the logic resources needed by the design. Registers have an individual asynchronous clear function that is controlled by a dedicated product term. These registers are cleared automatically during power-up.

In addition, macrocell registers can be individually clocked by either a global clock or any input or feedback path to the AND array. Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in both active-high and active-low modes. These features make it possible to simultaneously implement a variety of logic functions.

### Output Enable/Clock Select

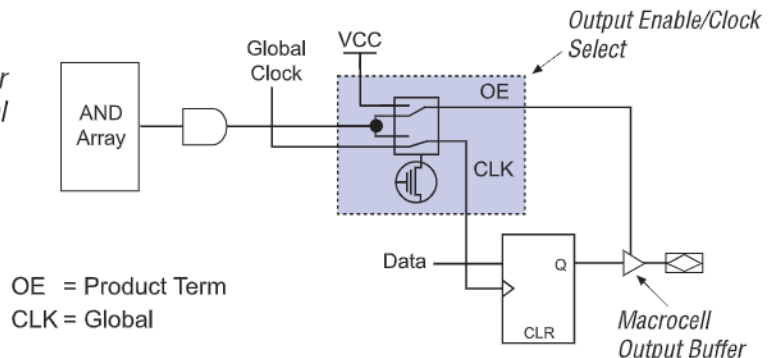
**Figure 2** shows the two operating modes (Modes 0 and 1) provided by the output enable/clock (OE/CLK) select. The OE/CLK select, which is controlled by a single programmable bit, can be individually configured for each macrocell. In Mode 0, the tri-state output buffer is controlled by a single product term. If the output enable is high, the output buffer is enabled. If the output enable is low, the output has a high-impedance value. In Mode 0, the macrocell flipflop is clocked by its global clock input signal.

In Mode 1, the output enable buffer is always enabled, and the macrocell register can be triggered by an array clock signal generated by a product term. This mode allows registers to be individually clocked by any signal on the AND array. With both true and complement signals in the AND array, the register can be configured to trigger on a rising or falling edge. This product-term-controlled clock configuration also supports gated clock structures.

**Figure 2. Classic Output Enable/Clock Select**

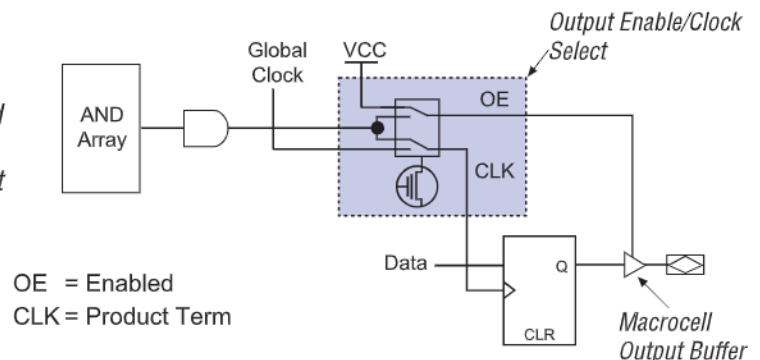
## Mode 0

*In Mode 0, the register is clocked by the global clock signal. The output is enabled by the logic from the product term.*



## Mode 1

*In Mode 1, the output is permanently enabled and the register is clocked by the product term, which allows gated clocks to be generated.*



## Feedback Select

Each macrocell in a Classic device provides feedback selection that is controlled by the feedback multiplexer. This feedback selection allows the designer to feed either the macrocell output or the I/O pin input associated with the macrocell back into the AND array. The macrocell output can be either the Q output of the programmable register or the combinatorial output of the macrocell. Different devices have different feedback multiplexer configurations. See [Figure 3](#).

**Figure 3. Classic Feedback Multiplexer Configurations**

### Global Feedback Multiplexer



### Quadrant Feedback Multiplexer



### Dual Feedback Multiplexer



EP610, EP610I, EP910, and EP910I devices have a global feedback configuration; either the macrocell output (Q) or the I/O pin input (I/O) can feed back to the AND array so that it is accessible to all other macrocells.

EP1810 macrocells can have either of two feedback configurations: quadrant or dual. Most macrocells in EP1810 devices have a quadrant feedback configuration; either the macrocell output or I/O pin input can feed back to other macrocells in the same quadrant. Selected macrocells in EP1810 devices have a dual feedback configuration: the output of the macrocell feeds back to other macrocells in the same quadrant, and the I/O pin input feeds back to all macrocells in the device. If the associated I/O pin is not used, the macrocell output can optionally feed all macrocells in the device. In this case, the output of the macrocell passes through the tri-state buffer and uses the feedback path between the buffer and the I/O pin.

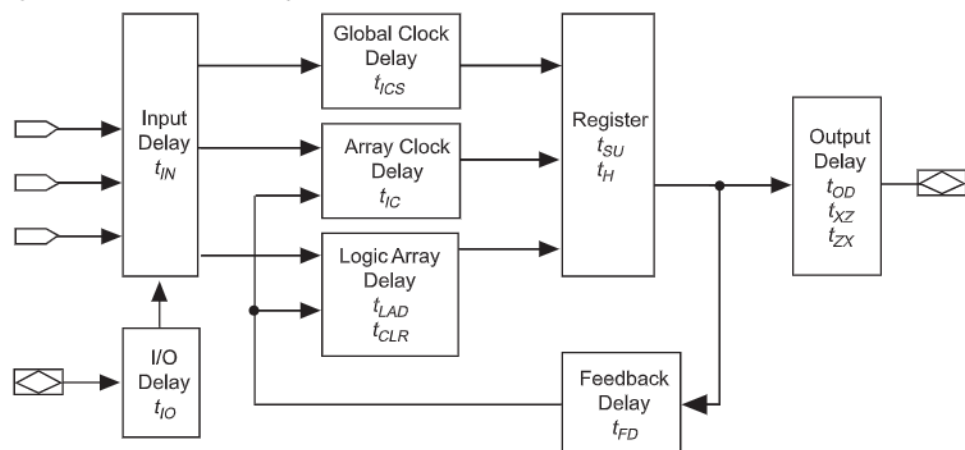
## Design Security

Classic devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because data within configuration elements is invisible. The security bit that controls this function and other program data is reset only when the device is erased.

## Timing Model

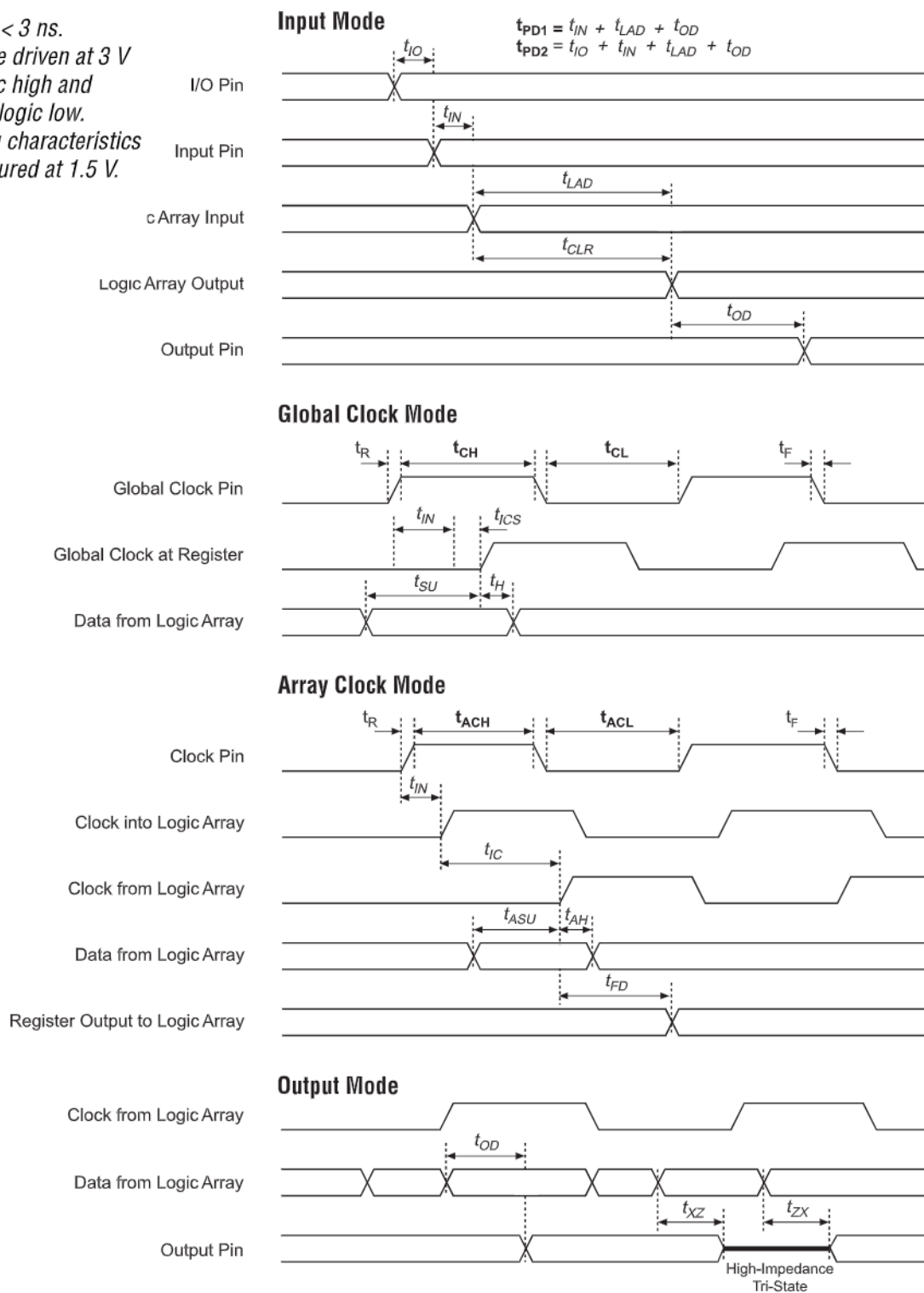
Device timing can be analyzed with the MAX+PLUS II software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 4. Devices have fixed internal delays that allow the user to determine the worst-case timing for any design. The MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

**Figure 4. Classic Timing Model**



**Figure 5. Classic Switching Waveforms**

$t_R$  and  $t_F < 3$  ns.  
Inputs are driven at 3 V  
for a logic high and  
0 V for a logic low.  
All timing characteristics  
are measured at 1.5 V.



## Turbo Bit Option

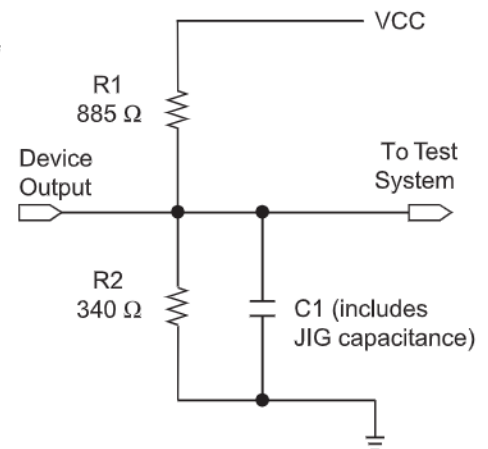
Many Classic devices contain a programmable Turbo Bit™ option to control the automatic power-down feature that enables the low-standby-power mode. When the Turbo Bit option is turned on, the low-standby-power mode is disabled. All AC values are tested with the Turbo Bit option turned on. When the device is operating with the Turbo Bit option turned off (non-Turbo mode), a non-Turbo adder must be added to the appropriate AC parameter to determine worst-case timing. The non-Turbo adder is specified in the “AC Operating Conditions” tables for each Classic device that supports the Turbo mode.

## Generic Testing

Classic devices are fully functionally tested. Complete testing of each programmable EPROM configuration element and all internal logic elements before and after packaging ensures 100% programming yield. See Figure 6 for AC test measurement conditions. These devices also contain on-board logic test circuitry to allow verification of function and AC specifications during standard production flow.

**Figure 6. AC Test Conditions**

*Power-supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.*



## Device Programming

Classic devices can be programmed on 486- and Pentium-based PCs with the MAX+PLUS II Programmer, an Altera Logic Programmer card, the MPU, and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.



### *Notes:*

Rochester EPLD devices normally sold in the un-configured state are tested using the original manufacturer's test software to guarantee the data sheet specifications. In some cases, EPLD devices can be configured to the customer's design and fully tested as such.

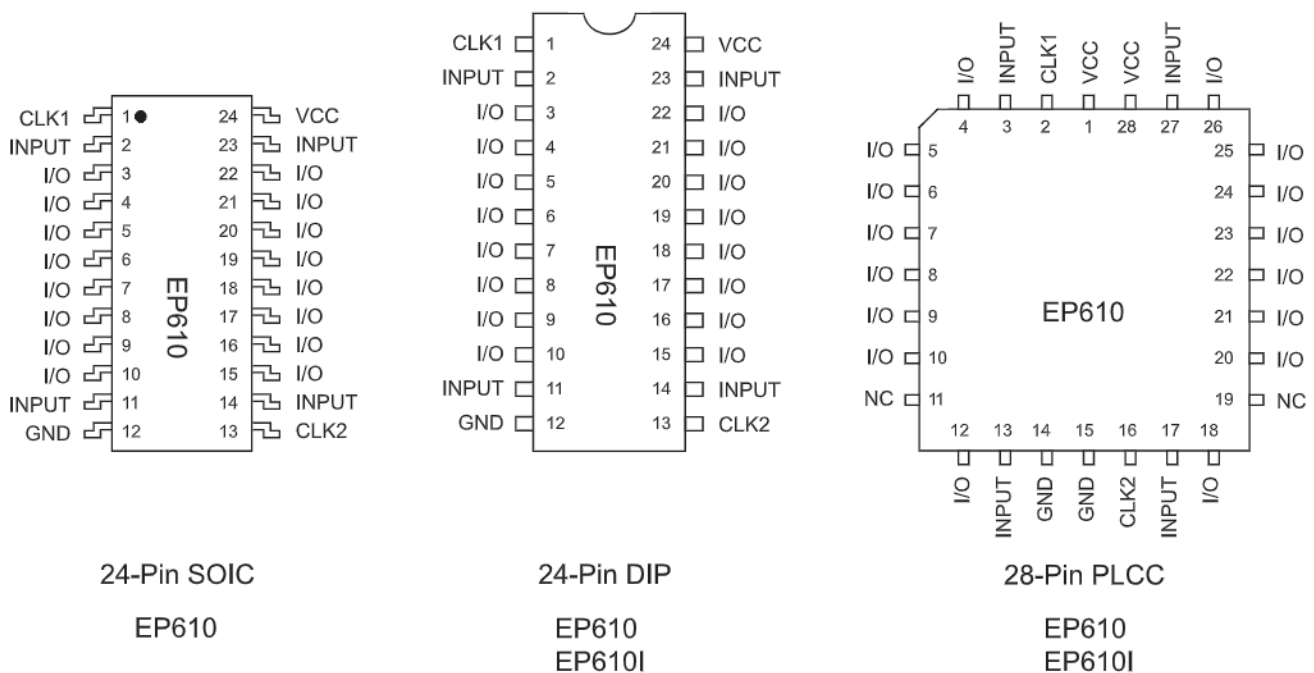
# EP610 EPLD

## Features

- High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with  $t_{PD}$  as fast as 10 ns
  - Counter frequencies of up to 100 MHz
  - Pipelined data rates of up to 125 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs and 2 clock pins
- EP610 and EP610I devices are pin-, function-, and programming file-compatible
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in the following packages (see [Figure 7](#)):
  - 24-pin small-outline integrated circuit (plastic SOIC only)
  - 24-pin ceramic and plastic dual in-line package (CerDIP and PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

**Figure 7. EP610 Package Pin-Out Diagrams**

*Package outlines not drawn to scale. Windows in ceramic packages only.*



## General Description

EP610 devices have 16 macrocells, 4 dedicated input pins, 16 I/O pins, and 2 global clock pins (see Figure 8). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. The CLK1 signal is a dedicated global clock input for the registers in macrocells 9 through 16. The CLK2 signal is a dedicated global clock input for registers in macrocells 1 through 8.

**Figure 8. EP610 Block Diagram**

Numbers without parentheses are for DIP and SOIC packages. Numbers in parentheses are for J-lead packages.

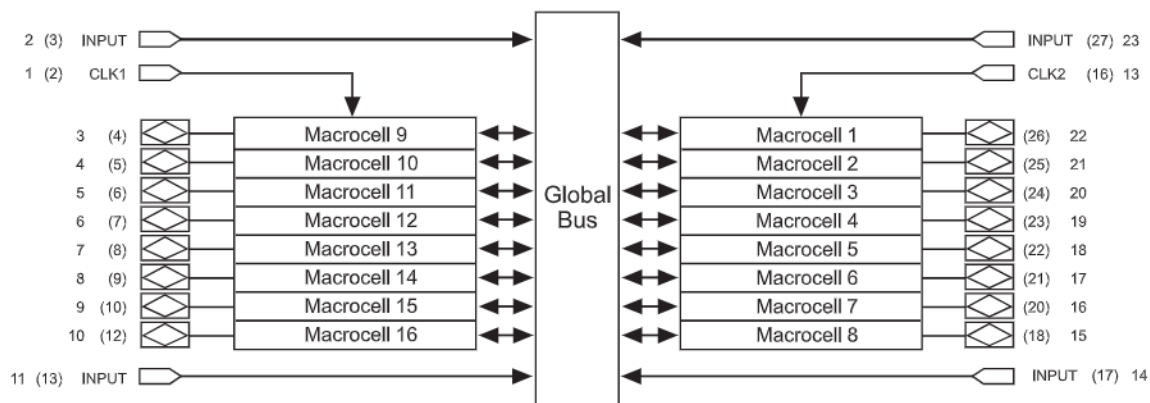
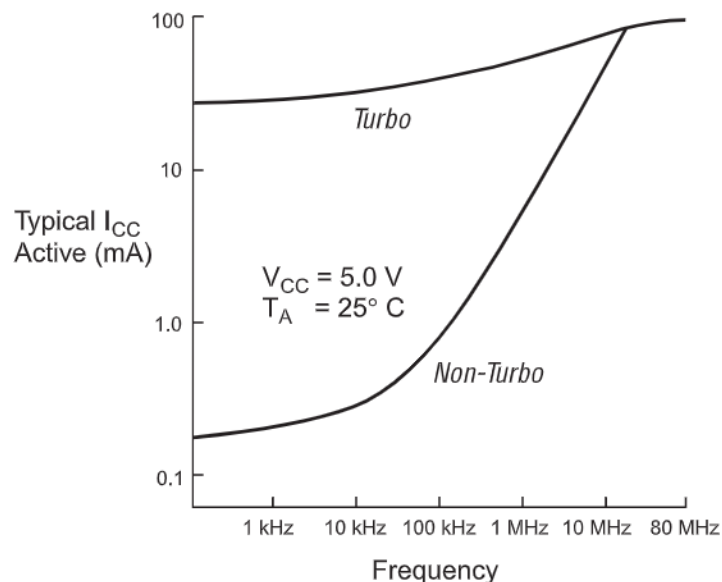


Figure 9 shows the typical supply current ( $I_{CC}$ ) versus frequency of EP610 devices.

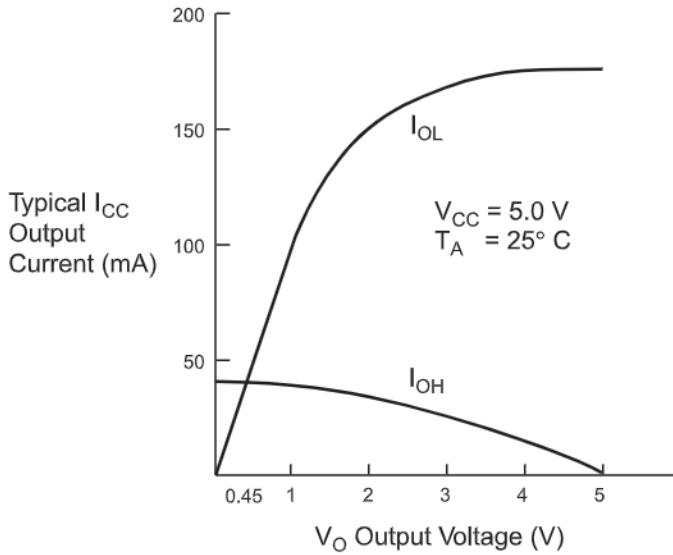
**Figure 9.  $I_{CC}$  vs. Frequency of EP610 Devices**



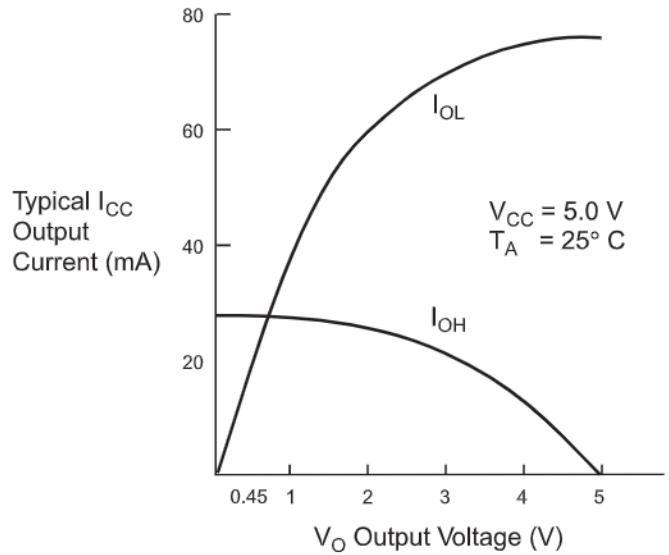
**Figure 10. Output Drive Characteristics of EP610 Devices**

*Drive characteristics may exceed shown curves.*

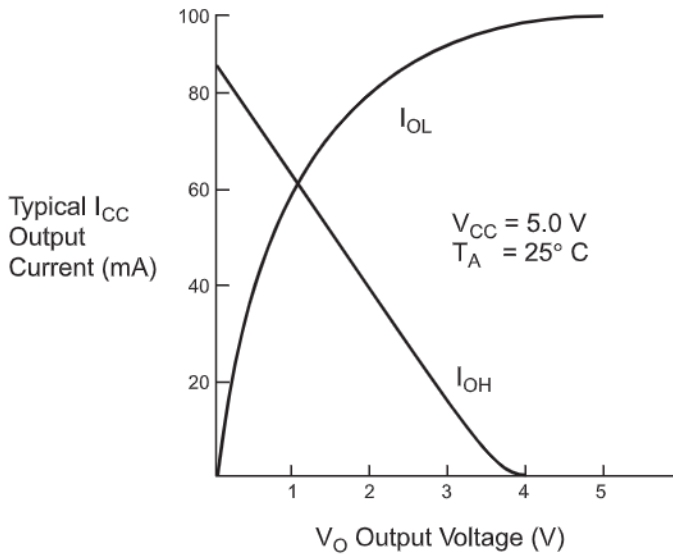
**EP610-15 & EP610-20 EPLDs**



**EP610-25, EP610-30 & EP610-35 EPLDs**



**EP610I EPLDs**



## Operating Conditions

Tables 2 through 7 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for EP610 and EP610I devices.

**Table 2. EP610 & EP610I Device Absolute Maximum Ratings** Note (1)

| Symbol    | Parameter                     | Conditions                   | EP610 |     | EP610I |                | Unit |
|-----------|-------------------------------|------------------------------|-------|-----|--------|----------------|------|
|           |                               |                              | Min   | Max | Min    | Max            |      |
| $V_{CC}$  | Supply voltage                | With respect to ground (2)   | -2.0  | 7.0 | -2.0   | 7.0            | V    |
| $V_I$     | DC input voltage              |                              | -2.0  | 7.0 | -0.5   | $V_{CC} + 0.5$ | V    |
| $I_{MAX}$ | DC $V_{CC}$ or ground current |                              | -175  | 175 |        |                | mA   |
| $I_{OUT}$ | DC output current, per pin    |                              | -25   | 25  |        |                | mA   |
| $T_{STG}$ | Storage temperature           | No bias                      | -65   | 150 | -65    | 150            | ° C  |
| $T_{AMB}$ | Ambient temperature           | Under bias                   | -65   | 135 | -65    | 135            | ° C  |
| $T_J$     | Junction temperature          | Ceramic packages, under bias |       | 150 |        | 150            | ° C  |
|           |                               | Plastic packages, under bias |       | 135 |        | 135            | ° C  |

**Table 3. EP610 & EP610I Device Recommended Operating Conditions** Note (1)

| Symbol   | Parameter             | Conditions         | EP610      |                | EP610I |                | Unit |
|----------|-----------------------|--------------------|------------|----------------|--------|----------------|------|
|          |                       |                    | Min        | Max            | Min    | Max            |      |
| $V_{CC}$ | Supply voltage        | (3)                | 4.75 (4.5) | 5.25 (5.5)     | 4.75   | 5.25           | V    |
| $V_I$    | Input voltage         |                    | -0.3       | $V_{CC} + 0.3$ | -0.3   | $V_{CC} + 0.3$ | V    |
| $V_O$    | Output voltage        |                    | 0          | $V_{CC}$       | 0      | $V_{CC}$       | V    |
| $T_A$    | Operating temperature | For commercial use | 0          | 70             | 0      | 70             | ° C  |
|          |                       | For industrial use | -40        | 85             | -40    | 85             | ° C  |
| $t_R$    | Input rise time       | (4)                |            | 100 (50)       |        | 500            | ns   |
| $t_F$    | Input fall time       | (4)                |            | 100 (50)       |        | 500            | ns   |

**Table 4. EP610 & EP610I Device DC Operating Conditions** Note (5)

| Symbol   | Parameter                                       | Conditions                     | Min  | Max            | Unit |
|----------|-------------------------------------------------|--------------------------------|------|----------------|------|
| $V_{IH}$ | High-level input voltage                        |                                | 2.0  | $V_{CC} + 0.3$ | V    |
| $V_{IL}$ | Low-level input voltage                         |                                | -0.3 | 0.8            | V    |
| $V_{OH}$ | High-level TTL output voltage                   | $I_{OH} = -4$ mA DC (6)        | 2.4  |                | V    |
|          | High-level CMOS output voltage                  | $I_{OH} = -0.6$ mA DC (6), (7) | 3.84 |                | V    |
| $V_{OL}$ | Low-level output voltage                        | $I_{OL} = 4$ mA DC (6)         |      | 0.45           | V    |
| $I_I$    | I/O pin leakage current of dedicated input pins | $V_I = V_{CC}$ or ground       | -10  | 10             | μA   |
| $I_{OZ}$ | Tri-state output leakage current                | $V_O = V_{CC}$ or ground       | -10  | 10             | μA   |

**Table 5. EP610 & EP610I Device Capacitance** Note (8)

| Symbol     | Parameter             | Conditions                                    | EP610-15<br>EP610-20 |     | EP610-25<br>EP610-30<br>EP610-35 |     | EP610I |     | Unit |
|------------|-----------------------|-----------------------------------------------|----------------------|-----|----------------------------------|-----|--------|-----|------|
|            |                       |                                               | Min                  | Max | Min                              | Max | Min    | Max |      |
| $C_{IN}$   | Input pin capacitance | $V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$  |                      | 10  |                                  | 20  |        | 8   | pF   |
| $C_{I/O}$  | I/O pin capacitance   | $V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$ |                      | 12  |                                  | 20  |        | 8   | pF   |
| $C_{CLK1}$ | CLK1 pin capacitance  | $V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$  |                      | 20  |                                  | 20  |        | 10  | pF   |
| $C_{CLK2}$ | CLK2 pin capacitance  | $V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$  |                      | 20  |                                  | 50  |        | 12  | pF   |

**Table 6. EP610 Device  $I_{CC}$  Supply Current** Note (1), (9)

| Symbol    | Parameter                                       | Conditions                                                            | Speed<br>Grade   | EP610 |     |          | Unit          |
|-----------|-------------------------------------------------|-----------------------------------------------------------------------|------------------|-------|-----|----------|---------------|
|           |                                                 |                                                                       |                  | Min   | Typ | Max      |               |
| $I_{CC1}$ | $V_{CC}$ supply current<br>(non-Turbo, standby) | $V_I = V_{CC}$ or ground, no load<br>(10), (11)                       |                  |       | 20  | 150      | $\mu\text{A}$ |
| $I_{CC2}$ | $V_{CC}$ supply current<br>(non-Turbo, active)  | $V_I = V_{CC}$ or ground, no load,<br>$f = 1.0\text{ MHz}$ (10), (11) |                  |       | 5   | 10 (15)  | mA            |
| $I_{CC3}$ | $V_{CC}$ supply current<br>(Turbo, active)      | $V_I = V_{CC}$ or ground, no load,<br>$f = 1.0\text{ MHz}$ (11)       | -15, -20         |       | 60  | 90 (115) | mA            |
|           |                                                 |                                                                       | -25, -30,<br>-35 |       | 45  | 60 (75)  | mA            |

**Table 7. EP610I Device  $I_{CC}$  Supply Current** Note (9)

| Symbol    | Parameter                                       | Conditions                                                            | EP610I |     |     | Unit          |
|-----------|-------------------------------------------------|-----------------------------------------------------------------------|--------|-----|-----|---------------|
|           |                                                 |                                                                       | Min    | Typ | Max |               |
| $I_{CC1}$ | $V_{CC}$ supply current<br>(non-Turbo, standby) | $V_I = V_{CC}$ or ground, no load,<br>(10), (11)                      |        | 20  | 150 | $\mu\text{A}$ |
| $I_{CC2}$ | $V_{CC}$ supply current<br>(non-Turbo, active)  | $V_I = V_{CC}$ or ground, no load,<br>$f = 1.0\text{ MHz}$ (10), (11) |        | 3   | 8   | mA            |
| $I_{CC3}$ | $V_{CC}$ supply current<br>(Turbo, active)      | $V_I = V_{CC}$ or ground, no load,<br>$f = 1.0\text{ MHz}$ (11)       |        | 65  | 105 | mA            |

### Notes to tables:

- (1) Numbers in parentheses are for industrial-temperature-range devices.
- (2) The minimum DC input is  $-0.3$  V. During transitions, the inputs may undershoot to  $-2.0$  V (EP610) or  $-0.5$  V (EP610I) or overshoot to  $7.0$  V (EP610) or  $V_{CC} + 0.5$  V (EP610I) for input currents less than  $100$  mA and periods less than  $20$  ns.
- (3) For EP610 devices, maximum  $V_{CC}$  rise time is  $50$  ms. For EP610I devices, maximum  $V_{CC}$  rise time is unlimited with monotonic rise.
- (4) For EP610-15 and EP610-20 devices:  $t_R$  and  $t_F = 40$  ns.  
For EP610-15 and EP610-20 clocks:  $t_R$  and  $t_F = 20$  ns.
- (5) These values are specified in [Table 3](#)
- (6) The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current; the  $I_{OL}$  parameter refers to low-level TTL output current.
- (7) This parameter does not apply to EP610I devices.
- (8) The device capacitance is measured at  $25^\circ$  C and is sample-tested only.
- (9) Typical values are for  $T_A = 25^\circ$  C and  $V_{CC} = 5$  V.
- (10) When the Turbo Bit option is not set (non-Turbo mode), EP610 devices enter standby mode if no logic transitions occur for  $100$  ns after the last transition. When the Turbo Bit option is not set, EP610I devices enter standby mode if no logic transitions occur for  $75$  ns after the last transition.
- (11) Measured with a device programmed as a 16-bit counter.

**Table 8. EP610-15 & EP610-20 External Timing Parameters** Notes (1)

| Symbol     | Parameter                               | Conditions     | EP610-15 |      | EP610-20 |      | Non-Turbo Adder | Unit |
|------------|-----------------------------------------|----------------|----------|------|----------|------|-----------------|------|
|            |                                         |                | Min      | Max  | Min      | Max  | (2)             |      |
| $t_{PD1}$  | Input to non-registered output          | C1 = 35 pF     |          | 15.0 |          | 20.0 | 20.0            | ns   |
| $t_{PD2}$  | I/O input to non-registered output      | C1 = 35 pF     |          | 17.0 |          | 22.0 | 20.0            | ns   |
| $t_{PZX}$  | Input to output enable                  | C1 = 35 pF     |          | 15.0 |          | 20.0 | 20.0            | ns   |
| $t_{PXZ}$  | Input to output disable                 | C1 = 5 pF (3)  |          | 15.0 |          | 20.0 | 20.0            | ns   |
| $t_{CLR}$  | Asynchronous output clear time          | C1 = 35 pF     |          | 15.0 |          | 20.0 | 20.0            | ns   |
| $f_{MAX}$  | Maximum clock frequency                 | (4)            | 83.3     |      | 62.5     |      | 0.0             | MHz  |
| $t_{SU}$   | Global clock input setup time           |                | 9.0      |      | 11.0     |      | 20.0            | ns   |
| $t_H$      | Global clock input hold time            |                | 0.0      |      | 0.0      |      | 0.0             | ns   |
| $t_{CH}$   | Global clock high time                  |                | 6.0      |      | 8.0      |      | 0.0             | ns   |
| $t_{CL}$   | Global clock low time                   |                | 6.0      |      | 8.0      |      | 0.0             | ns   |
| $t_{CO1}$  | Global clock to output delay            |                |          | 11.0 |          | 13.0 | 0.0             | ns   |
| $t_{CNT}$  | Global clock minimum period             |                |          | 12.0 |          | 16.0 | 0.0             | ns   |
| $f_{CNT}$  | Maximum internal global clock frequency | (5)            | 83.3     |      | 62.5     |      | 0.0             | MHz  |
| $t_{ASU}$  | Array clock input setup time            |                | 6.0      |      | 8.0      |      | 20.0            | ns   |
| $t_{AH}$   | Array clock input hold time             |                | 6.0      |      | 8.0      |      | 0.0             | ns   |
| $t_{ACH}$  | Array clock high time                   |                | 7.0      |      | 9.0      |      | 0.0             | ns   |
| $t_{ACL}$  | Array clock low time                    |                | 7.0      |      | 9.0      |      | 0.0             | ns   |
| $t_{ODH}$  | Output data hold time after clock       | C1 = 35 pF (6) | 1.0      |      | 1.0      |      | 1.0             | ns   |
| $t_{ACO1}$ | Array clock to output delay             |                |          | 15.0 |          | 20.0 | 20.0            | ns   |
| $t_{ACNT}$ | Array clock minimum period              |                |          | 14.0 |          | 18.0 | 0.0             | ns   |
| $f_{ACNT}$ | Array clock internal maximum frequency  | (5)            | 71.4     |      | 55.6     |      | 0.0             | MHz  |

**Table 9. EP610-15 & EP610-20 Internal Timing Parameters (Part 1 of 2)**

| Symbol    | Parameter                      | Conditions | EP610-15 |     | EP610-20 |      | Unit |
|-----------|--------------------------------|------------|----------|-----|----------|------|------|
|           |                                |            | Min      | Max | Min      | Max  |      |
| $t_{IN}$  | Input pad and buffer delay     |            |          | 4.0 |          | 4.0  | ns   |
| $t_{IO}$  | I/O input pad and buffer delay |            |          | 2.0 |          | 2.0  | ns   |
| $t_{LAD}$ | Logic array delay              |            |          | 6.0 |          | 11.0 | ns   |
| $t_{OD}$  | Output buffer and pad delay    | C1 = 35 pF |          | 5.0 |          | 5.0  | ns   |
| $t_{ZX}$  | Output buffer enable delay     | C1 = 35 pF |          | 5.0 |          | 5.0  | ns   |
| $t_{XZ}$  | Output buffer disable delay    | C1 = 5 pF  |          | 5.0 |          | 5.0  | ns   |

**Table 9. EP610-15 & EP610-20 Internal Timing Parameters (Part 2 of 2)**

| Symbol    | Parameter           | Conditions | EP610-15 |     | EP610-20 |      | Unit |
|-----------|---------------------|------------|----------|-----|----------|------|------|
|           |                     |            | Min      | Max | Min      | Max  |      |
| $t_{SU}$  | Register setup time |            | 5.0      |     | 4.0      |      | ns   |
| $t_H$     | Register hold time  |            | 4.0      |     | 7.0      |      | ns   |
| $t_{IC}$  | Array clock delay   |            |          | 6.0 |          | 11.0 | ns   |
| $t_{ICS}$ | Global clock delay  |            |          | 2.0 |          | 4.0  | ns   |
| $t_{FD}$  | Feedback delay      |            |          | 1.0 |          | 1.0  | ns   |
| $t_{CLR}$ | Register clear time |            |          | 6.0 |          | 11.0 | ns   |

Tables 10 and 11 show the timing parameters for EP610-25, EP610-30 and EP610-35 devices.

**Table 10. EP610-25, EP610-30 & EP610-35 External Timing Parameters** Notes (1)

| Symbol     | Parameter                               | Conditions     | EP610-25 |      | EP610-30 |      | EP610-35 |      | Non-Turbo Adder | Unit |
|------------|-----------------------------------------|----------------|----------|------|----------|------|----------|------|-----------------|------|
|            |                                         |                | Min      | Max  | Min      | Max  | Min      | Max  | (2)             |      |
| $t_{PD1}$  | Input to non-registered output          | C1 = 35 pF     |          | 25.0 |          | 30.0 |          | 35.0 | 30.0            | ns   |
| $t_{PD2}$  | I/O input to non-registered output      |                |          | 27.0 |          | 32.0 |          | 37.0 | 30.0            | ns   |
| $t_{PZX}$  | Input to output enable                  |                |          | 25.0 |          | 30.0 |          | 35.0 | 30.0            | ns   |
| $t_{PXZ}$  | Input to output disable                 | C1 = 5 pF (3)  |          | 25.0 |          | 30.0 |          | 35.0 | 30.0            | ns   |
| $t_{CLR}$  | Asynchronous output clear time          | C1 = 35 pF     |          | 27.0 |          | 32.0 |          | 37.0 | 30.0            | ns   |
| $f_{MAX}$  | Maximum frequency                       | (4)            | 47.6     |      | 41.7     |      | 37.0     |      | 0.0             | MHz  |
| $t_{SU}$   | Global clock input setup time           |                | 21.0     |      | 24.0     |      | 27.0     |      | 30.0            | ns   |
| $t_H$      | Global clock input hold time            |                | 0.0      |      | 0.0      |      | 0.0      |      | 0.0             | ns   |
| $t_{CH}$   | Global clock high time                  |                | 10.0     |      | 11.0     |      | 12.0     |      | 0.0             | ns   |
| $t_{CL}$   | Global clock low time                   |                | 10.0     |      | 11.0     |      | 12.0     |      | 0.0             | ns   |
| $t_{CO1}$  | Global clock to output delay            |                |          | 15.0 |          | 17.0 |          | 20.0 | 0.0             | ns   |
| $t_{CNT}$  | Global clock minimum period             |                |          | 25.0 |          | 30.0 |          | 35.0 | 0.0             | ns   |
| $f_{CNT}$  | Maximum internal global clock frequency | (5)            | 40.0     |      | 33.3     |      | 28.6     |      | 0.0             | MHz  |
| $t_{ASU}$  | Array clock input setup time            |                | 8.0      |      | 8.0      |      | 8.0      |      | 30.0            | ns   |
| $t_{AH}$   | Array clock input hold time             |                | 12.0     |      | 12.0     |      | 12.0     |      | 0.0             | ns   |
| $t_{ACH}$  | Array clock high time                   |                | 10.0     |      | 11.0     |      | 12.0     |      | 0.0             | ns   |
| $t_{ACL}$  | Array clock low time                    |                | 10.0     |      | 11.0     |      | 12.0     |      | 0.0             | ns   |
| $t_{ODH}$  | Output data hold time after clock       | C1 = 35 pF (6) | 1.0      |      | 1.0      |      | 1.0      |      |                 | ns   |
| $t_{ACO1}$ | Array clock to output delay             |                |          | 27.0 |          | 32.0 |          | 37.0 | 30.0            | ns   |
| $t_{ACNT}$ | Array clock minimum period              |                |          | 25.0 |          | 30.0 |          | 35.0 | 0.0             | ns   |
| $f_{ACNT}$ | Maximum internal global clock frequency | (5)            | 40.0     |      | 33.3     |      | 28.6     |      | 0.0             | MHz  |

**Table 11. EP610-25, EP610-30 & EP610-35 Internal Timing Parameters**

| Symbol    | Parameter                      | Condition  | EP610-25 |      | EP610-30 |      | EP610-35 |      | Unit |
|-----------|--------------------------------|------------|----------|------|----------|------|----------|------|------|
|           |                                |            | Min      | Max  | Min      | Max  | Min      | Max  |      |
| $t_{IN}$  | Input pad and buffer delay     |            |          | 8.0  |          | 9.0  |          | 11.0 | ns   |
| $t_{IO}$  | I/O input pad and buffer delay |            |          | 2.0  |          | 2.0  |          | 2.0  | ns   |
| $t_{LAD}$ | Logic array delay              |            |          | 11.0 |          | 14.0 |          | 15.0 | ns   |
| $t_{OD}$  | Output buffer and pad delay    | C1 = 35 pF |          | 6.0  |          | 7.0  |          | 9.0  | ns   |
| $t_{ZX}$  | Output buffer enable delay     | C1 = 35 pF |          | 6.0  |          | 7.0  |          | 9.0  | ns   |
| $t_{XZ}$  | Output buffer disable delay    | C1 = 5 pF  |          | 6.0  |          | 7.0  |          | 9.0  | ns   |
| $t_{SU}$  | Register setup time            |            | 11.0     |      | 11.0     |      | 12.0     |      | ns   |
| $t_H$     | Register hold time             |            | 10.0     |      | 10.0     |      | 10.0     |      | ns   |
| $t_{IC}$  | Array clock delay              |            |          | 13.0 |          | 16.0 |          | 17.0 | ns   |
| $t_{ICS}$ | Global clock delay             |            |          | 1.0  |          | 1.0  |          | 0.0  | ns   |
| $t_{FD}$  | Feedback delay                 |            |          | 3.0  |          | 5.0  |          | 8.0  | ns   |
| $t_{CLR}$ | Register clear time            |            |          | 13.0 |          | 16.0 |          | 17.0 | ns   |

**Notes to tables:**

- (1) These values are specified in [Table 3](#)
- (2) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.
- (3) Sample-tested only for an output change of 500 mV.
- (4) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (5) Measured with a device programmed as a 16-bit counter.
- (6) Sample-tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.

**Table 12. EP610I External Timing Parameters** Notes (1)

| Symbol            | Parameter                               | Conditions     | EP610I-10 |      | EP610I-12 |      | EP610I-15 |      | Non-Turbo Adder | Unit |
|-------------------|-----------------------------------------|----------------|-----------|------|-----------|------|-----------|------|-----------------|------|
|                   |                                         |                | Min       | Max  | Min       | Max  | Min       | Max  | (2)             |      |
| t <sub>PD1</sub>  | Input to non-registered output          | C1 = 35 pF     |           | 10.0 |           | 12.0 |           | 15.0 | 25.0            | ns   |
| t <sub>PD2</sub>  | I/O input to non-registered output      |                |           | 10.0 |           | 12.0 |           | 15.0 | 25.0            | ns   |
| t <sub>PZX</sub>  | Input to output enable                  |                |           | 15.0 |           | 15.0 |           | 18.0 | 25.0            | ns   |
| t <sub>PXZ</sub>  | Input to output disable                 | C1 = 5 pF (3)  |           | 13.0 |           | 15.0 |           | 18.0 | 25.0            | ns   |
| t <sub>CLR</sub>  | Asynchronous output clear time          | C1 = 35 pF     |           | 13.0 |           | 15.0 |           | 18.0 | 25.0            | ns   |
| f <sub>MAX</sub>  | Maximum frequency                       | (4)            | 125.0     |      | 100.0     |      | 83.3      |      | 0.0             | MHz  |
| t <sub>SU</sub>   | Global clock input setup time           |                | 7.0       |      | 9.0       |      | 12.0      |      | 25              | ns   |
| t <sub>H</sub>    | Global clock input hold time            |                | 0.0       |      | 0.0       |      | 0.0       |      | 0.0             | ns   |
| t <sub>CH</sub>   | Global clock high time                  |                | 5.0       |      | 5.0       |      | 5.0       |      | 0.0             | ns   |
| t <sub>CL</sub>   | Global clock low time                   |                | 5.0       |      | 5.0       |      | 5.0       |      | 0.0             | ns   |
| t <sub>CO1</sub>  | Global clock to output delay            |                |           | 6.5  |           | 8.0  |           | 8.0  | 0.0             | ns   |
| t <sub>CNT</sub>  | Global clock minimum period             |                |           | 10.0 |           | 12.0 |           | 15.0 | 25.0            | ns   |
| f <sub>CNT</sub>  | Maximum internal global clock frequency | (5)            | 100.0     |      | 83.3      |      | 66.0      |      | 0.0             | MHz  |
| t <sub>ASU</sub>  | Array clock input setup time            |                | 1.5       |      | 3.0       |      | 4.0       |      | 25.0            | ns   |
| t <sub>AH</sub>   | Array clock input hold time             |                | 5.5       |      | 6.0       |      | 6.0       |      | 0.0             | ns   |
| t <sub>ACH</sub>  | Array clock high time                   |                | 5.0       |      | 5.0       |      | 6.0       |      | 0.0             | ns   |
| t <sub>ACL</sub>  | Array clock low time                    |                | 5.0       |      | 5.0       |      | 6.0       |      | 0.0             | ns   |
| t <sub>ODH</sub>  | Output data hold time after clock       | C1 = 35 pF (6) | 1.0       |      | 1.0       |      | 1.0       |      |                 | ns   |
| t <sub>ACO1</sub> | Array clock to output delay             |                |           | 12.0 |           | 14.0 |           | 16.0 | 25.0            | ns   |
| t <sub>ACNT</sub> | Array clock minimum period              |                |           | 10.0 |           | 12.0 |           | 15.0 | 25.0            | ns   |
| f <sub>ACNT</sub> | Maximum internal array clock frequency  | (5)            | 100.0     |      | 83.3      |      | 66.0      |      | 0.0             | MHz  |

**Table 13. EP610 Internal Timing Parameters**

| Symbol    | Parameter                      | Conditions | EP610I-10 |     | EP610I-12 |     | EP610I-15 |      | Unit |
|-----------|--------------------------------|------------|-----------|-----|-----------|-----|-----------|------|------|
|           |                                |            | Min       | Max | Min       | Max | Min       | Max  |      |
| $t_{IN}$  | Input pad and buffer delay     |            |           | 1.5 |           | 4.0 |           | 4.0  | ns   |
| $t_{IO}$  | I/O input pad and buffer delay |            |           | 0.0 |           | 0.0 |           | 0.0  | ns   |
| $t_{LAD}$ | Logic array delay              |            |           | 5.5 |           | 6.0 |           | 9.0  | ns   |
| $t_{OD}$  | Output buffer and pad delay    | C1 = 35 pF |           | 3.0 |           | 2.0 |           | 2.0  | ns   |
| $t_{ZX}$  | Output buffer enable delay     | C1 = 35 pF |           | 8.0 |           | 5.0 |           | 6.0  | ns   |
| $t_{XZ}$  | Output buffer disable delay    | C1 = 5 pF  |           | 6.0 |           | 5.0 |           | 6.0  | ns   |
| $t_{SU}$  | Register setup time            |            | 3.5       |     | 5.0       |     | 5.0       |      | ns   |
| $t_H$     | Register hold time             |            | 3.5       |     | 4.0       |     | 7.0       |      | ns   |
| $t_{IC}$  | Array clock delay              |            |           | 7.5 |           | 8.0 |           | 10.0 | ns   |
| $t_{ICS}$ | Global clock delay             |            |           | 2.0 |           | 2.0 |           | 2.0  | ns   |
| $t_{FD}$  | Feedback delay                 |            |           | 1.0 |           | 1.0 |           | 1.0  | ns   |
| $t_{CLR}$ | Register clear time            |            |           | 8.5 |           | 9.0 |           | 12.0 | ns   |

**Notes to tables:**

- (1) These values are specified in [Table 3](#)
- (2) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.
- (3) Sample-tested only for an output change of 500 mV.
- (4) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (5) Measured with a device programmed as a 16-bit counter.
- (6) Sample-tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.



### *Notes:*

Rochester EPLD devices normally sold in the un-configured state are tested using the original manufacturer's test software to guarantee the data sheet specifications. In some cases, EPLD devices can be configured to the customer's design and fully tested as such.

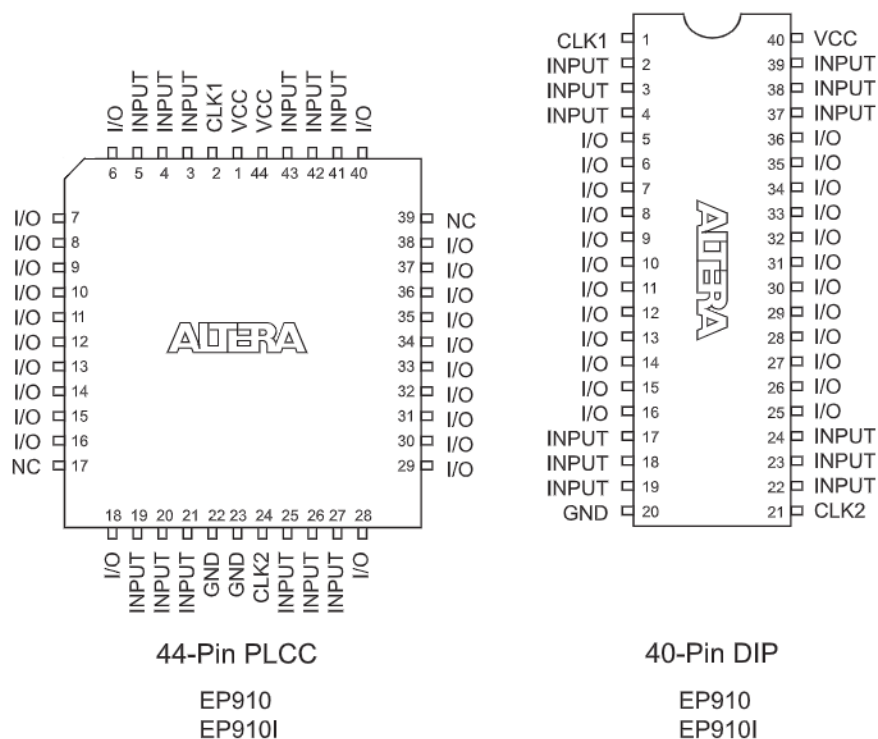
## EP910 EPLD

### Features

- High-performance, 24-macrocell Classic EPLD
  - Combinatorial speeds with  $t_{PD}$  as fast as 12 ns
  - Counter frequencies of up to 76.9 MHz
  - Pipelined data rates of up to 125 MHz
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- EP910 and EP910I devices are pin-, function-, and programming file-compatible
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in the following packages (see [Figure 11](#))
  - 44-pin plastic J-lead chip carrier (PLCC)
  - 40-pin ceramic and plastic dual in-line packages (CerDIP and PDIP)

**Figure 11. EP910 Package Pin-Out Diagrams**

*Package outlines are not drawn to scale. Windows in ceramic packages only.*

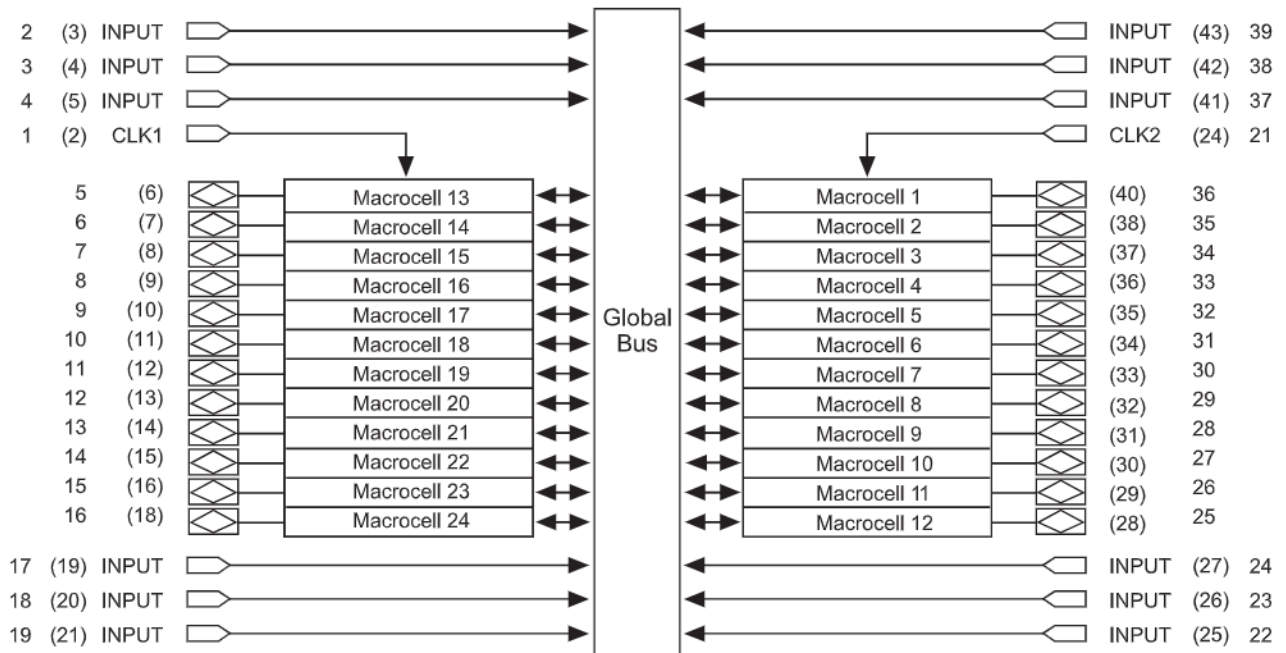


## General Description

EP910 devices can implement up to 450 usable gates of SSI and MSI logic functions. EP910 devices have 24 macrocells, 12 dedicated input pins, 24 I/O pins, and 2 global clock pins. Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true complement forms of either the output of the macrocell or the I/O input. The CLK1 and CLK2 signals are the dedicated clock inputs for the registers in macrocells 13 through 24 and 1 through 12, respectively.

**Figure 12. EP910 Block Diagram**

*Numbers without parentheses are for DIP packages. Numbers in parentheses are for J-lead packages.*



**Figure 13.  $I_{CC}$  vs. Frequency of EP910 Devices**

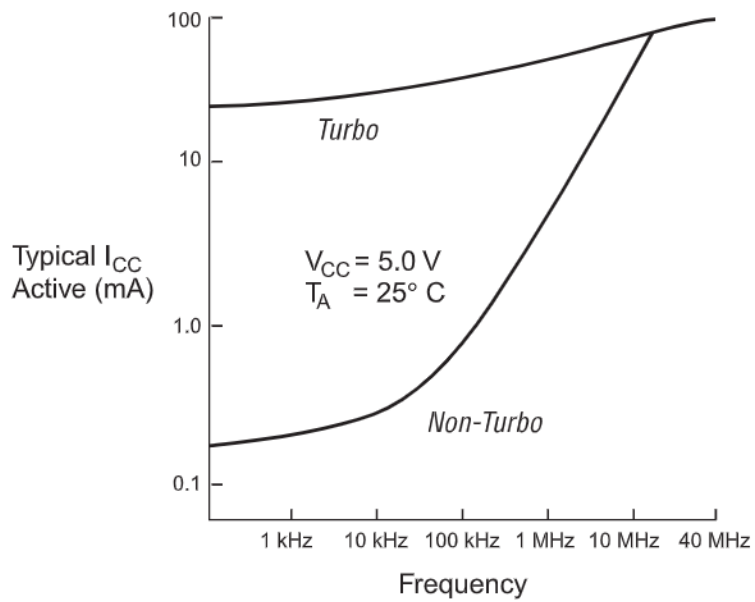
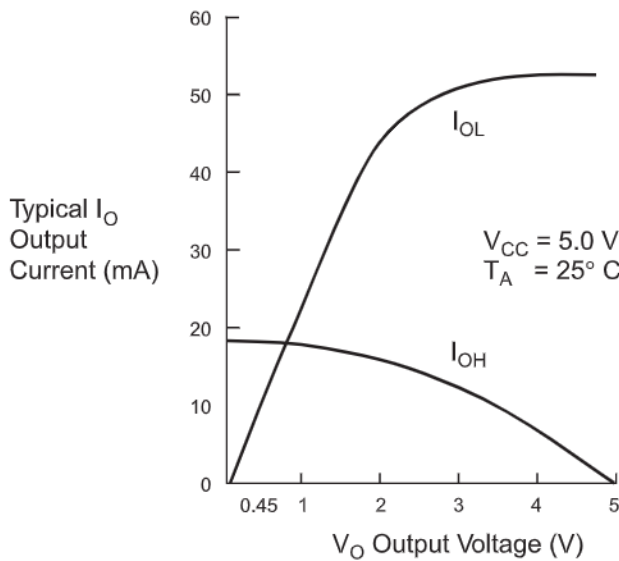


Figure 14 shows the typical output drive characteristics of EP910 devices.

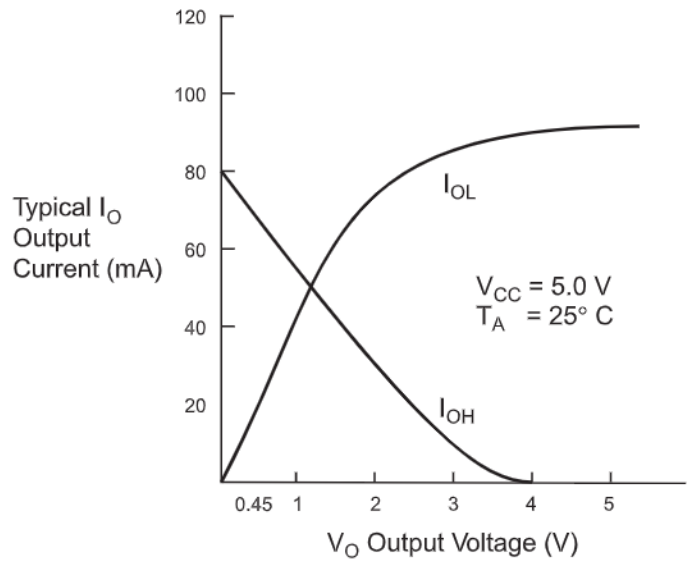
**Figure 14. Output Drive Characteristics of EP910 Devices**

Drive characteristics may exceed shown curves.

EP910 EPLDs



EP910I EPLDs



## Operating Conditions

Tables 14 through 18 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for EP910 and EP910I devices.

**Table 14. EP910 & EP910I Device Absolute Maximum Ratings** Notes (1)

| Symbol           | Parameter                            | Conditions                   | EP910 |     | EP910I |                       | Unit |
|------------------|--------------------------------------|------------------------------|-------|-----|--------|-----------------------|------|
|                  |                                      |                              | Min   | Max | Min    | Max                   |      |
| V <sub>CC</sub>  | Supply voltage                       | With respect to ground (2)   | –2.0  | 7.0 | –2.0   | 7.0                   | V    |
| V <sub>I</sub>   | DC input voltage                     |                              | –2.0  | 7.0 | –0.5   | V <sub>CC</sub> + 0.5 | V    |
| I <sub>MAX</sub> | DC V <sub>CC</sub> or ground current |                              | –250  | 250 |        |                       | mA   |
| I <sub>OUT</sub> | DC output current, per pin           |                              | –25   | 25  |        |                       | mA   |
| T <sub>STG</sub> | Storage temperature                  | No bias                      | –65   | 150 | –65    | 150                   | ° C  |
| T <sub>AMB</sub> | Ambient temperature                  | Under bias                   | –65   | 135 | –65    | 135                   | ° C  |
| T <sub>J</sub>   | Junction temperature                 | Ceramic packages, under bias |       | 150 |        | 150                   | ° C  |
|                  |                                      | Plastic packages, under bias |       | 135 |        | 135                   | ° C  |

**Table 15. EP910 & EP910I Device Recommended Operating Conditions** Notes (1)

| Symbol          | Parameter             | Conditions         | EP910      |                       | EP910I |                       | Unit |
|-----------------|-----------------------|--------------------|------------|-----------------------|--------|-----------------------|------|
|                 |                       |                    | Min        | Max                   | Min    | Max                   |      |
| V <sub>CC</sub> | Supply voltage        | (3)                | 4.75 (4.5) | 5.25 (5.5)            | 4.75   | 5.25                  | V    |
| V <sub>I</sub>  | Input voltage         |                    | –0.3       | V <sub>CC</sub> + 0.3 | –0.3   | V <sub>CC</sub> + 0.3 | V    |
| V <sub>O</sub>  | Output voltage        |                    | 0          | V <sub>CC</sub>       | 0      | V <sub>CC</sub>       | V    |
| T <sub>A</sub>  | Operating temperature | For commercial use | 0          | 70                    | 0      | 70                    | ° C  |
|                 |                       | For industrial use | –40        | 85                    |        |                       | ° C  |
| t <sub>R</sub>  | Input rise time       | (4)                |            | 100 (50)              |        | 500                   | ns   |
| t <sub>F</sub>  | Input fall time       | (4)                |            | 100 (50)              |        | 500                   | ns   |

**Table 16. EP910 & EP910I Device DC Operating Conditions** Notes (5), (6)

| Symbol          | Parameter                                   | Conditions                                 | Min  | Max                   | Unit |
|-----------------|---------------------------------------------|--------------------------------------------|------|-----------------------|------|
| V <sub>IH</sub> | High-level input voltage                    |                                            | 2.0  | V <sub>CC</sub> + 0.3 | V    |
| V <sub>IL</sub> | Low-level input voltage                     |                                            | –0.3 | 0.8                   | V    |
| V <sub>OH</sub> | High-level TTL output voltage               | I <sub>OH</sub> = –4 mA DC (7)             | 2.4  |                       | V    |
|                 | High-level CMOS output voltage              | I <sub>OH</sub> = –0.6 mA DC (7), (8)      | 3.84 |                       | V    |
| V <sub>OL</sub> | Low-level output voltage                    | I <sub>OL</sub> = 4 mA DC (7)              |      | 0.45                  | V    |
| I <sub>I</sub>  | I/O leakage current of dedicated input pins | V <sub>I</sub> = V <sub>CC</sub> or ground | –10  | 10                    | μA   |
| I <sub>OZ</sub> | Tri-state output leakage current            | V <sub>O</sub> = V <sub>CC</sub> or ground | –10  | 10                    | μA   |

**Table 17. EP910 & EP910I Device Capacitance** Notes (5)

| Symbol     | Parameter             | Conditions                                    | EP910 |     | EP910I |     | Unit |
|------------|-----------------------|-----------------------------------------------|-------|-----|--------|-----|------|
|            |                       |                                               | Min   | Max | Min    | Max |      |
| $C_{IN}$   | Input pin capacitance | $V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$  |       | 20  |        | 8   | pF   |
| $C_{I/O}$  | I/O pin capacitance   | $V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$ |       | 20  |        | 8   | pF   |
| $C_{CLK1}$ | CLK1 pin capacitance  | $V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$  |       | 20  |        | 10  | pF   |
| $C_{CLK2}$ | CLK2 pin capacitance  | $V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$  |       | 60  |        | 12  | pF   |

**Table 18. EP910 & EP910I Device  $I_{CC}$  Supply Current** Notes (1), (5), (6)

| Symbol    | Parameter                                    | Conditions                                                          | EP910 |     |          | EP910I |     |     | Unit |
|-----------|----------------------------------------------|---------------------------------------------------------------------|-------|-----|----------|--------|-----|-----|------|
|           |                                              |                                                                     | Min   | Typ | Max      | Min    | Typ | Max |      |
| $I_{CC1}$ | $V_{CC}$ supply current (non-Turbo, standby) | $V_I = V_{CC}$ or ground, no load (9), (10) †                       |       | 20  | 150      |        | 60  | 150 | μA   |
| $I_{CC2}$ | $V_{CC}$ supply current (non-Turbo, active)  | $V_I = V_{CC}$ or ground, no load, $f = 1.0\text{ MHz}$ (9), (10) † |       | 6   | 20       |        | 4   | 12  | mA   |
| $I_{CC3}$ | $V_{CC}$ supply current (Turbo, active)      | $V_I = V_{CC}$ or ground, no load, $f = 1.0\text{ MHz}$ (10)        |       | 45  | 80 (100) |        | 120 | 150 | mA   |

**Notes to tables:**

- (1) Numbers in parentheses are for industrial-temperature-range devices.
- (2) The minimum DC input is  $-0.3\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  (EP910) or  $-0.5\text{ V}$  (EP910I) or overshoot to  $7.0\text{ V}$  (EP910) or  $V_{CC} + 0.5\text{ V}$  (EP910I) for input currents less than  $100\text{ mA}$  and periods less than  $20\text{ ns}$ .  
Maximum  $V_{CC}$  rise time for EP910 devices =  $50\text{ ms}$ ; for EP910I devices, maximum  $V_{CC}$  rise time is unlimited with monotonic rise.
- (3) For all clocks:  $t_R$  and  $t_F = 100\text{ ns}$  ( $50\text{ ns}$  for the industrial-temperature-range version).
- (4) These values are specified in Table 15
- (5) The device capacitance is measured at  $25^\circ\text{ C}$  and is sample-tested only.
- (6) The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current; the  $I_{OL}$  parameter refers to low-level TTL output current.
- (7) This parameter does not apply to EP910I devices.
- (8) When the Turbo Bit option is not set (non-Turbo mode), an EP910 device will enter standby mode if no logic transitions occur for  $100\text{ ns}$  after the last transition, and an EP910I device will enter standby mode if no logic transitions occur for  $75\text{ ns}$  after the last transition.
- (9) Measured with a device programmed as a 24-bit counter.

**Table 19. EP910 External Timing Parameters** Notes (1)

| Symbol            | Parameter                               | Conditions     | EP910-30 |      | EP910-35 |      | EP910-40 |      | Non-Turbo Adder (2) | Unit |
|-------------------|-----------------------------------------|----------------|----------|------|----------|------|----------|------|---------------------|------|
|                   |                                         |                | Min      | Max  | Min      | Max  | Min      | Max  |                     |      |
| t <sub>PD1</sub>  | Input to non-registered output          | C1 = 35 pF     |          | 30.0 |          | 35.0 |          | 40.0 | 30.0                | ns   |
| t <sub>PD2</sub>  | I/O input to non-registered output      | C1 = 35 pF     |          | 33.0 |          | 38.0 |          | 43.0 | 30.0                | ns   |
| t <sub>PZX</sub>  | Input to output enable                  | C1 = 35 pF     |          | 30.0 |          | 35.0 |          | 40.0 | 30.0                | ns   |
| t <sub>PXZ</sub>  | Input to output disable                 | C1 = 5 pF (3)  |          | 30.0 |          | 35.0 |          | 40.0 | 30.0                | ns   |
| t <sub>CLR</sub>  | Asynchronous output clear time          | C1 = 35 pF     |          | 33.0 |          | 38.0 |          | 43.0 | 30.0                | ns   |
| f <sub>MAX</sub>  | Maximum frequency                       | (4)            | 41.7     |      | 37.0     |      | 32.3     |      | 0.0                 | MHz  |
| t <sub>SU</sub>   | Global clock input setup time           |                | 24.0     |      | 27.0     |      | 31.0     |      | 30.0                | ns   |
| t <sub>H</sub>    | Global clock input hold time            |                | 0.0      |      | 0.0      |      | 0.0      |      | 0.0                 | ns   |
| t <sub>CH</sub>   | Global clock high time                  |                | 12.0     |      | 13.0     |      | 15.0     |      | 0.0                 | ns   |
| t <sub>CL</sub>   | Global clock low time                   |                | 12.0     |      | 13.0     |      | 15.0     |      | 0.0                 | ns   |
| t <sub>CO1</sub>  | Global clock to output delay            | C1 = 35 pF     |          | 18   |          | 21.0 |          | 24.0 | 0.0                 | ns   |
| t <sub>CNT</sub>  | Global clock minimum clock period       | (5)            |          | 30.0 |          | 35.0 |          | 40.0 | 0.0                 | ns   |
| f <sub>CNT</sub>  | Maximum internal global clock frequency | (5)            | 33.3     |      | 28.6     |      | 25.0     |      | 0.0                 | MHz  |
| t <sub>ASU</sub>  | Array clock input setup time            |                | 10.0     |      | 10.0     |      | 10.0     |      | 30.0                | ns   |
| t <sub>AH</sub>   | Array clock input hold time             |                | 15.0     |      | 15.0     |      | 15.0     |      | 0.0                 | ns   |
| t <sub>ACH</sub>  | Array clock high time                   |                | 15.0     |      | 16.0     |      | 17.0     |      | 0.0                 | ns   |
| t <sub>ACL</sub>  | Array clock low time                    |                | 15.0     |      | 16.0     |      | 17.0     |      | 0.0                 | ns   |
| t <sub>ODH</sub>  | Output data hold time after clock       | C1 = 35 pF (6) | 1.0      |      | 1.0      |      | 1.0      |      |                     | ns   |
| t <sub>ACO1</sub> | Array clock to output delay             | C1 = 35 pF     |          | 33.0 |          | 38.0 |          | 43.0 | 30.0                | ns   |
| t <sub>ACNT</sub> | Array clock minimum clock period        |                |          | 30.0 |          | 35.0 |          | 40.0 | 0.0                 | ns   |
| f <sub>ACNT</sub> | Maximum internal array clock frequency  | (5)            | 33.3     |      | 28.6     |      | 25.0     |      | 0.0                 | MHz  |

**Table 20. EP910 Internal Timing Parameters**

| Symbol    | Parameter                      | Condition  | EP910-30 |      | EP910-35 |      | EP910-40 |      | Unit |
|-----------|--------------------------------|------------|----------|------|----------|------|----------|------|------|
|           |                                |            | Min      | Max  | Min      | Max  | Min      | Max  |      |
| $t_{IN}$  | Input pad and buffer delay     |            |          | 9.0  |          | 10.0 |          | 13.0 | ns   |
| $t_{IO}$  | I/O input pad and buffer delay |            |          | 3.0  |          | 3.0  |          | 3.0  | ns   |
| $t_{LAD}$ | Logic array delay              |            |          | 14.0 |          | 16.0 |          | 17.0 | ns   |
| $t_{OD}$  | Output buffer and pad delay    | C1 = 35 pF |          | 7.0  |          | 9.0  |          | 10.0 | ns   |
| $t_{ZX}$  | Output buffer enable delay     | C1 = 35 pF |          | 7.0  |          | 9.0  |          | 10.0 | ns   |
| $t_{XZ}$  | Output buffer disable delay    | C1 = 5 pF  |          | 7.0  |          | 9.0  |          | 10.0 | ns   |
| $t_{SU}$  | Register setup time            |            | 12.0     |      | 13.0     |      | 15.0     |      | ns   |
| $t_H$     | Register hold time             |            | 12.0     |      | 12.0     |      | 12.0     |      | ns   |
| $t_{IC}$  | Array clock delay              |            |          | 17.0 |          | 19.0 |          | 20.0 | ns   |
| $t_{ICS}$ | Global clock delay             |            |          | 2.0  |          | 2.0  |          | 1.0  | ns   |
| $t_{FD}$  | Feedback delay                 |            |          | 4.0  |          | 6.0  |          | 8.0  | ns   |
| $t_{CLR}$ | Register clear time            |            |          | 17.0 |          | 19.0 |          | 20.0 | ns   |

**Notes to tables:**

- (1) These values are specified in [Table 15](#)
- (2) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.
- (3) Sample-tested only for an output change of 500 mV.
- (4) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (5) Measured with a device programmed as a 24-bit counter.
- (6) Sample-tested only. This parameter is a guideline based on extensive device characterization and applies for both global and array clocking.

**Table 21. EP910I External Timing Parameters** Notes (1)

| Symbol     | Parameter                               | Conditions     | EP910I-12 |      | EP910I-15 |      | EP910I-25 |      | Non-Turbo Adder | Unit |
|------------|-----------------------------------------|----------------|-----------|------|-----------|------|-----------|------|-----------------|------|
|            |                                         |                | Min       | Max  | Min       | Max  | Min       | Max  | (2)             |      |
| $t_{PD1}$  | Input to non-registered output          | C1 = 35 pF     |           | 12.0 |           | 15.0 |           | 25.0 | 40.0            | ns   |
| $t_{PD2}$  | I/O input to non-registered output      | C1 = 35 pF     |           | 12.0 |           | 15.0 |           | 25.0 | 40.0            | ns   |
| $t_{PZX}$  | Input to output enable                  | C1 = 35 pF     |           | 15.0 |           | 18.0 |           | 28.0 | 40.0            | ns   |
| $t_{PXZ}$  | Input to output disable                 | C1 = 35 pF (3) |           | 15.0 |           | 18.0 |           | 28.0 | 40.0            | ns   |
| $t_{CLR}$  | Asynchronous output clear time          | C1 = 35 pF     |           | 15.0 |           | 18.0 |           | 28.0 | 40.0            | ns   |
| $f_{MAX}$  | Global clock maximum frequency          | (4)            | 125.0     |      | 100.0     |      | 62.5      |      | 0.0             | MHz  |
| $t_{SU}$   | Global clock input setup time           |                | 8.0       |      | 11.0      |      | 16.0      |      | 40.0            | ns   |
| $t_H$      | Global clock input hold time            |                | 0.0       |      | 0.0       |      | 0.0       |      | 0.0             | ns   |
| $t_{CH}$   | Global clock high time                  |                | 5.0       |      | 6.0       |      | 10.0      |      | 0.0             | ns   |
| $t_{CL}$   | Global clock low time                   |                | 5.0       |      | 6.0       |      | 10.0      |      | 0.0             | ns   |
| $t_{CO1}$  | Global clock to output delay            |                |           | 8.0  |           | 9.0  |           | 14.0 | 0.0             | ns   |
| $t_{CNT}$  | Global clock minimum clock period       | C1 = 35 pF     |           | 13.0 |           | 15.0 |           | 25.0 | 40.0            | ns   |
| $f_{CNT}$  | Maximum internal global clock frequency | (5)            | 76.9      |      | 66.6      |      | 40.0      |      | 0.0             | MHz  |
| $t_{ASU}$  | Array clock input setup time            |                | 3.0       |      | 4.0       |      | 8.0       |      | 40.0            | ns   |
| $t_{AH}$   | Array clock input hold time             |                | 6.0       |      | 7.0       |      | 8.0       |      |                 | ns   |
| $t_{ACH}$  | Array clock high time                   |                | 6.0       |      | 7.5       |      | 12.5      |      |                 | ns   |
| $t_{ACL}$  | Array clock low time                    |                | 6.0       |      | 7.5       |      | 12.5      |      |                 | ns   |
| $t_{ODH}$  | Output data hold time after clock       | C1 = 35 pF (6) | 1.0       |      | 1.0       |      | 1.0       |      |                 | ns   |
| $t_{ACO1}$ | Array clock to output delay             | C1 = 35 pF     |           | 16.0 |           | 18.0 |           | 22.0 | 40.0            | ns   |
| $t_{ACNT}$ | Array clock minimum clock period        |                |           | 13.0 |           | 15.0 |           | 25.0 | 40.0            | ns   |
| $f_{ACNT}$ | Maximum internal array clock frequency  | (5)            | 76.9      |      | 66.6      |      | 40.0      |      |                 | MHz  |

**Table 22. EP910I Internal Timing Parameters**

| Symbol    | Parameter                      | Condition  | EP910I-12 |      | EP910I-15 |      | EP910I-25 |      | Unit |
|-----------|--------------------------------|------------|-----------|------|-----------|------|-----------|------|------|
|           |                                |            | Min       | Max  | Min       | Max  | Min       | Max  |      |
| $t_{IN}$  | Input pad and buffer delay     |            |           | 2.0  |           | 3.0  |           | 2.0  | ns   |
| $t_{IO}$  | I/O input pad and buffer delay |            |           | 0.0  |           | 0.0  |           | 0.0  | ns   |
| $t_{LAD}$ | Logic array delay              |            |           | 8.0  |           | 9.0  |           | 17.0 | ns   |
| $t_{OD}$  | Output buffer and pad delay    | C1 = 35 pF |           | 2.0  |           | 3.0  |           | 6.0  | ns   |
| $t_{ZX}$  | Output buffer enable delay     | C1 = 35 pF |           | 5.0  |           | 6.0  |           | 9.0  | ns   |
| $t_{XZ}$  | Output buffer disable delay    | C1 = 5 pF  |           | 5.0  |           | 6.0  |           | 9.0  | ns   |
| $t_{SU}$  | Register setup time            |            | 4.0       |      | 5.0       |      | 5.0       |      | ns   |
| $t_H$     | Register hold time             |            | 4.0       |      | 6.0       |      | 11.0      |      | ns   |
| $t_{IC}$  | Array clock delay              |            |           | 12.0 |           | 12.0 |           | 14.0 | ns   |
| $t_{ICS}$ | Global clock delay             |            |           | 4.0  |           | 3.0  |           | 6.0  | ns   |
| $t_{FD}$  | Feedback delay                 |            |           | 1.0  |           | 1.0  |           | 3.0  | ns   |
| $t_{CLR}$ | Register clear time            |            |           | 11.0 |           | 12.0 |           | 20.0 | ns   |

**Notes to tables:**

- (1) These values are specified in [Table 15](#)
- (2) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.
- (3) Sample-tested only for an output change of 500 mV.
- (4) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (5) Measured with a device programmed as a 24-bit counter.
- (6) Sample-tested only. This parameter is a guideline based on extensive device characterization and applies for both global and array clocking.



### *Notes:*

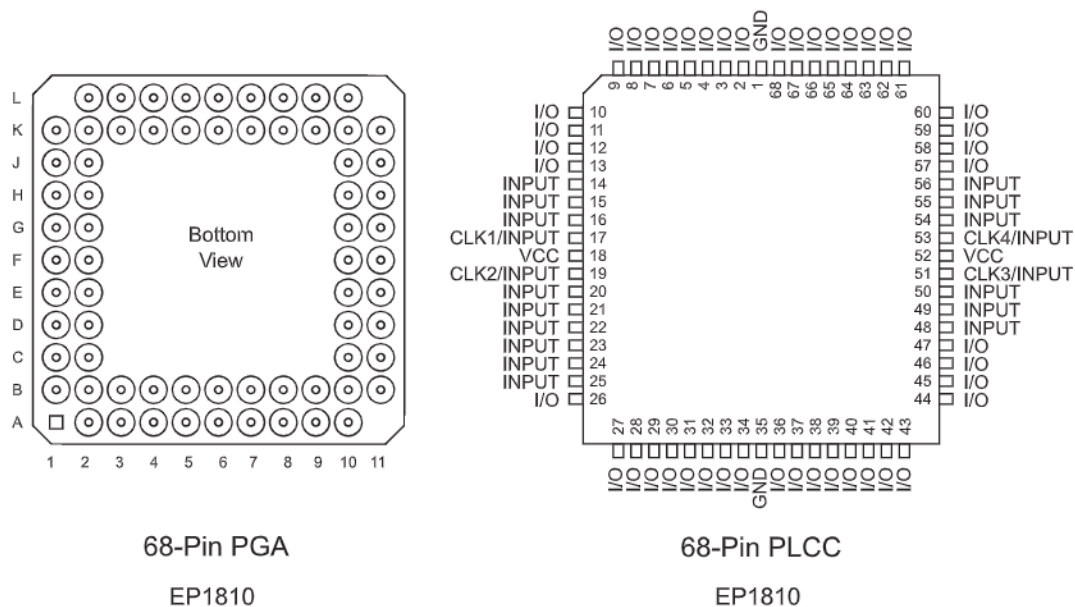
Rochester EPLD devices normally sold in the un-configured state are tested using the original manufacturer's test software to guarantee the data sheet specifications. In some cases, EPLD devices can be configured to the customer's design and fully tested as such.

# EP1810 EPLD

## Features

- High-performance, 48-macrocell Classic EPLD
  - Combinatorial speeds with  $t_{PD}$  as fast as 20 ns
  - Counter frequencies of up to 50 MHz
  - Pipelined data rates of up to 62.5 MHz
- Programmable I/O architecture with up to 64 inputs or 48 outputs
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in the following packages (see [Figure 15](#))
  - 68-pin ceramic pin-grid array (PGA)
  - 68-pin plastic J-lead chip carrier (PLCC)

**Figure 15. EP1810 Package Pin-Out Diagrams**



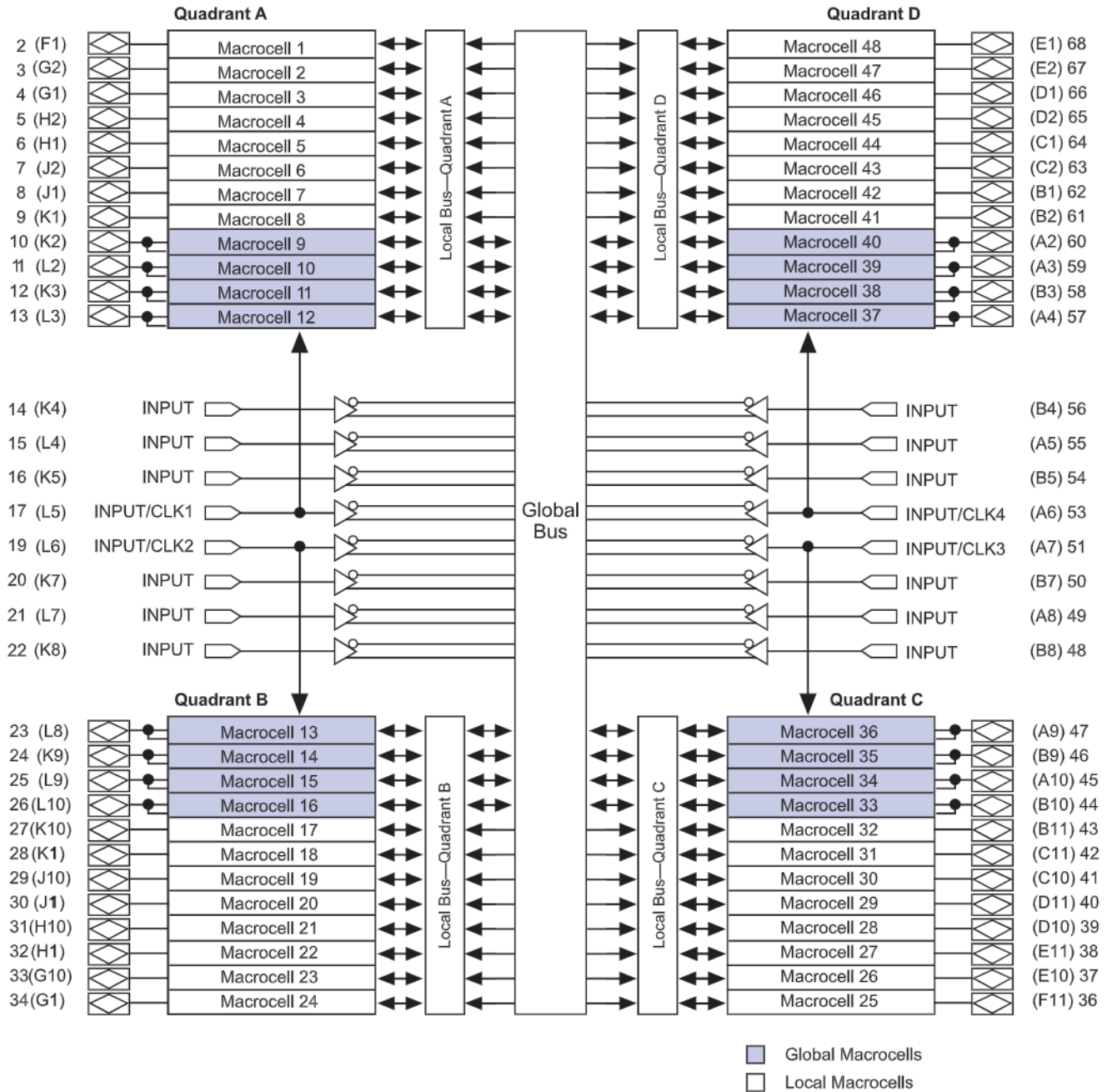
### General Description

The EP1810 device offers LSI density, TTL-equivalent speed, and low-power consumption. EP1810 devices have 48 macrocells, 16 dedicated input pins, and 48 I/O pins. EP1810 devices are divided into four quadrants, each containing 12 macrocells. Of the 12 macrocells in each quadrant, 8 have quadrant feedback and are “local” macrocells. The remaining 4 macrocells in the quadrant are “global” macrocells. Both local and global macrocells can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of the feedbacks from the global macrocells.

EP1810 devices also have four dedicated inputs (one in each quadrant) that can be used as quadrant clock inputs. If the dedicated input is used as a clock pin, the input feeds the clock input of all registers in that particular quadrant.

**Figure 16. EP1810 Block Diagram**

Pin numbers are for J-lead packages. Pin numbers in parentheses are for PGA packages.



**Figure 17.  $I_{CC}$  vs. Frequency of EP1810 Devices**

EP1810

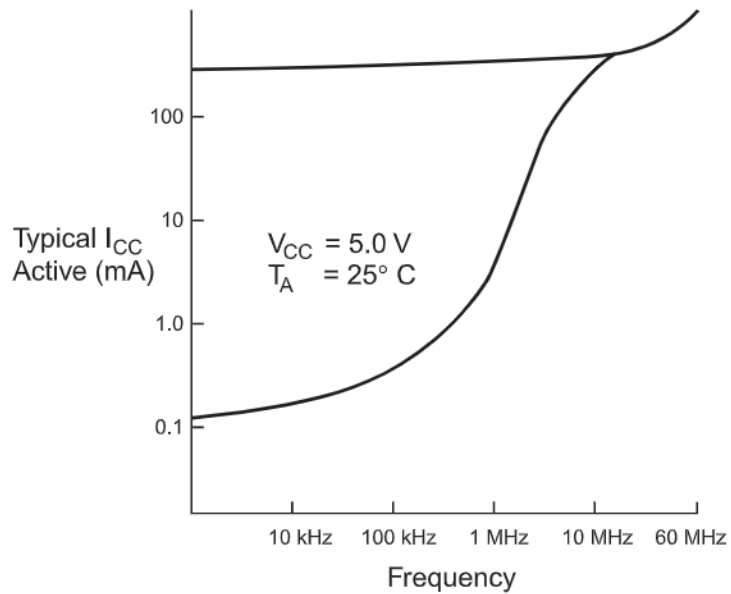
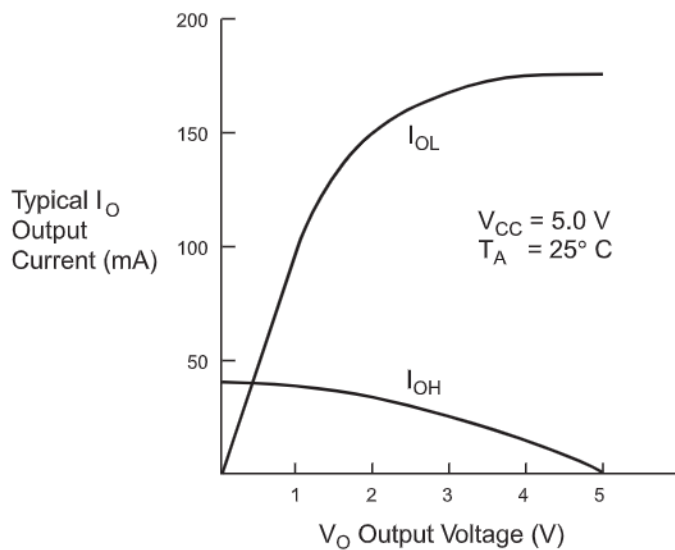


Figure 18 shows the output drive characteristics of EP1810 devices.

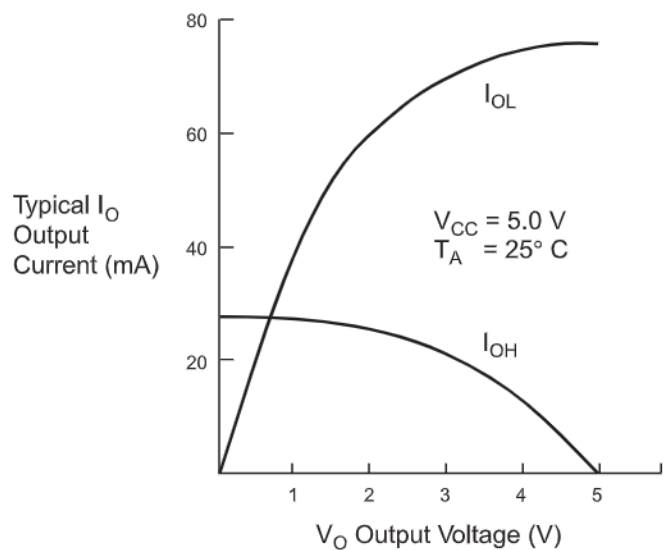
**Figure 18. Output Drive Characteristics of EP1810 Devices**

Drive characteristics may exceed shown curves.

EP1810-20 & EP1810-25 EPLDs



EP1810-35 & EP1810-45 EPLDs



## Operating Conditions

Tables 23 through 27 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for EP1810 devices.

**Table 23. EP1810 Device Absolute Maximum Ratings** Notes (1)

| Symbol    | Parameter                     | Conditions                   | Min         | Max       | Unit |
|-----------|-------------------------------|------------------------------|-------------|-----------|------|
| $V_{CC}$  | Supply voltage                | With respect to ground (2)   | -2.0 (-0.5) | 7.0       | V    |
| $V_I$     | DC input voltage              | With respect to ground (2)   | -2.0 (-0.5) | 7.0       | V    |
| $I_{MAX}$ | DC $V_{CC}$ or ground current |                              | -300 (-400) | 300 (400) | mA   |
| $I_{OUT}$ | DC output current, per pin    |                              | -25         | 25        | mA   |
| $T_{STG}$ | Storage temperature           | No bias                      | -65         | 150       | °C   |
| $T_{AMB}$ | Ambient temperature           | Under bias                   | -65         | 135       | °C   |
| $T_J$     | Junction temperature          | Ceramic packages, under bias |             | 150       | °C   |
|           |                               | Plastic packages, under bias |             | 135       | °C   |

**Table 24. EP1810 Device Recommended Operating Conditions** Notes (1)

| Symbol   | Parameter             | Conditions         | Min        | Max            | Unit |
|----------|-----------------------|--------------------|------------|----------------|------|
| $V_{CC}$ | Supply voltage        | (3)                | 4.75 (4.5) | 5.25 (5.5)     | V    |
| $V_I$    | Input voltage         |                    | -0.3       | $V_{CC} + 0.3$ | V    |
| $V_O$    | Output voltage        |                    | 0          | $V_{CC}$       | V    |
| $T_A$    | Operating temperature | For commercial use | 0          | 70             | °C   |
|          |                       | For industrial use | -40        | 85             | °C   |
| $t_R$    | Input rise time       | (4)                |            | 50             | ns   |
| $t_F$    | Input fall time       | (4)                |            | 50             | ns   |

**Table 25. EP1810 Device DC Operating Conditions** Notes (5), (6)

| Symbol   | Parameter                                       | Conditions                | Min  | Max            | Unit |
|----------|-------------------------------------------------|---------------------------|------|----------------|------|
| $V_{IH}$ | High-level input voltage                        |                           | 2.0  | $V_{CC} + 0.3$ | V    |
| $V_{IL}$ | Low-level input voltage                         |                           | -0.3 | 0.8            | V    |
| $V_{OH}$ | High-level TTL output voltage                   | $I_{OH} = -4$ mA DC (7)   | 2.4  |                | V    |
|          | High-level CMOS output voltage                  | $I_{OH} = -0.6$ mA DC (7) | 3.84 |                | V    |
| $V_{OL}$ | Low-level output voltage                        | $I_{OL} = 4$ mA DC (7)    |      | 0.45           | V    |
| $I_I$    | I/O pin leakage current of dedicated input pins | $V_I = V_{CC}$ or ground  | -10  | 10             | μA   |
| $I_{OZ}$ | Tri-state output leakage current                | $V_O = V_{CC}$ or ground  | -10  | 10             | μA   |

**Table 26. EP1810 Device Capacitance** Notes (8)

| Symbol     | Parameter                  | Conditions                                    | Min | Max | Unit |
|------------|----------------------------|-----------------------------------------------|-----|-----|------|
| $C_{IN}$   | Input pin capacitance      | $V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$  |     | 20  | pF   |
| $C_{IO}$   | I/O pin capacitance        | $V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$ |     | 20  | pF   |
| $C_{CLK1}$ | $C_{CLK1}$ pin capacitance | $V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$  |     | 25  | pF   |
| $C_{CLK2}$ | $C_{CLK2}$ pin capacitance | $V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$  |     | 160 | pF   |

**Table 27. EP1810 Device  $I_{CC}$  Supply Current** Notes (1), (5), (6)

| Symbol    | Parameter                                    | Conditions                                                  | Speed Grade | Min | Typ | Max       | Unit          |
|-----------|----------------------------------------------|-------------------------------------------------------------|-------------|-----|-----|-----------|---------------|
| $I_{CC1}$ | $V_{CC}$ supply current (non-Turbo, standby) | $V_I = V_{CC}$ or ground, no load, (9)                      | -20, -25    |     | 50  | 150       | $\mu\text{A}$ |
|           |                                              |                                                             | -35, -45    |     | 35  | 150       | $\mu\text{A}$ |
| $I_{CC2}$ | $V_{CC}$ supply current (non-Turbo, active)  | $V_I = V_{CC}$ or ground, no load, $f = 1.0\text{ MHz}$ (9) | -20, -25    |     | 20  | 40        | mA            |
|           |                                              |                                                             | -35, -45    |     | 10  | 30 (40)   | mA            |
| $I_{CC3}$ | $V_{CC}$ supply current (Turbo, active)      | $V_I = V_{CC}$ or ground, no load $f = 1.0\text{ MHz}$ (9)  | -20, -25    |     | 180 | 225 (250) | mA            |
|           |                                              |                                                             | -35, -45    |     | 100 | 180 (240) | mA            |

**Notes to tables:**

- (1) Numbers in parentheses are for industrial-temperature-range devices.
- (2) The minimum DC input is  $-0.3\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $7.0\text{ V}$  for input currents less than  $100\text{ mA}$  and periods less than  $20\text{ ns}$ .
- (3) Maximum  $V_{CC}$  rise time is  $50\text{ ms}$ .
- (4) For EP1810 clocks:  $t_R$  and  $t_F = 100\text{ ns}$  ( $50\text{ ns}$  for industrial-temperature-range versions).
- (5) Typical values are for  $T_A = 25^\circ\text{ C}$  and  $V_{CC} = 5\text{ V}$ .
- (6) These values are specified in [Table 24](#)
- (7) The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current; the  $I_{OL}$  parameter refers to low-level TTL output current.
- (8) The device capacitance is measured at  $25^\circ\text{ C}$  and is sample-tested only.
- (9) Measured with a device programmed as four 12-bit counters.

**Table 28. EP1810-20 & EP1810-25 External Timing Parameters** Notes (1)

| Symbol     | Parameter                              | Conditions     | EP1810-20 |      | EP1810-25 |      | Non-Turbo Adder | Unit |
|------------|----------------------------------------|----------------|-----------|------|-----------|------|-----------------|------|
|            |                                        |                | Min       | Max  | Min       | Max  | (2)             |      |
| $t_{PD1}$  | Input to non-registered output         | C1 = 35 pF     |           | 20.0 |           | 25.0 | 25.0            | ns   |
| $t_{PD2}$  | I/O input to non-registered output     | C1 = 35 pF     |           | 22.0 |           | 28.0 | 25.0            | ns   |
| $t_{SU}$   | Global clock setup time                |                | 13.0      |      | 17.0      |      | 25.0            | ns   |
| $t_H$      | Global clock hold time                 |                | 0.0       |      | 0.0       |      | 0.0             | ns   |
| $t_{CH}$   | Global clock high time                 |                | 8.0       |      | 10.0      |      | 0.0             | ns   |
| $t_{CL}$   | Global clock low time                  |                | 8.0       |      | 10.0      |      | 0.0             | ns   |
| $t_{CO1}$  | Global clock to output delay           | C1 = 35 pF     |           | 15.0 |           | 18.0 | 0.0             | ns   |
| $t_{CNT}$  | Minimum global clock period            | (3)            |           | 20.0 |           | 25.0 | 0.0             | ns   |
| $f_{CNT}$  | Maximum internal frequency             | (3)            | 50.0      |      | 40.0      |      | 0.0             | MHz  |
| $t_{ASU}$  | Array clock setup time                 |                | 8.0       |      | 10.0      |      | 25.0            | ns   |
| $t_{AH}$   | Array clock hold time                  |                | 8.0       |      | 10.0      |      | 0.0             | ns   |
| $t_{ACO1}$ | Array clock to output delay            | C1 = 35 pF     |           | 20.0 |           | 25.0 | 25.0            | ns   |
| $t_{ODH}$  | Output data hold time after clock      | C1 = 35 pF (4) | 1.0       |      | 1.0       |      | 0.0             | ns   |
| $t_{ACNT}$ | Array clock maximum clock period       | (3)            |           | 20.0 |           | 25.0 | 0.0             | ns   |
| $f_{ACNT}$ | Maximum internal array clock frequency | (3)            | 50.0      |      | 40.0      |      | 0.0             | ns   |
| $f_{MAX}$  | Maximum clock frequency                | (5)            | 62.5      |      | 50.0      |      | 0.0             | MHz  |

**Table 29. EP1810-20 and EP1810-25 Internal Timing Parameters**

| Symbol    | Parameter                      | Conditions    | EP1810-20 |     | EP1810-25 |      | Non-Turbo Adder | Unit |
|-----------|--------------------------------|---------------|-----------|-----|-----------|------|-----------------|------|
|           |                                |               | Min       | Max | Min       | Max  | (2)             |      |
| $t_{IN}$  | Input pad and buffer delay     |               |           | 5.0 |           | 7.0  | 0.0             | ns   |
| $t_{IO}$  | I/O input pad and buffer delay |               |           | 2.0 |           | 3.0  | 0.0             | ns   |
| $t_{LAD}$ | Logic array delay              |               |           | 9.0 |           | 12.0 | 25.0            | ns   |
| $t_{OD}$  | Output buffer and pad delay    | C1 = 35 pF    |           | 6.0 |           | 6.0  | 0.0             | ns   |
| $t_{ZX}$  | Output buffer enable delay     | C1 = 35 pF    |           | 6.0 |           | 6.0  | 0.0             | ns   |
| $t_{XZ}$  | Output buffer disable delay    | C1 = 5 pF (6) |           | 6.0 |           | 6.0  | 0.0             | ns   |
| $t_{SU}$  | Register setup time            |               | 8.0       |     | 10.0      |      | 0.0             | ns   |
| $t_H$     | Register hold time             |               | 5.0       |     | 10.0      |      | 0.0             | ns   |
| $t_{IC}$  | Array clock delay              |               |           | 9.0 |           | 12.0 | 25.0            | ns   |
| $t_{ICS}$ | Global clock delay             |               |           | 4.0 |           | 5.0  | 0.0             | ns   |
| $t_{FD}$  | Feedback delay                 |               |           | 3.0 |           | 3.0  | -25.0           | ns   |
| $t_{CLR}$ | Register clear time            |               |           | 9.0 |           | 12.0 | 25.0            | ns   |

**Table 30. EP1810-35 & EP1810-45 External Timing Parameters** Notes (1)

| Symbol     | Parameter                              | Conditions     | EP1810-35 |      | EP1810-45 |      | Non-Turbo Adder | Unit |
|------------|----------------------------------------|----------------|-----------|------|-----------|------|-----------------|------|
|            |                                        |                | Min       | Max  | Min       | Max  | (3)             |      |
| $t_{PD1}$  | Input to non-registered output         | C1 = 35 pF     |           | 35.0 |           | 45.0 | 30.0            | ns   |
| $t_{PD2}$  | I/O input to non-registered output     | C1 = 35 pF     |           | 40.0 |           | 50.0 | 30.0            | ns   |
| $t_{SU}$   | Global clock setup time                |                | 25.0      |      | 30.0      |      | 30.0            | ns   |
| $t_H$      | Global clock hold time                 |                | 0.0       |      | 0.0       |      | 0.0             | ns   |
| $t_{CH}$   | Global clock high time                 |                | 12.0      |      | 15.0      |      | 0.0             | ns   |
| $t_{CL}$   | Global clock low time                  |                | 12.0      |      | 15.0      |      | 0.0             | ns   |
| $t_{CO1}$  | Global clock to output delay           | C1 = 35 pF     |           | 20.0 |           | 25.0 | 0.0             | ns   |
| $t_{CNT}$  | Minimum global clock period            | (3)            |           | 35.0 |           | 45.0 | 0.0             | ns   |
| $f_{CNT}$  | Maximum internal frequency             | (3)            | 28.6      |      | 22.2      |      | 0.0             | MHz  |
| $t_{ASU}$  | Array clock setup time                 |                | 10.0      |      | 11.0      |      | 30.0            | ns   |
| $t_{AH}$   | Array clock hold time                  |                | 15.0      |      | 18.0      |      | 0.0             | ns   |
| $t_{ACO1}$ | Array clock to output delay            | C1 = 35 pF     |           | 35.0 |           | 45.0 | 30.0            | ns   |
| $t_{ODH}$  | Output data hold time after clock      | C1 = 35 pF (4) | 1.0       |      | 1.0       |      |                 | ns   |
| $t_{ACNT}$ | Array clock maximum clock period       | (3)            |           | 35.0 |           | 45.0 | 0.0             | ns   |
| $f_{ACNT}$ | Maximum internal array clock frequency | (3)            | 28.6      |      | 22.2      |      | 0.0             | ns   |
| $f_{MAX}$  | Maximum clock frequency                | (5)            | 40        |      | 33.3      |      | 0.0             | MHz  |

**Table 31. EP1810-35 & EP1810-45 Internal Timing Parameters**

| Symbol    | Parameter                      | Conditions    | EP1810-35 |      | EP1810-45 |      | Non-Turbo Adder | Unit |
|-----------|--------------------------------|---------------|-----------|------|-----------|------|-----------------|------|
|           |                                |               | Min       | Max  | Min       | Max  | (2)             |      |
| $t_{IN}$  | Input pad and buffer delay     |               |           | 7.0  |           | 6.0  | 0.0             | ns   |
| $t_{IO}$  | I/O input pad and buffer delay |               |           | 5.0  |           | 5.0  | 0.0             | ns   |
| $t_{LAD}$ | Logic array delay              |               |           | 19.0 |           | 28.0 | 30.0            | ns   |
| $t_{OD}$  | Output buffer and pad delay    | C1 = 35 pF    |           | 9.0  |           | 11.0 | 0.0             | ns   |
| $t_{ZX}$  | Output buffer enable delay     | C1 = 35 pF    |           | 9.0  |           | 11.0 | 0.0             | ns   |
| $t_{XZ}$  | Output buffer disable delay    | C1 = 5 pF (6) |           | 9.0  |           | 11.0 | 0.0             | ns   |
| $t_{SU}$  | Register setup time            |               | 10.0      |      | 10.0      |      | 0.0             | ns   |
| $t_H$     | Register hold time             |               | 15.0      |      | 18.0      |      | 0.0             | ns   |
| $t_{IC}$  | Array clock delay              |               |           | 19.0 |           | 28.0 | 30.0            | ns   |
| $t_{ICS}$ | Global clock delay             |               |           | 4.0  |           | 8.0  | 0.0             | ns   |
| $t_{FD}$  | Feedback delay                 |               |           | 6.0  |           | 7.0  | -30.0           | ns   |
| $t_{CLR}$ | Register clear time            |               |           | 24.0 |           | 32.0 | 30.0            | ns   |

## Notes to tables:

- (1) These values are specified in [Table 24](#)
- (2) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.
- (3) Measured with a device programmed as four 12-bit counters.
- (4) Sample-tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Sample-tested only for an output change of 500 mV.

## Pin-Out Information

[Table 32](#) provides pin-out information for EP1810 devices in 68-pin PGA packages.

**Table 32. EP1810 PGA Pin-Outs**

| Pin | Function   | Pin | Function | Pin | Function | Pin | Function   |
|-----|------------|-----|----------|-----|----------|-----|------------|
| A2  | I/O        | B9  | I/O      | F10 | GND      | K4  | INPUT      |
| A3  | I/O        | B10 | I/O      | F11 | I/O      | K5  | INPUT      |
| A4  | I/O        | B11 | I/O      | G1  | I/O      | K6  | VCC        |
| A5  | INPUT      | C1  | I/O      | G2  | I/O      | K7  | INPUT      |
| A6  | CLK4/INPUT | C2  | I/O      | G10 | I/O      | K8  | INPUT      |
| A7  | CLK3/INPUT | C10 | I/O      | G11 | I/O      | K9  | I/O        |
| A8  | INPUT      | C11 | I/O      | H1  | I/O      | K10 | I/O        |
| A9  | I/O        | D1  | I/O      | H2  | I/O      | K11 | I/O        |
| A10 | I/O        | D2  | I/O      | H10 | I/O      | L2  | I/O        |
| B1  | I/O        | D10 | I/O      | H11 | I/O      | L3  | I/O        |
| B2  | I/O        | D11 | I/O      | J1  | I/O      | L4  | INPUT      |
| B3  | I/O        | E1  | I/O      | J2  | I/O      | L5  | CLK1/INPUT |
| B4  | INPUT      | E2  | I/O      | J10 | I/O      | L6  | CLK2/INPUT |
| B5  | INPUT      | E10 | I/O      | J11 | I/O      | L7  | INPUT      |
| B6  | VCC        | E11 | I/O      | K1  | I/O      | L8  | I/O        |
| B7  | INPUT      | F1  | I/O      | K2  | I/O      | L9  | I/O        |
| B8  | INPUT      | F2  | GND      | K3  | I/O      | L10 | I/O        |



### *Notes:*

Rochester EPLD devices normally sold in the un-configured state are tested using the original manufacturer's test software to guarantee the data sheet specifications. In some cases, EPLD devices can be configured to the customer's design and fully tested as such.

## EP600I Classic EPLD

### Features

- ❑ Formerly Intel's 5C060 device
- ❑ High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with  $t_{PD} = 45$  ns
  - Counter frequencies up to 22.2 MHz
  - Pipelined data rates up to 26.3 MHz
- ❑ Pin-, function-, and programming file-compatible with Altera's EP610 EPLDs
- ❑ Programmable I/O architecture with up to 20 inputs or 16 outputs
- ❑ Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- ❑ Available in windowed ceramic and one-time-programmable plastic packages:
  - 24-pin dual in-line packages (CerDIP and PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

## EP600I Classic EPLD

## Data Sheet Supplement

**Absolute Maximum Ratings** See *Operating Requirements for Altera Devices* in the current Altera **Data Book**.

| Symbol    | Parameter           | Conditions     | Min  | Max            | Unit |
|-----------|---------------------|----------------|------|----------------|------|
| $V_{CC}$  | Supply voltage      | Note (1)       | -2.0 | 7.0            | V    |
| $V_I$     | DC input voltage    | Notes (1), (2) | -0.5 | $V_{CC} + 0.5$ | V    |
| $T_{STG}$ | Storage temperature |                | -65  | 150            | °C   |
| $T_{AMB}$ | Ambient temperature | Note (3)       | -10  | 85             | °C   |

## Recommended Operating Conditions

| Symbol   | Parameter             | Conditions         | Min  | Max      | Unit |
|----------|-----------------------|--------------------|------|----------|------|
| $V_{CC}$ | Supply voltage        |                    | 4.75 | 5.25     | V    |
| $V_I$    | Input voltage         |                    | 0    | $V_{CC}$ | V    |
| $V_O$    | Output voltage        |                    | 0    | $V_{CC}$ | V    |
| $T_A$    | Operating temperature | For commercial use | 0    | 70       | °C   |
| $T_A$    | Operating temperature | For industrial use | -40  | 85       | °C   |
| $T_C$    | Case temperature      | For military use   | -55  | 125      | °C   |
| $t_R$    | Input rise time       | Note (4)           |      | 500      | ns   |
| $t_F$    | Input fall time       | Note (4)           |      | 500      | ns   |

## DC Operating Conditions Note (5)

| Symbol    | Parameter                                    | Conditions                                                                      | Min  | Typ | Max            | Unit |
|-----------|----------------------------------------------|---------------------------------------------------------------------------------|------|-----|----------------|------|
| $V_{IH}$  | High-level input voltage                     | Note (6)                                                                        | 2.0  |     | $V_{CC} + 0.3$ | V    |
| $V_{IL}$  | Low-level input voltage                      | Note (6)                                                                        | -0.3 |     | 0.8            | V    |
| $V_{OH}$  | High-level output voltage                    | $I_{OH} = -4$ mA DC, $V_{CC} = \min$                                            | 2.4  |     |                | V    |
| $V_{OL}$  | Low-level output voltage                     | $I_{OL} = 4$ mA DC, $V_{CC} = \min$                                             |      |     | 0.45           | V    |
| $I_I$     | Input leakage current                        | $V_{CC} = \max$ , $GND < V_{IN} < V_{CC}$                                       | -10  |     | 10             | μA   |
| $I_{OZ}$  | Tri-state output off-state current           | $V_{CC} = \max$ , $GND < V_{OUT} < V_{CC}$                                      | -10  |     | 10             | μA   |
| $I_{CC1}$ | $V_{CC}$ supply current (non-turbo, standby) | $V_{CC} = \max$ , $V_{IN} = V_{CC}$ or GND, Note (7)                            |      | 50  | 100            | μA   |
| $I_{CC2}$ | $V_{CC}$ supply current (non-turbo, active)  | $V_{CC} = \max$ , $V_{IN} = V_{CC}$ or GND, no load, $f_{IN} = 1$ MHz, Note (8) |      | 10  | 15             | mA   |

## Capacitance Note (5)

| Symbol     | Parameter            | Conditions                     | Min | Max | Unit |
|------------|----------------------|--------------------------------|-----|-----|------|
| $C_{IN}$   | Input capacitance    | $V_{IN} = 0$ V, $f = 1.0$ MHz  |     | 20  | pF   |
| $C_{OUT}$  | Output capacitance   | $V_{OUT} = 0$ V, $f = 1.0$ MHz |     | 20  | pF   |
| $C_{CLK1}$ | CLK1 pin capacitance | $V_{IN} = 0$ V, $f = 1.0$ MHz  |     | 20  | pF   |
| $C_{CLK2}$ | CLK2 pin capacitance | $V_{IN} = 0$ V, $f = 1.0$ MHz  |     | 50  | pF   |

# EP610-910-1810

Data Sheet Supplement

EP600I Classic EPLD

## AC Operating Conditions Note (5)

| External Timing Parameters |                                    |            | EP600I-45 |     | EP600I-55 |     | Non-Turbo Adder |      |
|----------------------------|------------------------------------|------------|-----------|-----|-----------|-----|-----------------|------|
| Symbol                     | Parameter                          | Conditions | Min       | Max | Min       | Max | Note (9)        | Unit |
| $t_{PD1}$                  | Input to non-registered output     |            |           | 43  |           | 53  | 25              | ns   |
| $t_{PD2}$                  | I/O input to non-registered output |            |           | 45  |           | 55  | 25              | ns   |
| $t_{PZX}$                  | Input to output enable             | Note (10)  |           | 45  |           | 55  | 25              | ns   |
| $t_{PXZ}$                  | Input to output disable            | Note (10)  |           | 45  |           | 55  | 25              | ns   |
| $t_{CLR}$                  | Asynchronous output clear time     |            |           | 45  |           | 55  | 25              | ns   |

| Global Clock Mode |                            |            | EP600I-45 |     | EP600I-55 |     | Non-Turbo Adder |      |
|-------------------|----------------------------|------------|-----------|-----|-----------|-----|-----------------|------|
| Symbol            | Parameter                  | Conditions | Min       | Max | Min       | Max | Note (9)        | Unit |
| $f_{MAX}$         | Maximum frequency          |            | 26.3      |     | 23.3      |     | 0               | MHz  |
| $t_{SU1}$         | Input setup time           |            | 36        |     | 41        |     | 25              | ns   |
| $t_{SU2}$         | I/O setup time             |            | 38        |     | 43        |     | 25              | ns   |
| $t_H$             | Input hold time            |            | 0         |     | 0         |     | 0               | ns   |
| $t_{CH}$          | Clock high time            |            | 17.5      |     | 21.5      |     | 0               | ns   |
| $t_{CL}$          | Clock low time             |            | 17.5      |     | 21.5      |     | 0               | ns   |
| $t_{CO}$          | Clock to output delay      |            |           | 22  |           | 25  | 0               | ns   |
| $t_{CNT}$         | Minimum clock period       |            |           | 45  |           | 55  | 25              | ns   |
| $f_{CNT}$         | Internal maximum frequency |            | 22.2      |     | 18.2      |     | 0               | MHz  |

| Array Clock Mode |                            |            | EP600I-45 |     | EP600I-55 |     | Non-Turbo Adder |      |
|------------------|----------------------------|------------|-----------|-----|-----------|-----|-----------------|------|
| Symbol           | Parameter                  | Conditions | Min       | Max | Min       | Max | Note (9)        | Unit |
| $f_{MAX}$        | Maximum frequency          |            | 28.6      |     | 23.3      |     | 0               | MHz  |
| $t_{ASU1}$       | Input setup time           |            | 10        |     | 10        |     | 25              | ns   |
| $t_{ASU2}$       | I/O setup time             |            | 12        |     | 12        |     | 25              | ns   |
| $t_{AH}$         | Input hold time            |            | 15        |     | 15        |     | 0               | ns   |
| $t_{ACH}$        | Clock high time            |            | 17.5      |     | 21.5      |     | 25              | ns   |
| $t_{ACL}$        | Clock low time             |            | 17.5      |     | 21.5      |     | 25              | ns   |
| $t_{ACO}$        | Clock to output delay      |            |           | 50  |           | 58  | 25              | ns   |
| $t_{ACNT}$       | Minimum clock period       |            |           | 45  |           | 55  | 25              | ns   |
| $f_{ACNT}$       | Internal maximum frequency |            | 22.2      |     | 18.2      |     | 0               | MHz  |

**Notes to tables:**

- (1) Voltage is with respect to GND.
- (2) The minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to +7.0 V for periods less than 20 ns under no-load conditions.
- (3) This parameter is under bias. Extended temperature versions are also available.
- (4) For all Clocks:  $t_R$  and  $t_F = 250$  ns (maximum).
- (5) Operating conditions:  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 5\%$  for commercial use.  
 $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$  for industrial use.  
 $T_C = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$  for military use.
- (6) Absolute values with respect to device GND; all over- and undershoots due to system or tester noise are included.
- (7) When the Turbo Bit is not set (non-turbo mode), device enters standby mode approximately 100 ns after the last input transition.
- (8) Measured with a device programmed as a 16-bit counter.
- (9) When the Turbo Bit is not set (non-turbo mode), the non-turbo adder values must be added to the appropriate AC parameter to determine worst-case timing.
- (10) The  $t_{PZX}$  and  $t_{PXZ}$  parameters are measured at  $\pm 0.5\text{ V}$  from steady state voltage as driven by the output load specification;  $t_{PZX}$  is measured with  $C_L = 5\text{ pF}$ .

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