MP4562

60V, 2A Step-Down Converter with Configurable Frequency Up to 2.5MHz in a TSOT23-8 Package

DESCRIPTION

The MP4562 is a configurable-frequency, step-down converter with an integrated, high-voltage high-side MOSFET (HS-FET). It provides up to 2A of output current (I_{OUT}) across a 4.5V to 60V input voltage (V_{IN}) range.

Peak current mode control with internal compensation provides fast transient response and easy loop design. It supports a wide 100kHz to 2.5MHz switching frequency (f_{SW}) range. The device provides a small-sized, high-efficiency solution for a wide variety of step-down applications.

The MP4562 features cycle-by-cycle current limit (I_{LIMIT}) foldback and frequency foldback, which protects against overload and short circuit conditions, regardless of whether V_{IN} is high. The frequency stretch-down function improves efficiency and reduces the output voltage (V_{OUT}) ripple (ΔV_{OUT}).

The MP4562 is available in a space-saving TSOT23-8 package.

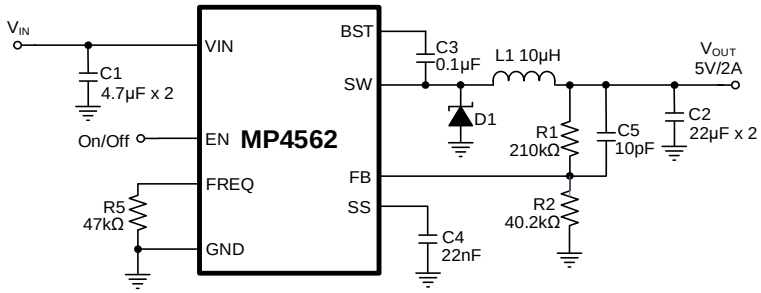
FEATURES

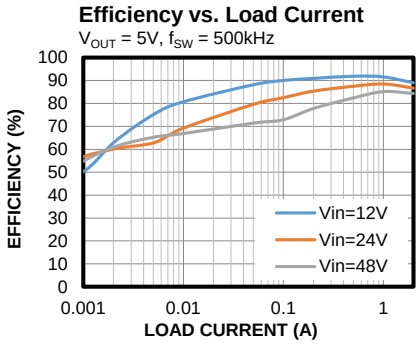
- 4.5V to 60V Input Voltage (V_{IN}) Range
- 0.8V to 30V Output Voltage (V_{OUT}) Range
- 30μA Low Quiescent Current (I_Q)
- 99% Duty Low-Dropout Regulation
- 120mΩ Integrated, Internal High-Side MOSFET (HS-FET)
- 100kHz to 2.5MHz Switching Frequency (f_{SW})
- Internal Loop Compensation
- Configurable External Soft Start (SS)
- Configurable Accurate Under-Voltage Lockout (UVLO) Hysteresis
- Short-Circuit Protection (SCP) with Frequency Foldback and Current Limit (I_{LIMIT}) Foldback
- Feedback (FB) Over-Voltage Protection (OVP) (FB OVP Threshold = 110% of V_{REF})
- Over-Temperature Protection (OTP) (OTP Rising Threshold = 150°C)
- Available in a TSOT23-8 Package

APPLICATIONS

- Non-Isolated Power over Ethernet (PoE) Powered Devices (PD) Power Supplies
- Industrial Power Systems
- Telecom and Data Communication Systems
- General, Wide-Input Voltage Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4562GJ	TSOT23-8	*See Below*	1

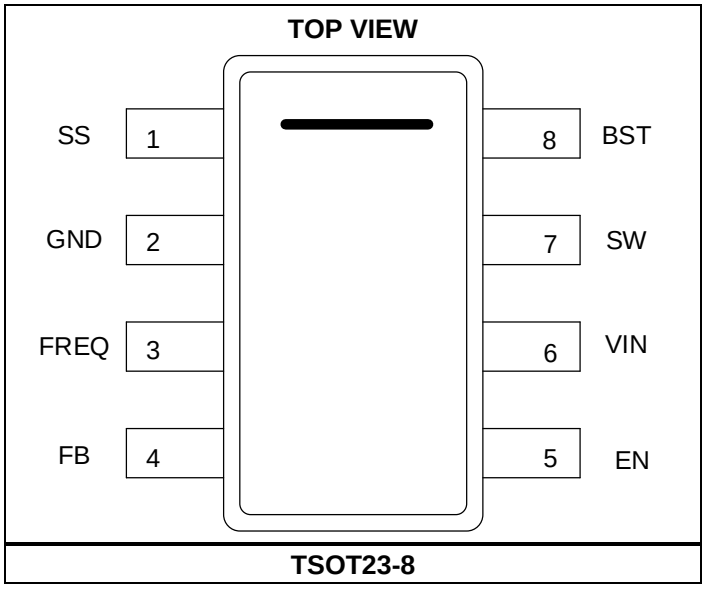
* For Tape & Reel, add suffix -Z (e.g. MP4562GJ-Z).

TOP MARKING

BQCY

BQ: Product code of MP4562GJ
C: Country of origin code
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	SS	**Soft start control**. Connect a capacitor between the SS and GND pins to configure the soft-start time (t_{SS}).
2	GND	**System ground**. The GND pin is the reference ground of the regulated output voltage (V_{OUT}).
3	FREQ	**Switching frequency setting.** Connect an external resistor between the FREQ and GND pins to set the switching frequency (f_{SW}).
4	FB	**Output voltage feedback.** Connect a resistor divider between the output voltage (V_{OUT}) and the feedback (FB) pin.
5	EN	**Enable.** Pull the enable (EN) pin high to turn the converter on; pull EN low to turn it off. When EN is floating, the MP4562 can be enabled via the pull-up current from VIN.
6	VIN	**Power supply input.** Place a decoupling capacitor connected to ground close to the VIN pin to reduce switching spikes.
7	SW	**Converter switching node**. Connect the SW pin to the source of the internal high-side MOSFET (HS-FET). Place a low-forward voltage Schottky rectifier connected to ground close to the SW pin to reduce switching spikes.
8	BST	**Bootstrap power for the HS-FET gate driver**. Connect a 0.1μF capacitor between the BST and SW pins.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{EN} ..... -0.3V to +65V
V_{SW} ..... -0.5V to +65V
V_{SW} (<5ns) ..... -4V to +66V
BST to SW ..... -0.3V to +6.5V
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) (4) 2W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±1500V

Recommended Operating Conditions (3)

Input voltage (V_{IN}) ..... 4.5V to 60V
Output voltage (V_{OUT}) ..... 0.8V to 0.99 x V_{IN} or 30V max
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
EV4562-J-00A (4)	61	7.7	°C/W
TSOT23-8 (5)	100	55	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the converter to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV4562-J-00A (51mmx51mm), 1oz, 2-layer PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48 V, T_J = -40°C to +125°C [6], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	V_{UVLO_RISING}	V_{IN} rising		4.2	4.4	V
V_{IN} UVLO hysteresis	V_{UVLO_HYS}			0.4		V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on the VIN pin		1	2	μA
Quiescent current	I_Q	V_{FB} = 0.82V, no switching, measured on the VIN pin		30	40	μA
Enable (EN) Control						
EN rising threshold	V_{EN_RISING}	V_{EN} rising, micropower mode			1	V
EN falling threshold	$V_{EN\_FALLING}$	V_{EN} falling, micropower mode	0.2			V
EN start-up threshold	V_{EN_SU}	V_{EN} rising, switching	1.1	1.2	1.3	V
EN pull-up current	I_{EN}	V_{EN} < V_{EN_SU}		0.25		μA
		V_{EN} > V_{EN_SU}		3.8		μA
EN start-up delay [7]		EN on to IC switching, C_{SS} = 22nF		650		μs
Switching Frequency (f_{SW})						
Switching Frequency	f_{SW}	R_{FREQ} = 47kΩ	450	500	600	kHz
		R_{FREQ} = 20kΩ	900	1000	1200	kHz
Foldback frequency		f_{SW} = 500kHz, V_{FB} = 0V		50		kHz
Minimum on time [7]	t_{ON_MIN}			90		ns
Minimum off time [7]	t_{OFF_MIN}	V_{FB} = 0V		100		ns
Feedback (FB) Reference Voltage (V_{REF})						
Reference voltage	V_{REF}	V_{IN} = 4.5V to 60V, T_J = 25°C	0.792	0.8	0.808	V
		V_{IN} = 4.5V to 60V, T_J = -40°C to +125°C	0.788	0.8	0.812	V
FB input current	I_{FB}	V_{FB} = 0.82V			50	nA
Soft start (SS) current	I_{SS}		3.8	4.8	5.8	μA
Under-voltage protection (UVP) threshold [7]	V_{UVP}	Frequency foldback and I_{LIMIT} foldback threshold		50		% of V_{REF}
FB over-voltage protection (OVP) threshold	V_{OVP}	IC stops switching	105	110	115	% of V_{REF}
FB OVP recovery threshold			102	107	112	% of V_{REF}
Power MOSFET						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)}$	V_{BST} - V_{SW} = 5V		120		mΩ
Current Limit (I_{LIMIT})						
Switching peak I_{LIMIT}			3	3.6	4.5	A
Foldback I_{LIMIT}		V_{FB} = 0V		1.8		A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 48 V, T_J = -40°C to +125°C [6], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Over-Temperature Protection (OTP)						
OTP rising threshold [7]				150		°C
OTP hysteresis [7]				20		°C

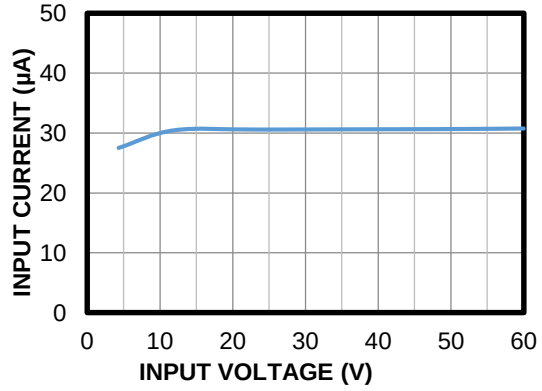
Notes:

6) Guaranteed by over-temperature correlation. Not tested in production.
7) Guaranteed by sample characterization. Not tested in production.

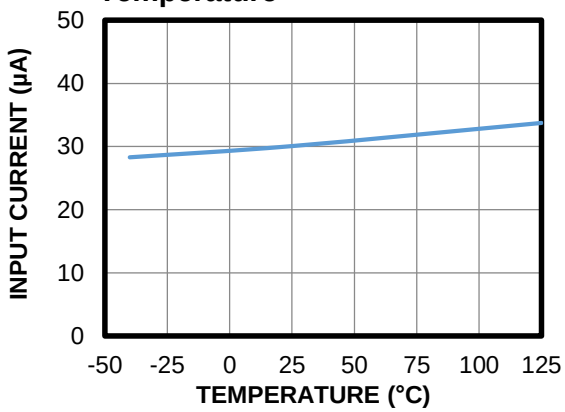
TYPICAL CHARACTERISTICS

V_{IN} = 48V, T_A = 25°C, unless otherwise noted.

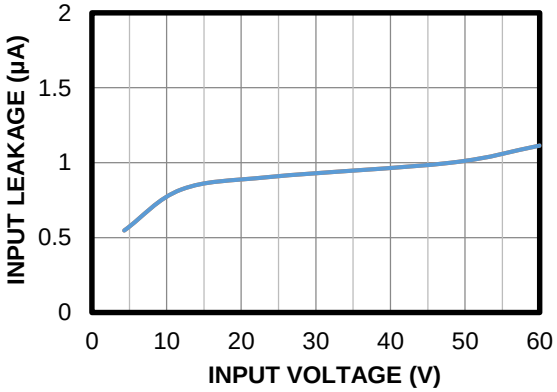
Quiescent Current vs. Input Voltage



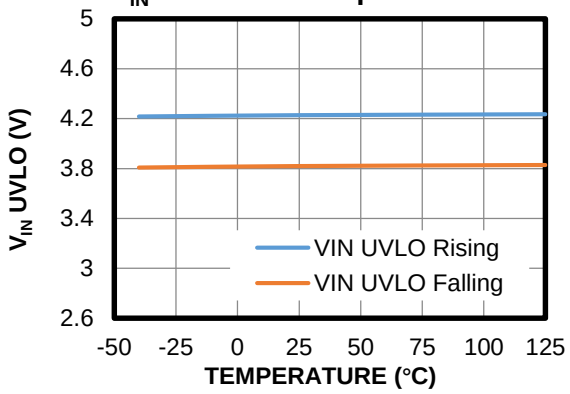
Quiescent Current vs. Temperature



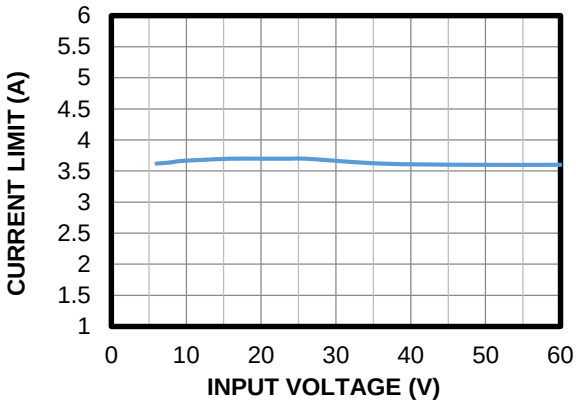
Shutdown Current vs. Input Voltage



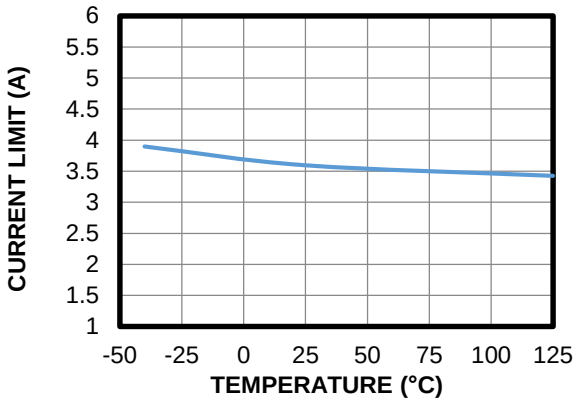
V_{IN} UVLO vs. Temperature



Current Limit vs. Input Voltage



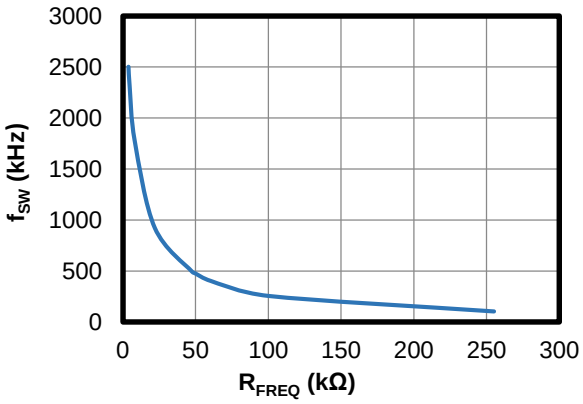
Current Limit vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

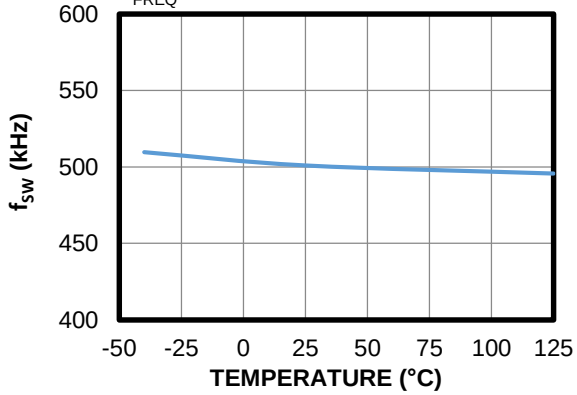
V_{IN} = 48V, T_A = 25°C, unless otherwise noted.

Switching Frequency vs. R_{FREQ}

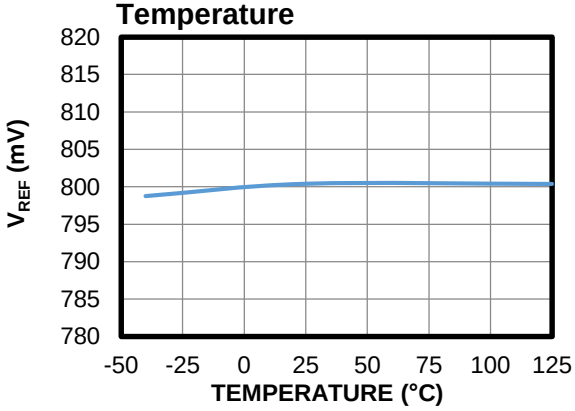


Switching Frequency vs. Temperature

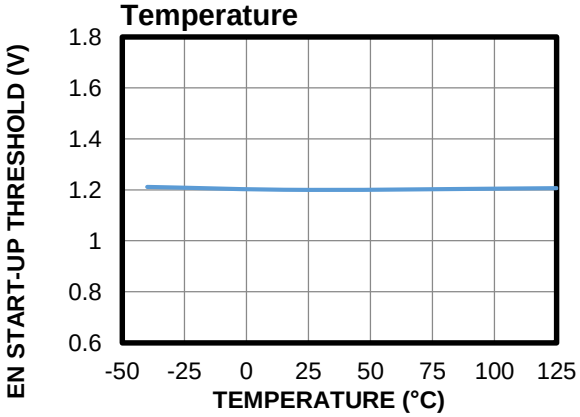
R_{FREQ} = 47kΩ



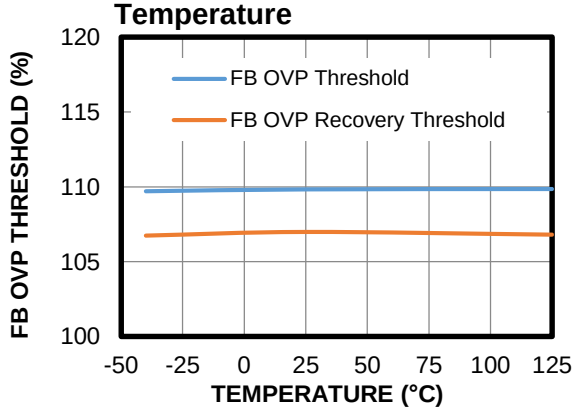
Reference Voltage vs. Temperature



EN Start-Up Threshold vs. Temperature



FB OVP Threshold vs. Temperature

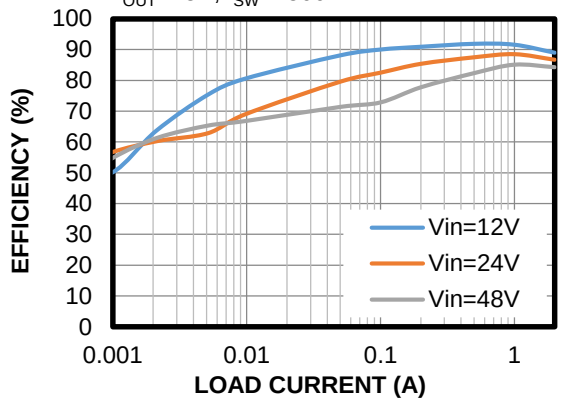


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, V_{OUT} = 5V, L = 10µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

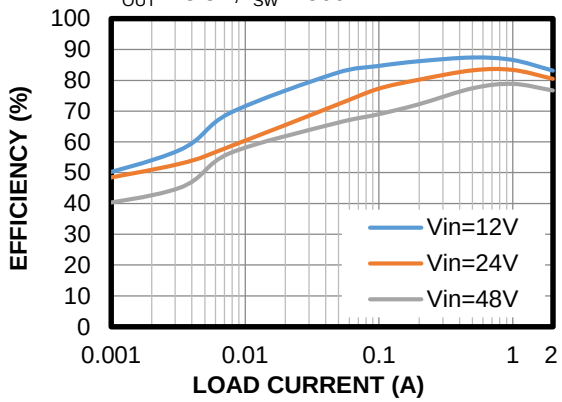
Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 500kHz



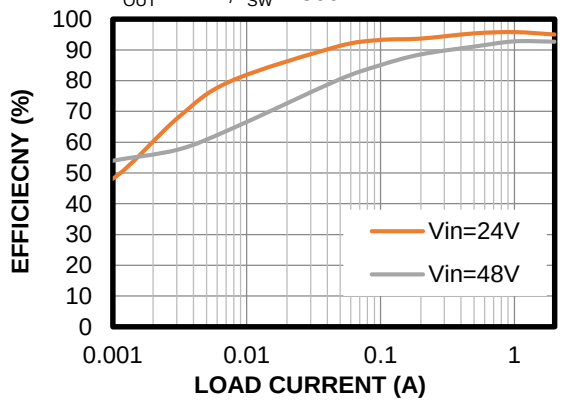
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 500kHz

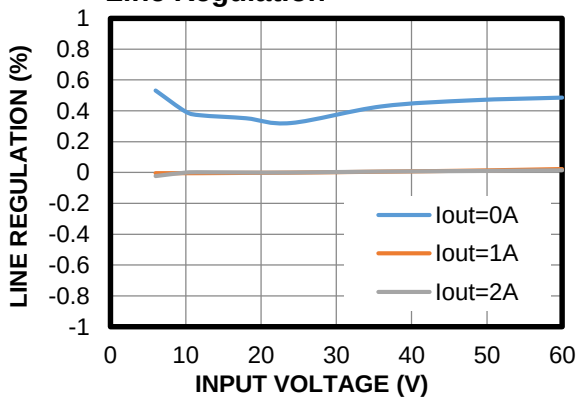


Efficiency vs. Load Current

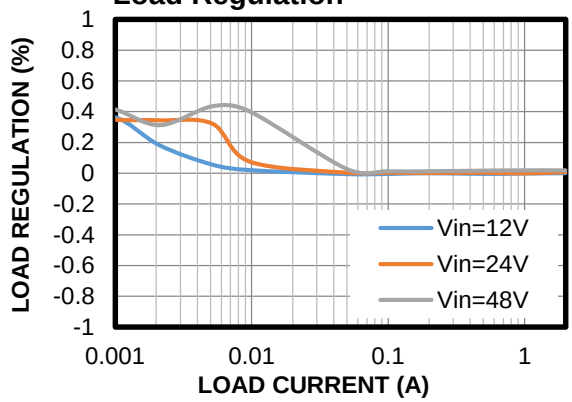
V_{OUT} = 12V, f_{SW} = 500kHz



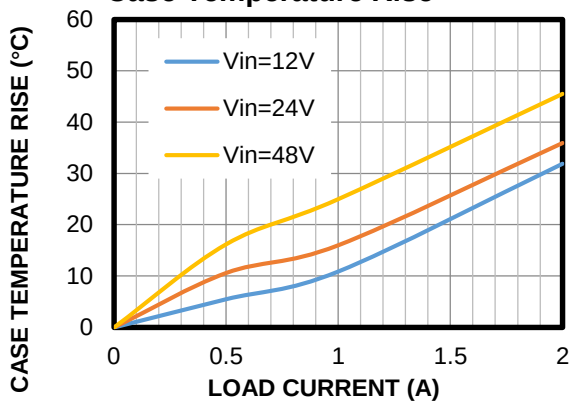
Line Regulation



Load Regulation



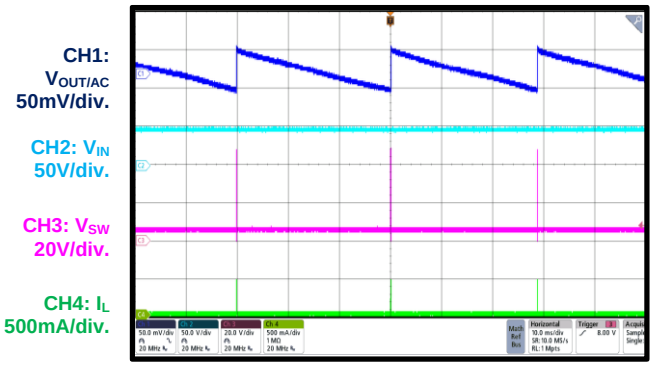
Case Temperature Rise



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

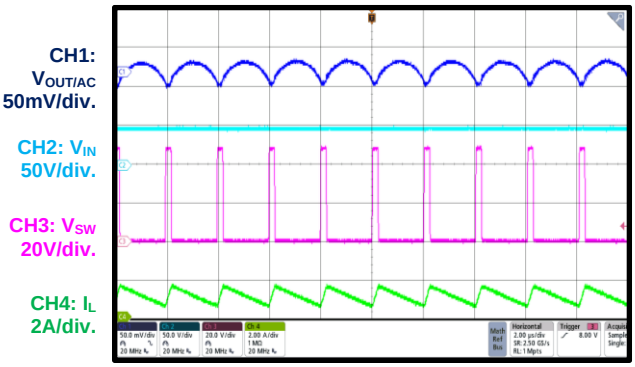
V_{IN} = 48V, V_{OUT} = 5V, L = 10µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

Steady State
I_{OUT} = 0A



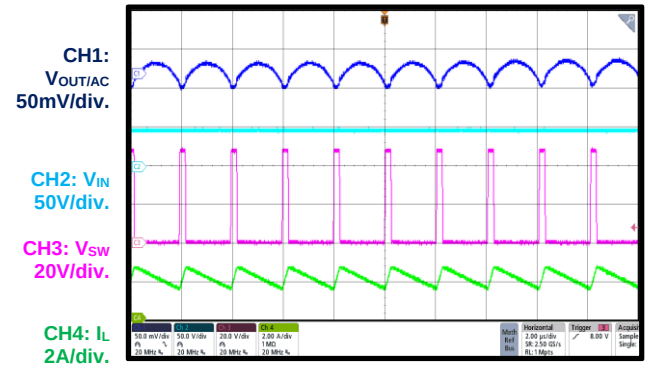
10ms/div.

Steady State
I_{OUT} = 1A



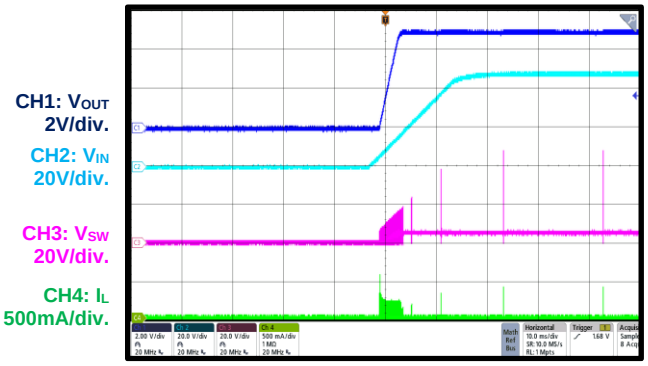
2 µ s/div

Steady State
I_{OUT} = 2A



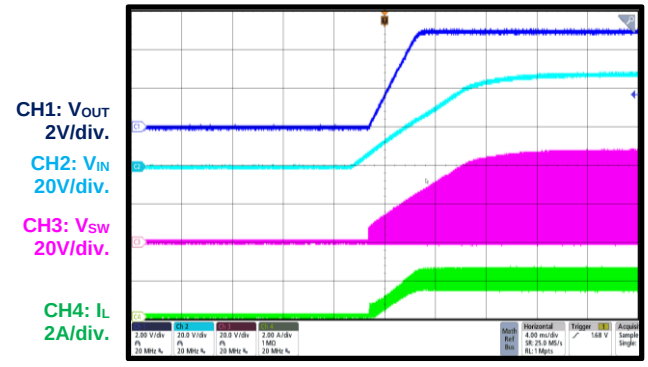
2µs/div.

Start-Up through VIN
I_{OUT} = 0A



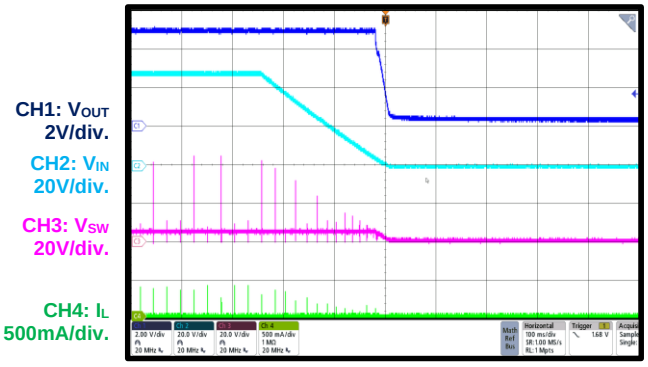
10ms/div.

Start-Up through VIN
I_{OUT} = 2A



4ms/div.

Shutdown through VIN
I_{OUT} = 0A



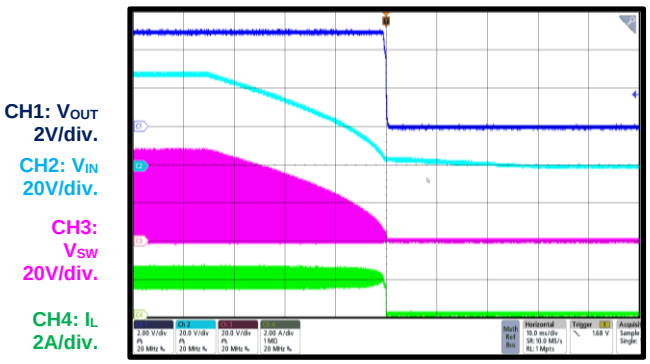
100ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 5V, L = 10µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

Shutdown through VIN

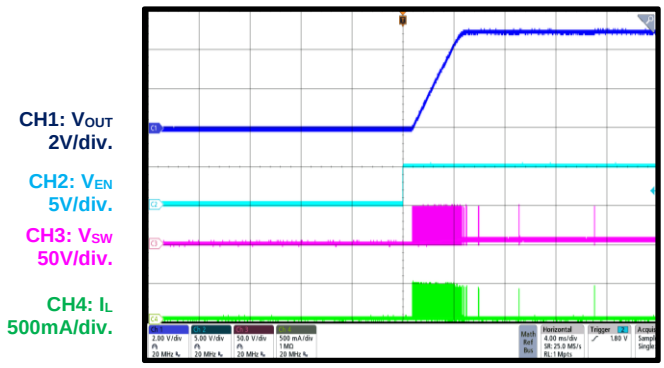
I_{OUT} = 2A



10ms/div.

Start-Up through EN

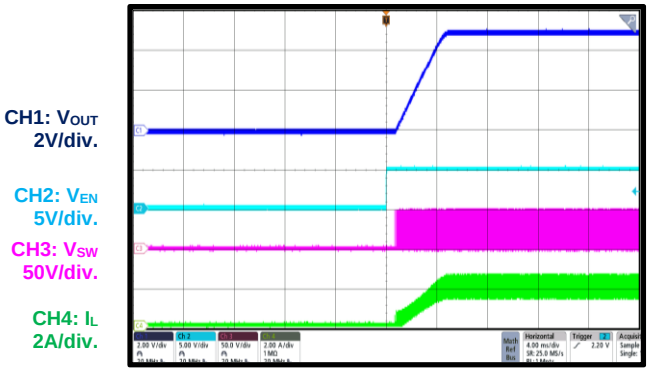
I_{OUT} = 0A



4ms/div.

Start-Up through EN

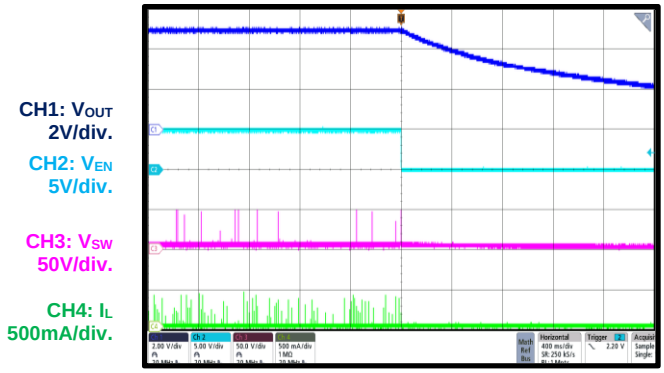
I_{OUT} = 2A



4ms/div.

Shutdown through EN

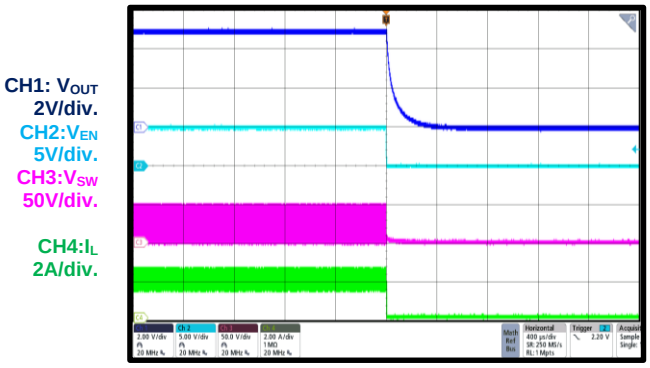
I_{OUT} = 0A



400ms/div.

Shutdown through EN

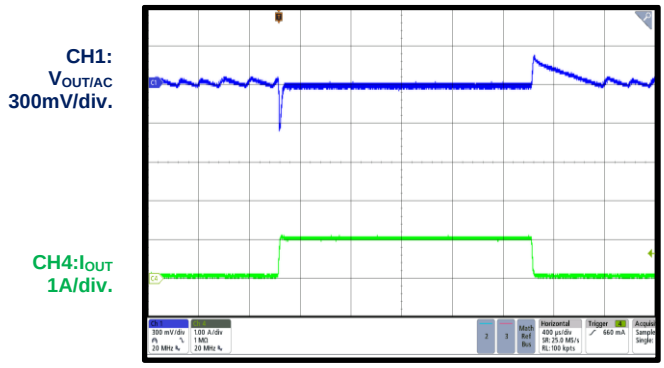
I_{OUT} = 2A



400µs/div.

Load Transient

I_{OUT} = 0A to 1A, slew rate = 100mA/µs



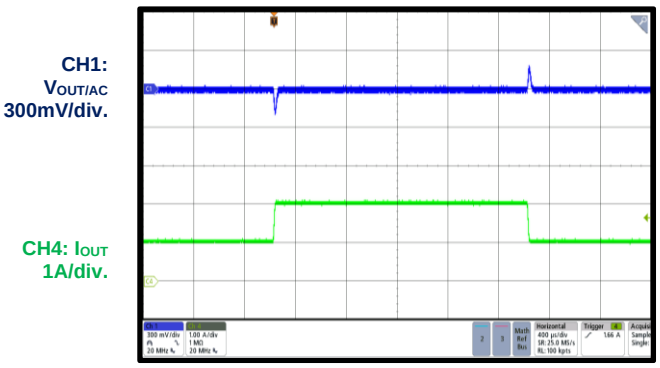
400µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 5V, L = 10µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

Load Transient

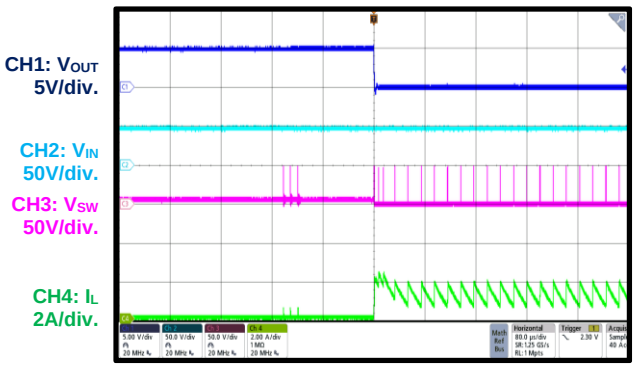
I_{OUT} = 1A to 2A, slew rate = 100mA/µs



400µs/div.

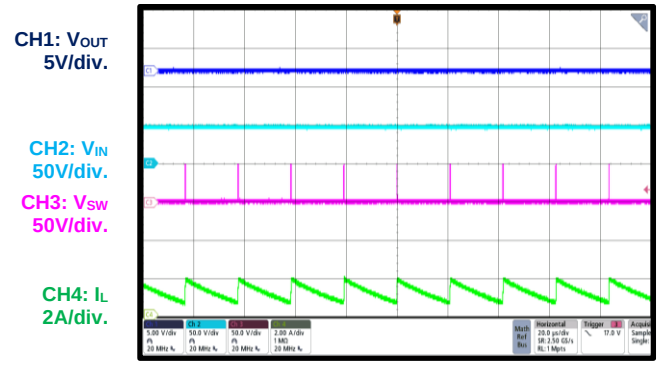
SCP Entry

I_{OUT} = 0A



80µs/div.

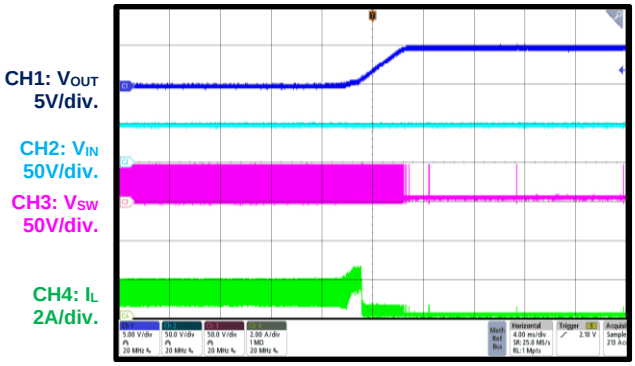
SCP Steady State



20µs/div.

SCP Recovery

I_{OUT} = 0A



4ms/div.

FUNCTIONAL BLOCK DIAGRAM

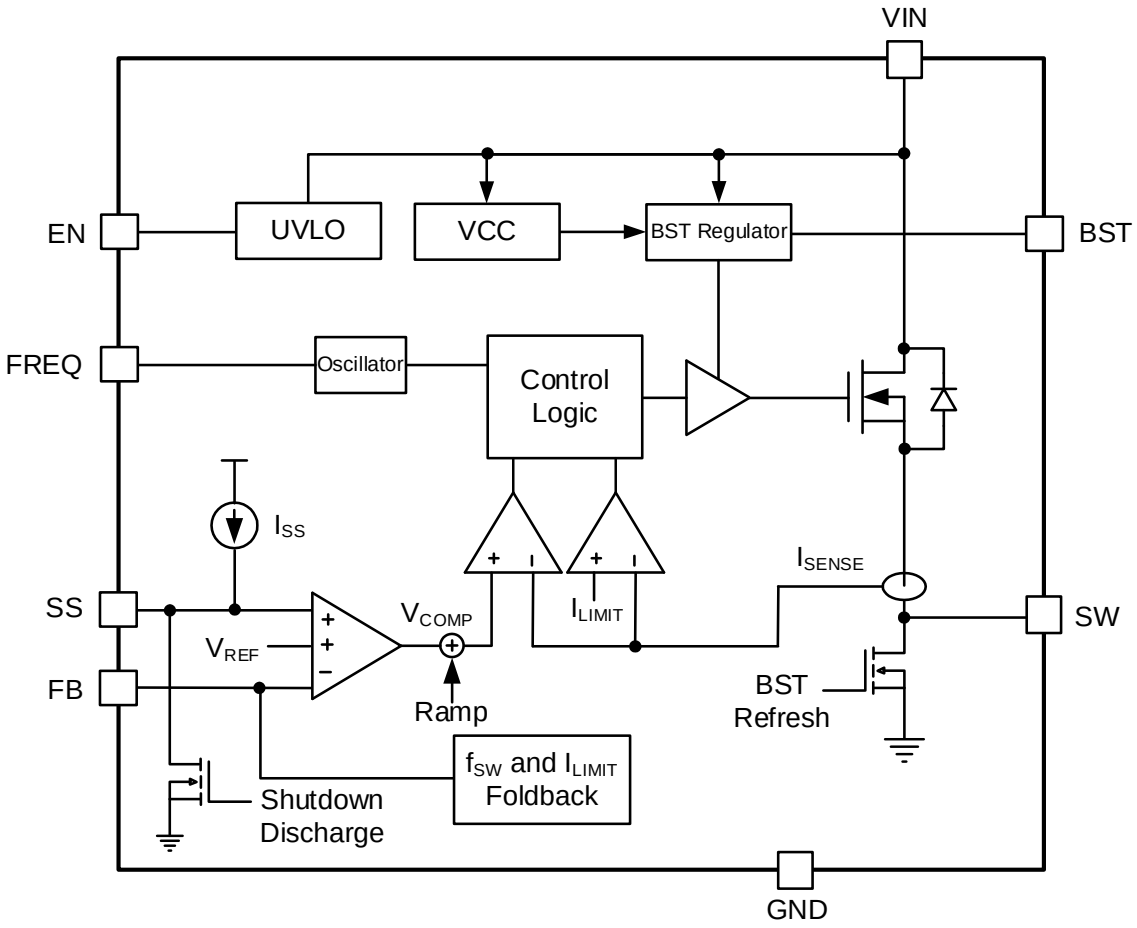


Figure 1: Functional Block Diagram

OPERATION

The MP4562 is a configurable-frequency, non-synchronous, step-down switching converter with an integrated, high-voltage high-side power MOSFET (HS-FET). It provides a high-efficiency solution with current mode control for fast loop response. The device features a wide input voltage (V_{IN}) range, configurable soft start (SS), and precise current limiting.

Figure 1 on page 12 shows the MP4562's functional block diagram. The MP4562's detailed functions are described below.

Peak Current Mode Control

The MP4562 operates in fixed-frequency, peak current control mode to regulate the output voltage (V_{OUT}). First a pulse-width modulation (PWM) cycle is initiated by the internal clock, then the HS-FET turns on and remains on until its current (I_{HS}) reaches the value set by the internal comparator voltage (V_{COMP}). When the HS-FET turns off, it remains off for at least 100ns before the next cycle starts. If I_{HS} does not reach the value set by V_{COMP} in one PWM period, then the HS-FET remains on, saving a turn-off operation.

The MP4562 has an internal error amplifier (EA) that compares the feedback (FB) voltage (V_{FB}) and the internal reference voltage (V_{REF}) to output a voltage proportional to the difference between the two inputs. The EA's output is V_{COMP}, which is used to control I_{HS}.

The MP4562 features internal ramp compensation for the sensed current signal, which prevents subharmonic oscillations at >50% duty cycles.

Light-Load Operation

Under light-load conditions, V_{COMP} decreases as the switching frequency (f_{SW}) stretched down to reduce switching and driver losses. The final frequency at no load can be almost 0Hz before the device enters power-saving sleep mode.

Under-Voltage Lockout (UVLO) Protection

Under-voltage lockout (UVLO) is implemented to protect the device from operating at an insufficient V_{IN}. The UVLO rising threshold is about 4.2V, and its falling threshold is 3.8V.

Enable (EN) and Configurable UVLO

The MP4562 has a dedicated enable (EN) control pin. If applying an EN voltage (V_{EN}) above the EN rising threshold (1V max), the MP4562 starts up some of the internal circuitry (micropower mode). If V_{EN} exceeds the start-up threshold (1.2V), the MP4562 enables all functions and starts switching. Switching is disabled when V_{EN} drops below 1.2V. To completely shut down the MP4562, pull V_{EN} below 0.2V. EN is compatible with voltages up to 60V. For automatic start-up, float EN or connect EN to VIN directly.

The MP4562 features a configurable UVLO hysteresis. If V_{EN} is below 1.2V, then EN is pulled up by an internal current (0.25µA). Once V_{EN} exceeds 1.2V, an additional current (3.55µA) pulls EN pin high (for a total current of 3.8µA), which generates the UVLO hysteresis – determined by the bottom resistor (R_{BOT}) (see Figure 2).

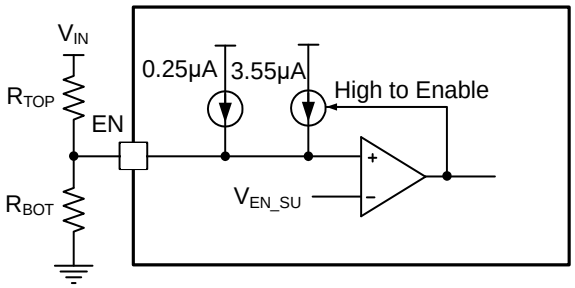


Figure 2: V_{IN} VULO Configuration

The V_{IN} start-up threshold (V_{IN_SU}) can be calculated with Equation (1):

$$V_{IN\_SU}=\frac{(R_{TOP}+R_{BOT})\times V_{EN\_SU}}{R_{BOT}}-0.25\mu A\times R_{TOP} \quad (1)$$

Where V_{EN_SU} is the EN start-up threshold (typically 1.2V).

Once V_{EN} reaches V_{EN_SU}, the additional 3.55µA source current turns on to create a reverse hysteresis for the V_{IN} UVLO. The V_{IN} UVLO hysteresis ($V_{IN\_UVLO\_HYS}$) can be calculated with Equation (2):

$$V_{IN\_UVLO\_HYS}=3.55\mu A\times R_{TOP} \quad (2)$$

Soft Start (SS)

Once the MP4562 is enabled, a soft start (SS) is initiated to start up the converter. The soft-start voltage (V_{SS}) is controlled by charging the SS pin from 0V, then comparing V_{SS} to the internal V_{REF}. The lower value is fed to the EA to control V_{OUT}. Once V_{SS} exceeds V_{REF}, soft start is complete, and V_{REF} takes control of FB loop regulation.

If there is an output bias, the MP4562 stops switching until V_{SS} exceeds V_{FB}, which is proportional to the bias V_{OUT}.

Once the device is enabled, the SS pin is charged by an internal soft-start current (I_{SS}) (4.8μA). The soft-start time (t_{SS}) set by the external soft-start capacitor (C_{SS}) can be calculated with Equation (3):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (3)$$

Where V_{REF} is the internal reference voltage (0.8V).

Switching Frequency (f_{SW})

Selecting f_{SW} is a tradeoff between efficiency and component size. Low-frequency operation increases efficiency by reducing MOSFET switching losses; however, low-frequency operation requires larger inductance and capacitance to maintain a low V_{OUT} ripple (ΔV_{OUT}).

f_{SW} can be set by the FREQ pin. The FREQ resistor (R_{FREQ}) can be calculated with Equation (4):

$$R_{FREQ}(k\Omega) = \frac{26500}{f_{SW}(kHz)} - 6 \quad (4)$$

For example, if f_{SW} is 500kHz, then R_{FREQ} should be 47kΩ. This f_{SW} (500kHz) is set under heavy-load conditions in continuous work mode. Under light-load or short-circuit conditions, f_{SW} stretches down.

f_{SW} can be set between 100kHz and 2.5MHz.

Minimum On Time and Minimum Off Time

The MP4562 blanks the MOSFET's on state for 90ns in each cycle to improve noise immunity. If the minimum on time (t_{ON_MIN}) (90ns) is triggered with a small V_{OUT} to V_{IN} ratio or a high f_{SW}, V_{COMP} drops and activates the frequency stretch-down logic, which decreases f_{SW} to regulate V_{OUT}.

The MP4562 also blanks the MOSFET's off state with a minimum off time (t_{OFF_MIN}) in each cycle. During t_{OFF_MIN}, the MOSFET does not turn on. If the MOSFET is on, and the inductor current (I_L) does not trigger V_{COMP} in the same period (which typically occurs when the V_{OUT} to V_{IN} ratio is too large), then t_{OFF_MIN} is ignored.

If V_{IN} continues to decrease after t_{OFF_MIN}, f_{SW} folds back gradually until the V_{OUT} to V_{IN} ratio reaches about 99%. This guarantees low dropout from V_{IN} to V_{OUT}.

Overload Protection (OLP) and Short-Circuit Protection (SCP)

The MP4562 features a fixed, cycle-by-cycle peak switching current limit (I_{LIMIT}). In each cycle, the internal current-sense circuit monitors I_{HS}. Once the sensed current reaches the I_{LIMIT} threshold, the HS-FET turns off. I_{HS} is blanked internally for about 90ns to improve noise immunity.

I_{LIMIT} is constant for all duty cycles without ramp compensation, which provides a constant I_{LIMIT} across the wide V_{IN} range.

During an overload fault, I_L is limited cycle-by-cycle, and V_{OUT} decreases. If V_{OUT} continues to decrease during an overload condition, both f_{SW} and I_{LIMIT} decrease when V_{FB} drops below 50% of V_{REF}. f_{SW} and I_{LIMIT} decrease smoothly as V_{FB} drops. During a short-circuit fault, V_{OUT} and V_{FB} are pulled to 0V, f_{SW} decreases to 1/10 of its value set by R_{FREQ}, and I_{LIMIT} folds back to 1/2 of the typical I_{LIMIT}. Once V_{FB} is high enough, the f_{SW} and I_{LIMIT} return to their set values.

Over-Voltage Protection (OVP)

The MP4562 monitors V_{FB} to detect whether an over-voltage (OV) fault has occurred. Once V_{FB} exceeds 110% of its target voltage, the converter stops switching. The MP4562 recovers to normal loop control once V_{OUT} drops to 107% of the regulation voltage. This prevents V_{OUT} from dropping further once it reaches 100% of the regulation.

Bootstrap (BST) Power Supply

An external bootstrap (BST) capacitor (C_{BST}) powers the HS-FET driver, and C_{BST} is powered by the VIN pin. Once the difference between the

BST voltage (V_{BST}) and the SW voltage (V_{SW}) (V_{BST} - V_{SW}) drops below 2.3V, BST refreshes and turns on the low-side MOSFET (LS-FET) to refresh C_{BST} with small duty cycle. The HS-FET can be driven normally again once (V_{BST} - V_{SW}) reaches to 2.5V.

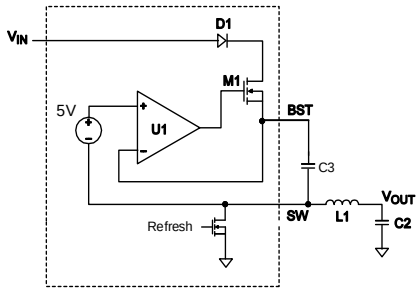


Figure 3: Internal Bootstrap Power Supply

Over-Temperature Protection (OTP)

The MP4562 monitors the junction temperature (T_J) internally to prevent the device from operating at exceedingly high temperatures. If T_J exceeds over-temperature protection (OTP) rising threshold (150°C), then the converter shuts down. Once T_J drops below 130°C, the device initiates an SS and resumes normal operation.

APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT})

The external resistor divider sets V_{OUT}. The FB resistor (R1) sets the FB loop bandwidth using the internal compensation capacitor. Choose an R1 value. Then R2 can be calculated with Equation (5):

$$R2=\frac{R1}{\frac{V_{OUT}}{V_{REF}}-1} \quad (5)$$

Where V_{REF} is the reference voltage (typically 0.8V).

A feed-forward capacitor can improve load transient. Figure 4 shows the FB network.

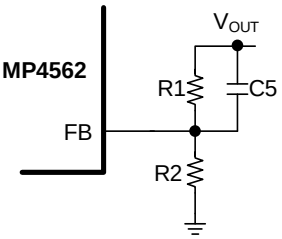


Figure 4: Feedback Network

Table 1 lists the recommended resistor and capacitor values for common output voltages.

Table 1: Resistor and Capacitor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C5 (pF)
3.3	210	68	10	15
5	210	40.2	10	10
12	210	15	22	6.8

Selecting the Inductor

The inductor is required to supply constant current to the output load while being driven by the switched V_{IN}. A larger-value inductor results in less ripple current and a lower ΔV_{OUT}; however, a larger-value inductor has a larger physical footprint, higher series resistance, and lower saturation current. The inductance (L) can be calculated with Equation (6):

$$L=\frac{V_{OUT}}{f_{SW}\times\Delta I_L}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum peak inductor current (I_{L_PEAK}). I_{L_PEAK} can be calculated with Equation (7):

$$I_{L\_PEAK}=I_{OUT}+\frac{V_{OUT}}{2f_{SW}\times L}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients. Placed these capacitors as close to the VIN pin as possible.

The capacitors should have a ripple current rating greater than the converter's maximum input ripple current (I_{CIN}). I_{CIN} can be estimated with Equation (8):

$$I_{CIN}=I_{OUT}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}})} \quad (8)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (9):

$$I_{CIN}=\frac{I_{OUT}}{2} \quad (9)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance (C_{IN}) determines the converter's V_{IN} ripple (ΔV_{IN}). If the system has an ΔV_{IN} requirement, choose an input capacitor that meets the specification.

ΔV_{IN} can be estimated with Equation (10):

$$\Delta V_{IN}=\frac{I_{OUT}}{f_{SW}\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (11):

$$\Delta V_{IN}=\frac{1}{4}\times\frac{I_{OUT}}{f_{SW}\times C_{IN}} \quad (11)$$

Selecting the Output Capacitor (C_{OUT})

The output capacitor (C_{OUT}) is required to maintain the DC V_{OUT}. Ceramic or POSCAP capacitors are recommended for the best performance. ΔV_{OUT} can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (12)$$

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times C_{OUT} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

For POSCAP capacitors the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (14)$$

A larger C_{OUT} can also improve load transient response. Consider the maximum C_{OUT} (C_{OUT_MAX}) during application design. If C_{OUT} is too high, V_{OUT} cannot reach its design value during t_{SS} and fails to regulate. C_{OUT_MAX} can be calculated with Equation (15):

$$C_{OUT\_MAX} = (I_{LIMIT\_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (15)$$

Where, I_{LIMIT_AVG} is the average start-up current limit during SS, and t_{SS} is the soft-start time.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 5 and follow the guidelines below:

1. Place the high current paths (the input capacitor, IC, and diode) close to each other using short, direct, and wide traces.
2. Place a small input capacitor as close to the VIN and GND pins as possible.
3. Place the external feedback resistors next to the FB pin.
4. Route the switching node (SW) away from the FB network using short traces.

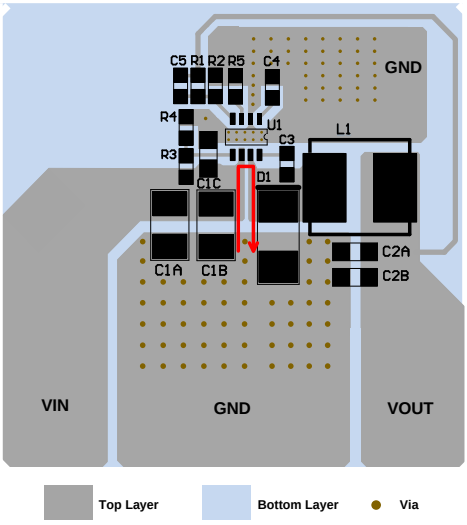


Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

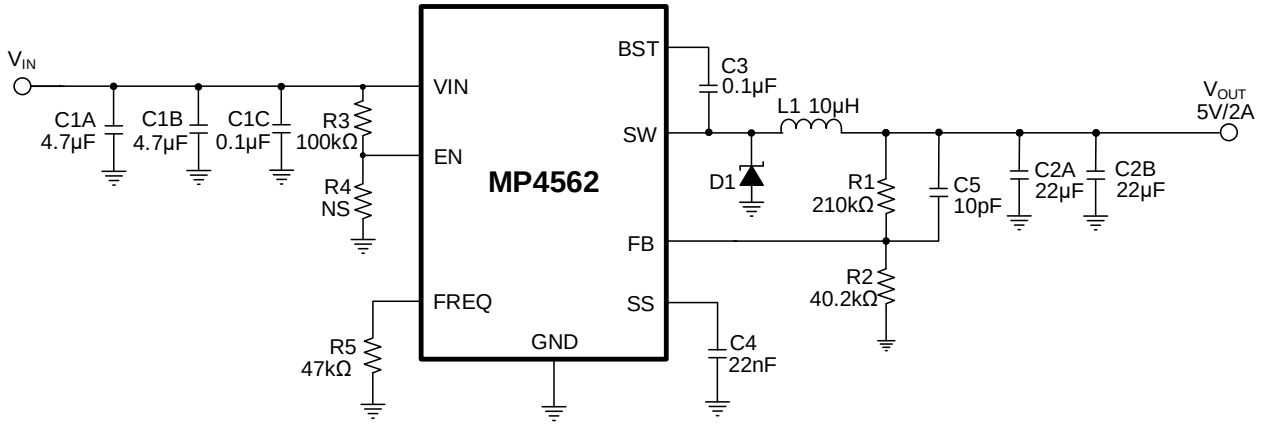
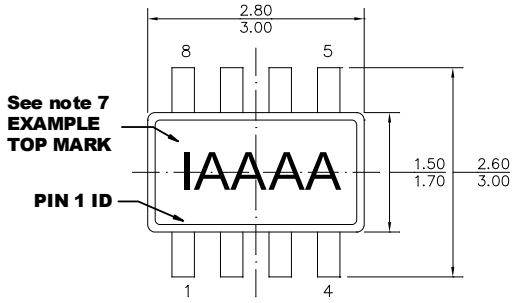


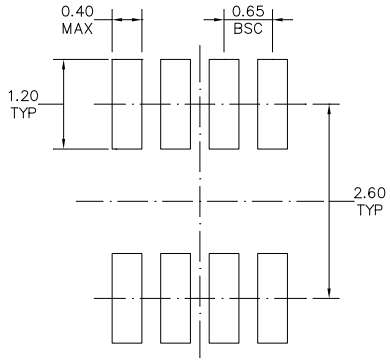
Figure 6: Typical Application Circuit

PACKAGE INFORMATION

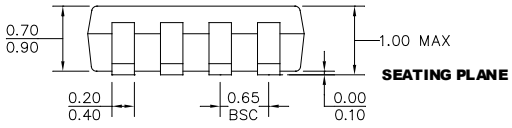
TSOT23-8



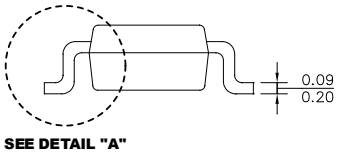
TOP VIEW



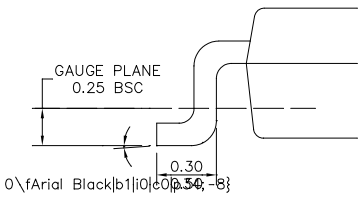
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

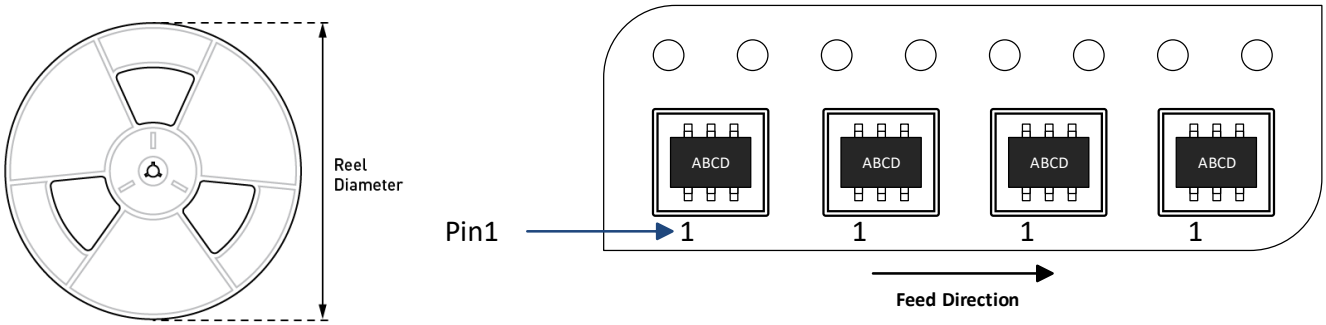


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4562GJ-Z	TSOT23-8	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/3/2023	Initial Release	-