TS82250FK – 20 W GaN Broadband RF Switch SPDT

1.0 Features

- Low insertion loss: 0.2dB @ 800MHz
- High isolation: 45dB @ 800MHz
- High CW power handling capability 20 W
- No external DC blocking capacitors on RF lines
- All RF ports OFF state
- Versatile 2.6-5.25V power supply
- Operating frequency: 30MHz to 5.0GHz

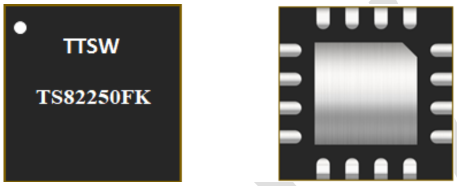

Figure 1 Device Image
(16 Pin 3×3×0.8mm QFN Package)

2.0 Applications

- Private mobile radio handsets
- Public safety handsets
- Cellular infrastructure
- Small cells (3×3mm QFN package)
- LTE relays and microcells
- Satellite terminals

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS82250FK is a symmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high peak power switching applications. Its broadband behavior from 30MHz to 5.0GHz frequencies makes the TS82250FK an excellent switch for all applications requiring low insertion loss, high isolation and high linearity within a small package size. This part has the internal charge pump disabled to eliminate the charge pump spurs. A -17V supply is needed on the VCP pin.

The TS82250FK is packaged into a compact Quad Flat No lead (QFN) 3x3mm 16 leads plastic package.

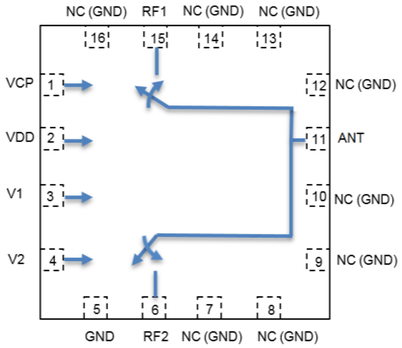

Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1a Ordering Information

Device Part Number	Package Type	Eval Board Part Number
TS82250FK	16 Pin 3×3×0.8mm QFN	TS82250FK-EVB

Table 1b Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3,000	13” (330mm)	18mm

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VCP	Negative Voltage Supply, -17V
2	VDD	DC power supply
3	V1	Switch control input 1
4	V2	Switch control input 2
6	RF2	RF port 2
5,7,8,9,10,12,13,14,16	NC	No internal connection, can be grounded
11	ANT	Antenna port
15	RF1	RF port 1

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	5.25	V
Charge Pump Voltage	VCP	-18	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
Maximum RF input power	RFx/ANT	43	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	25	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	39	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+3.3V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating Frequency		30		5000	MHz
Insertion Loss, RFx	400MHz		0.15		dB
	800MHz		0.18		
	1.95GHz		0.24		
	2.6GHz		0.26		
	5.0GHz		0.5		
Isolation ANT-RFx	400MHz		54		dB
	800MHz		45		
	1.95GHz		35		
	2.6GHz		30		
	5.0GHz		22		
Return Loss ANT-RFx	400MHz		35		dB
	800MHz		32		
	1.95GHz		25		
	2.6GHz		24		
	5.0GHz		16		
Harmonic distortion					
H2	CW, 800MHz, Pin=40dBm		-92		dBc
H3	CW, 800MHz, Pin=40dBm		-95		dBc
IIP3	800MHz		77		dBm
P0.1dB[1]	800MHz, 1% duty cycle, 1mS period		46		dBm
	800MHz, CW	43	45		dBm
Switching Time	50% ctrl to 10/90% of the RF value is settled. C1=1nF (refer to Figure 3)		0.9		μs
Control Voltage	Power supply VDD	2.6	3.3	5.25	V
	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control Current	All control pins low, I_{il}		0		μA
	All control pins high, I_{ih}			7.5	μA
Current Consumption, IDD	Active mode		160	200	μA

Note:

[1] P0.1dB, input 0.1 dB compression point, is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	Active RF Path
0	1	All OFF
0	0	ANT-RF1
1	0	ANT-RF2

Attention:
[1] **VDD should be applied first before VCP**. Minimum time between VDD and VCP should be 50usec.
[2] V1, or V2 can be toggled/switched after VCP has settled.

9.0 Evaluation Board

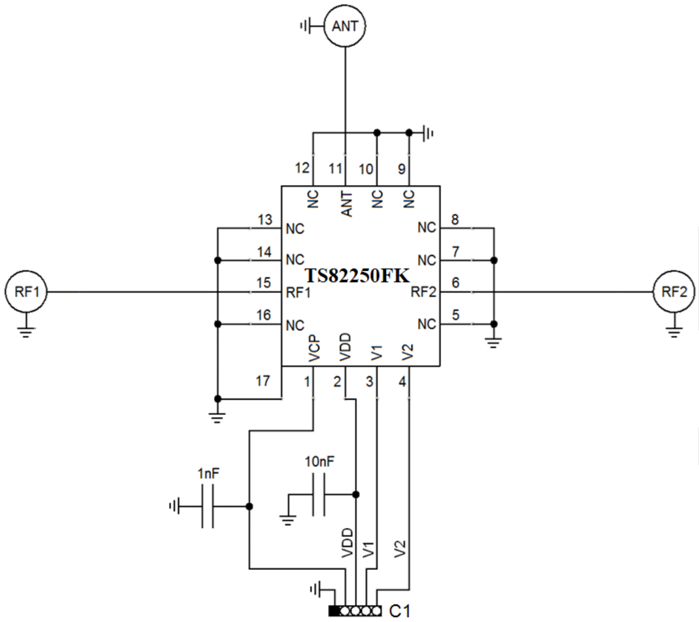

Figure 3 Evaluation Board Schematic

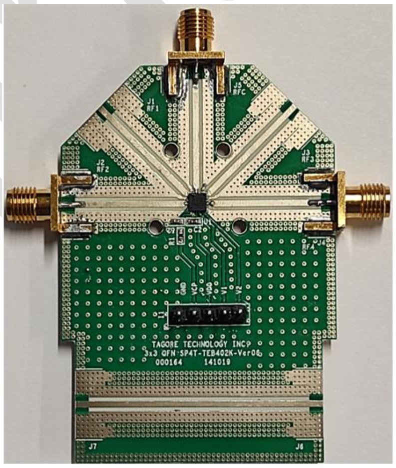

Figure 4 Evaluation Board Image

Attention:
[1] 17 refers to the center pad of the device.
[2] -17V needed on VCP pin.

10.0 Typical Characteristics

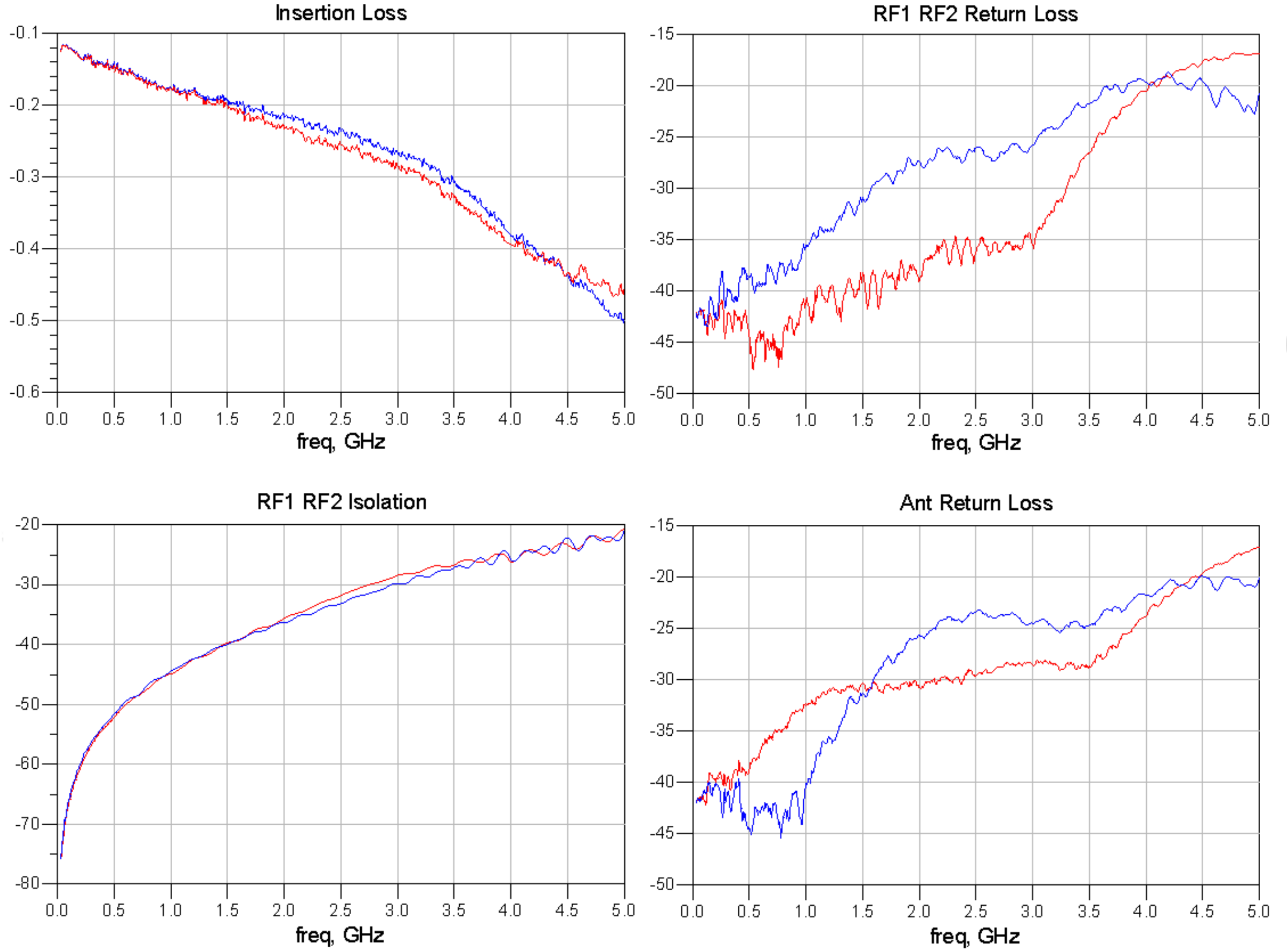

Figure 4 Evaluation Board Typical Characteristics (no match)

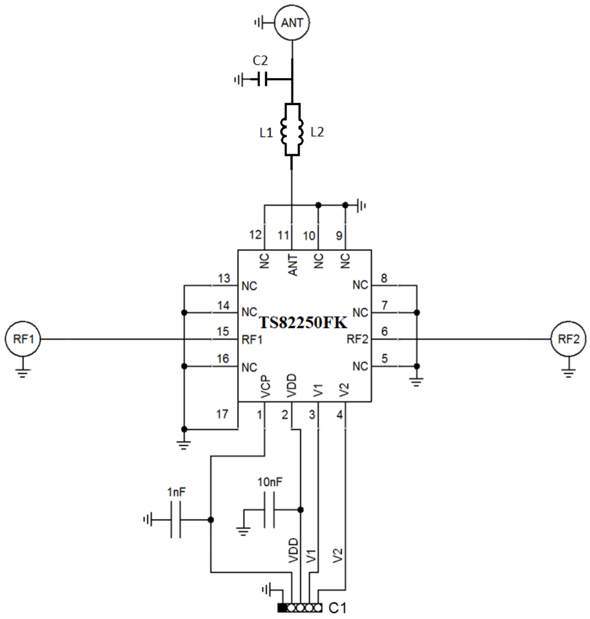

Figure 5 Evaluation Board with matching circuits

C2	0603N0R2BW251	PPI
L1	0402DC-N80XJRU	Coilcraft
L2	0402DC-N80XJRU	Coilcraft

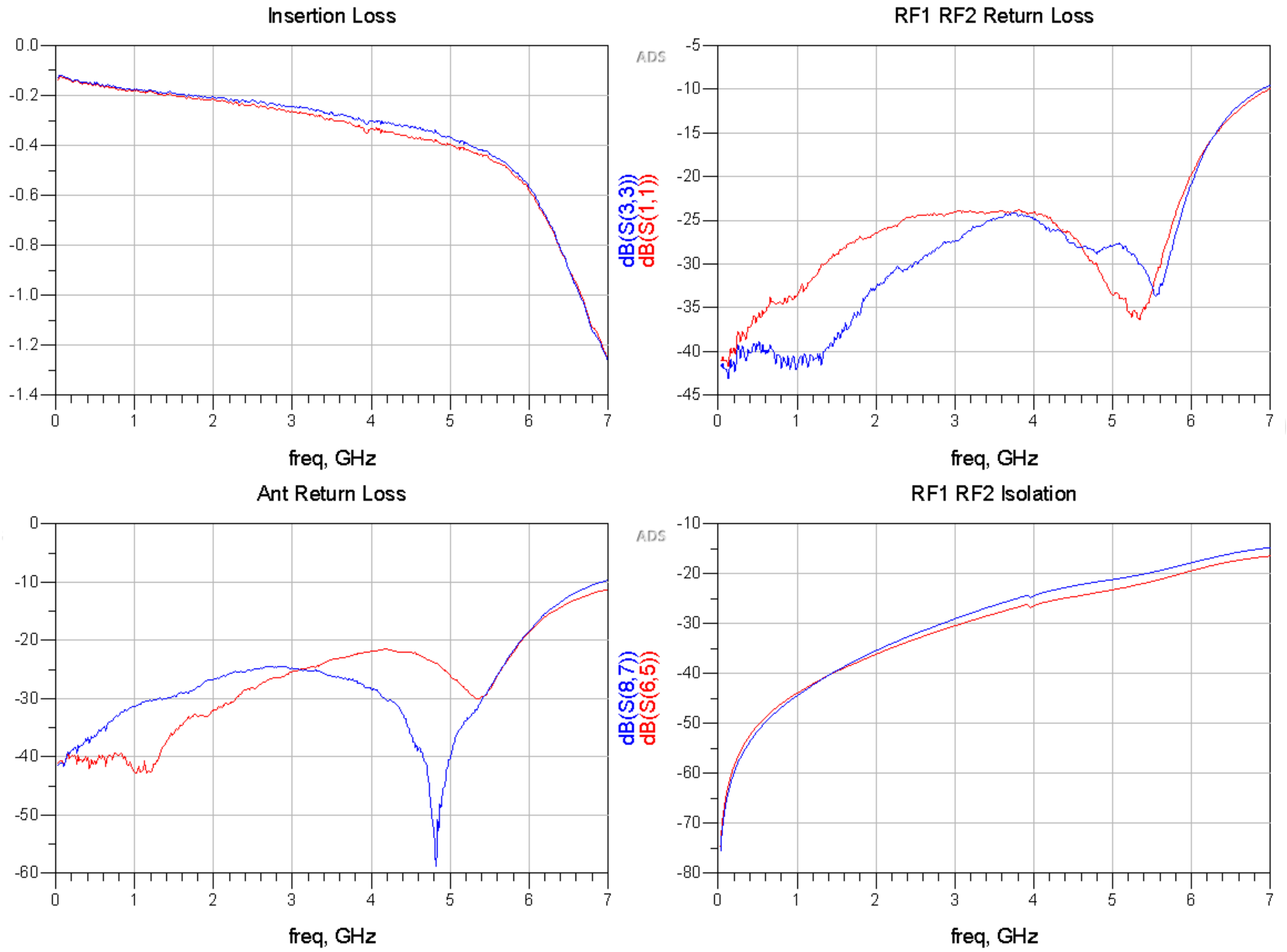

Figure 6 Evaluation Board Typical Characteristics (matched)

11.0 Device Package Information

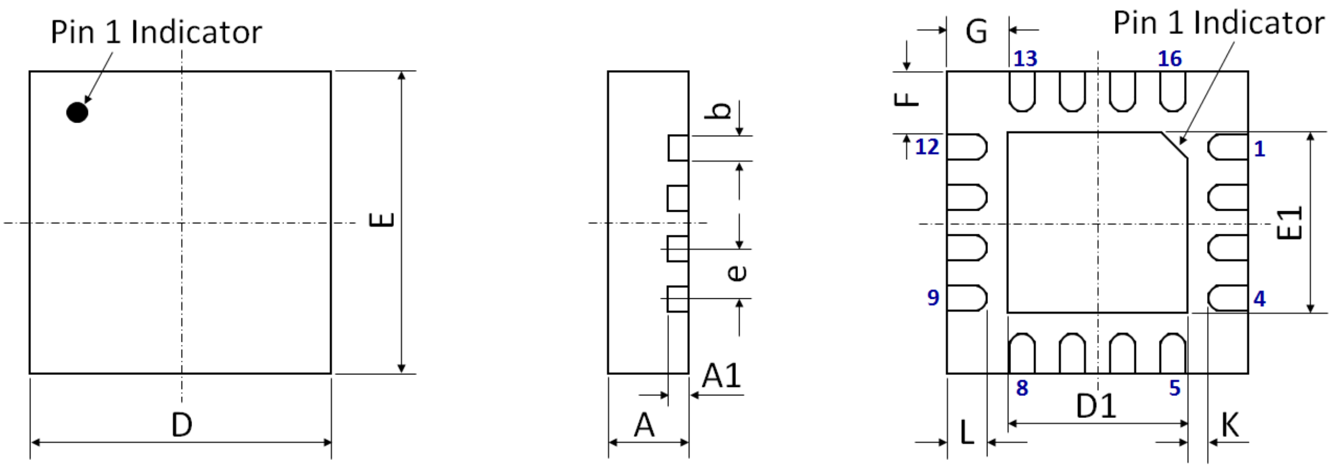

Figure 7 Device Package Drawing

(All dimensions are in mm)

Table 6 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.80	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

12.0 PCB Land Design

Guidelines:

[1] 4 layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 3(X)×3(Y)=9.

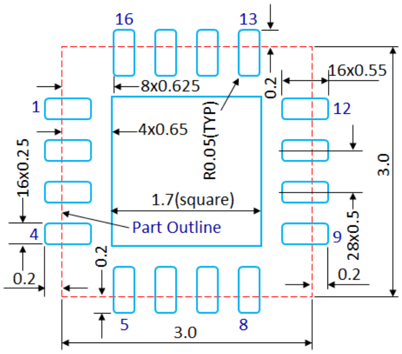

Figure 8 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined
(Preferred)

Solder Mask Defined

Figure 9 Solder Mask Pattern
(Dimensions are in mm)

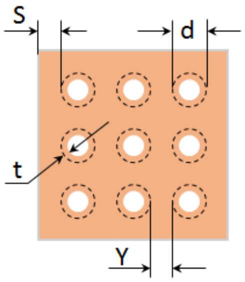

Figure 10 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

13.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125µm.

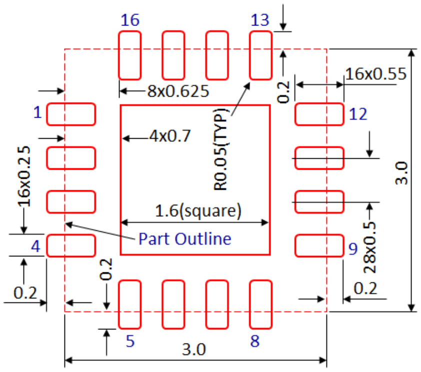

Figure 11 Stencil Openings
(Dimensions are in mm)

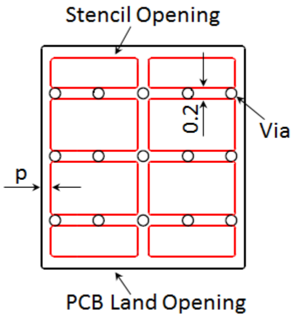

Figure 12 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

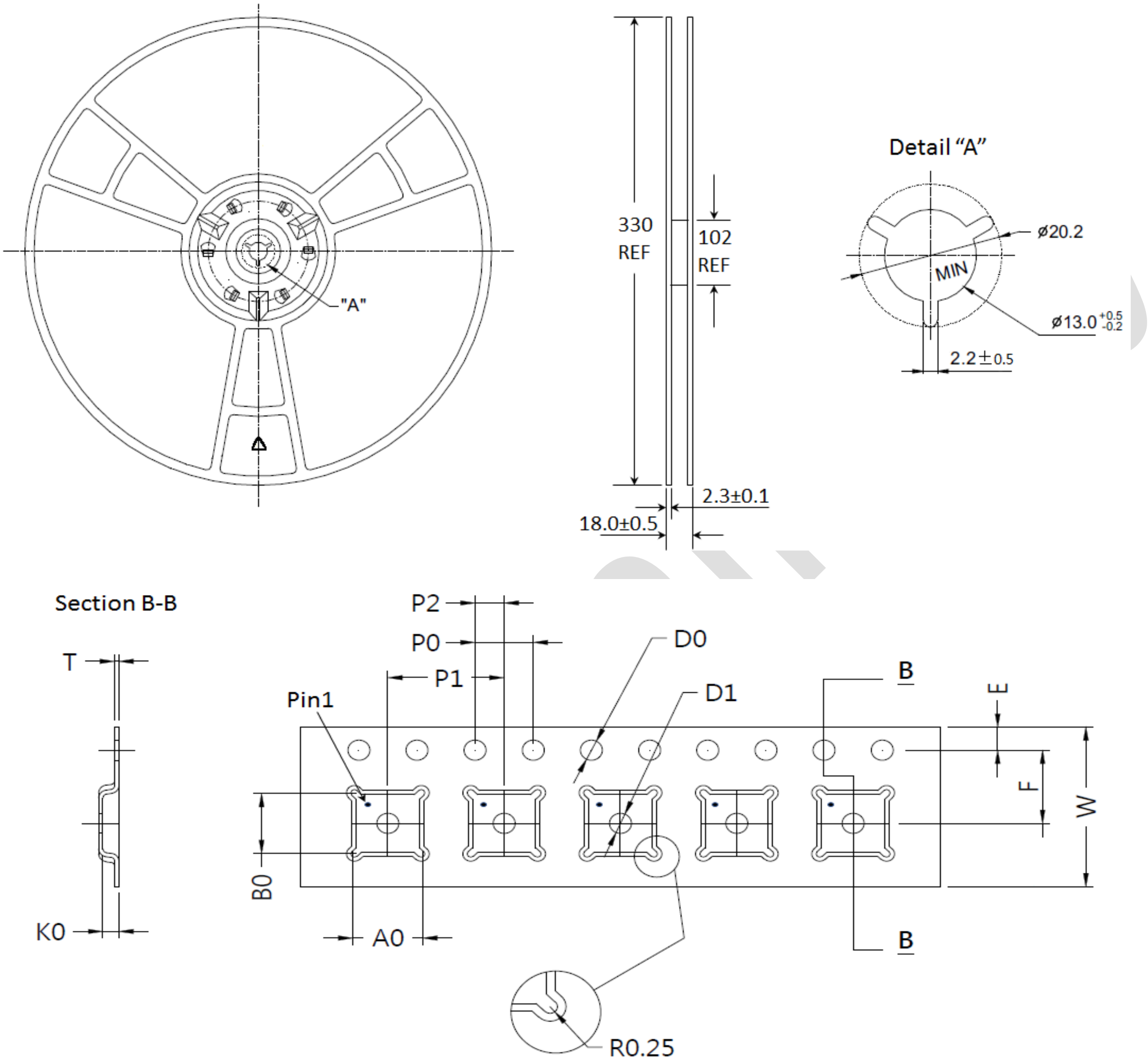

Figure 13 Tape and Reel Drawing

Table 7 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	3.35	±0.10	K0	1.10	±0.10
B0	3.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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