Si512

NFC Front-end chip

1 Introduction

Si512 is a highly integrated NFC front-end for contactless communication at 13.56 MHz.This NFC front-end utilizes an outstanding modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols at 13.56 MHz and supports automatic carrier detection function.

The Si512 NFC front-end supports 5 different operating modes:

- Reader/Writer mode supporting ISO/IEC 14443A and FeliCa scheme
- Reader/Writer mode supporting ISO/IEC 14443B
- Card Operation mode supporting ISO/IEC 14443A and FeliCa scheme
- NFCIP-1 mode
- ACD mode, automatic RF card and RF field detection with extremely low power consumption at 13.56 MHz

The Si512's internal transmitter part is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443A cards and transponders without additional active circuitry. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO/IEC 14443A compatible cards and transponders. The digital part handles the complete ISO/IEC 14443A framing and error detection (Parity and CRC).

The Si512 supports all layers of the ISO/IEC 14443B reader/writer communication scheme, given correct implementation of additional components, like oscillator, power supply, coil etc. and provided that standardized protocols, e.g. like ISO/IEC 14443-4 and/or ISO/IEC 14443B anticollision are correctly implemented.

Enabled in Reader/Writer mode for FeliCa, the Si512 NFC front-end supports the FeliCa communication scheme. The receiver part provides a robust and efficient implementation of the demodulation and decoding circuitry for FeliCa coded signals. The digital part handles the FeliCa framing and error detection like CRC. The Si512 supports contactless communication using FeliCa Higher transfer speeds up to 424 kbit/s in both directions.

In Card Operation mode, the Si512 NFC front-end is able to answer to a reader/writer command either according to the FeliCa or ISO/IEC 14443A card

interface scheme without additional active circuitry. The Si512 generates the digital load modulated signals and in addition with an external circuit the answer can be sent back to the reader/writer.

Si512 NFC front-end offers the possibility to communicate directly to an NFCIP-1 device in the NFCIP-1 mode. The NFCIP-1 mode offers different communication mode and transfer speeds up to 424 kbit/s according to the Ecma 340 and ISO/IEC 18092 NFCIP-1 Standard. The digital part handles the complete NFCIP-1 framing and error detection.

In ACD mode, the chip is mostly in a dormant state and wakes up by 3K RC at a fixed time. It detects a 13.56MHz RF field and RF card with extremely low power consumption, and automatically generates interrupts to wake up the MCU when the field or card is detected. The functions of the detection field and card can be enabled separately. Under a typical 500ms polling cycle, the current is approximately 7.8uA. The entire ACD process does not require MCU intervention.

Various host controller interfaces are implemented:

- SPI interface
- serial UART (similar to RS232 with voltage levels according pad voltage supply)
- I2C interface
- 8-bit parallel interface

Contents

2 Feature and benefits

- Highly integrated analog circuitry to demodulate and decode responses
- Integrated RF Level detector
- Integrated data mode detector
- Supports ISO/IEC 14443 A
- Supports ISO/IEC 14443 B Read/Write modes
- Typical operating distance in Read/Write mode up to 50 mm depending on the antenna size and tuning
- Typical operating distance in NFCIP-1 mode up to 50 mm depending on the antenna size and tuning and power supply
- Typical operating distance in ISO/IEC 14443A card or FeliCa Card Operation mode of about 100 mm depending on the antenna size and tuning and the external field strength
- ISO/IEC 14443A higher transfer speed communication at 212 kbit/s and 424 kbit/s
- Contactless communication according to the FeliCa scheme at 212 kbit/s and 424 kbit/s
- Integrated RF interface for NFCIP-1 up to 424 kbit/s
- S2C interface
- Supported host interfaces
  - SPI up to 10 Mbit/s
  - I2C-bus interface up to 400 kBd in Fast mode, up to 3400 kBd in High-speed mode
  - Serial UART up to 1228.8 kBd
  - 8-bit parallel interface with and without Address Latch Enable
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Support soft power-down
- Integrated programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- 2.5 V to 3.6 V power supply
- CRC coprocessor
- Programmable I/O pins

- Internal self-test
- Low power RF card detection at 13.56MHz
- Low power RF field detection at 13.56MHz
- Support ACD mode
- ACD mode supports for automatic detection of RF and cards
- The ACD process don’t require MCU intervention
- OSC vibration failure monitoring

3 Quick reference data

Voltage、current、temperature in various modes

Table1 Quick reference data

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Analog supply voltage	VDDA	AVDD=PVDD=SVDD=TVDD; VSSA=VSSD=VSS(PVSS)=VSS(TVSS)=0V	(1)	2.3	3.3	4	V
TVDD supply voltage	VDD(TVDD)			2.3	3.3	4	V
PVDD supply voltage	VDD(PVDD)		(1)	2.3	3.3	4	V
SVDD supply voltage	VDD(SVDD)	VSSA=VSSD=VSS(PVSS)=VSS(TVSS)=0V		2.3	3.3	4	V
power-down current	Ipd	AVDD=VDD(SVDD)=VDD(TVDD)=VDD(PVDD)=3.3V					
		hard power-down; pin NRSTPD set LOW	(2)	-	1.1	1.5	uA
		soft power-down; RF level detector on	(2)	-	5.5	6	uA
average current of automatic detect card	IACD1	automatic detect card time interval is 500ms		-	7.8	8.5	uA
average current of automatic detect field	IACD2	automatic detect field time interval is 500ms		-	7.2	8	uA
PVDD supply current	IDDD	Pin PVDD；PVDD=3.3V		-	1.1	1.5	mA
Analog supply current	IDDA	pin AVDD; VDDA = 3 V, CommandReg register's RcvOff bit = 0		-	3	4	mA
		pin AVDD; receiver switched off; VDDA = 3 V, CommandReg register's RcvOff bit = 1		-	0.9	1	mA
TVDD supply current	IDD(TVDD)	continuous wave	(3)	-	20	30	mA
Storage temperature		QFN32		-55	-	+125	℃
Operating temperature		QFN32		-40	-	+85	℃

NOTE: (1) VDDA, VDDD and VDD(TVDD) must always be the same voltage.

(2) Ipd is the total current for all supplies.

(3)During typical circuit operation, the overall current is below 30 mA

NOTE：If the plus condition exceeds the rating of the "limit rated parameter", it will cause permanent damage to the chip.

4 Block diagram

The analog interface handles the modulation and demodulation of the analog signals according to the Card Receiving mode, Reader/Writer mode and NFCIP-1 mode communication scheme.

The RF level detector detects the presence of an external RF-field delivered by the antenna to the RX pin.

The Data mode detector detects a FeliCa or NFCIP-1 mode in order to prepare the internal receiver to demodulate signals.

The communication interface (S^2C) provides digital signals to support communication for transfer speeds above 424 kbit/s and digital signals to communicate to a secure IC.

The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host. The FIFO buffer ensures fast and convenient data transfer to and from the host and the contactless UART and vice versa.

Various host interfaces are implemented to meet different customer requirements.

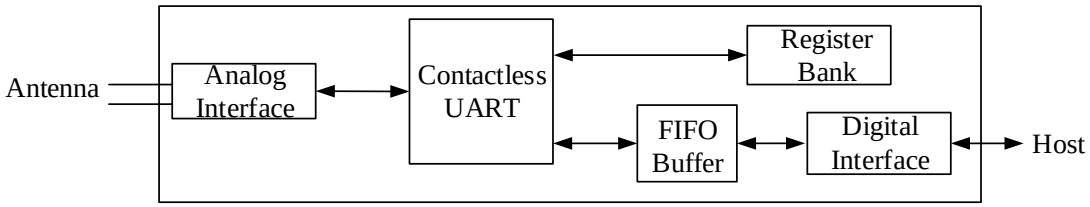


Figure 4.1 Simplified block diagram of the Si512

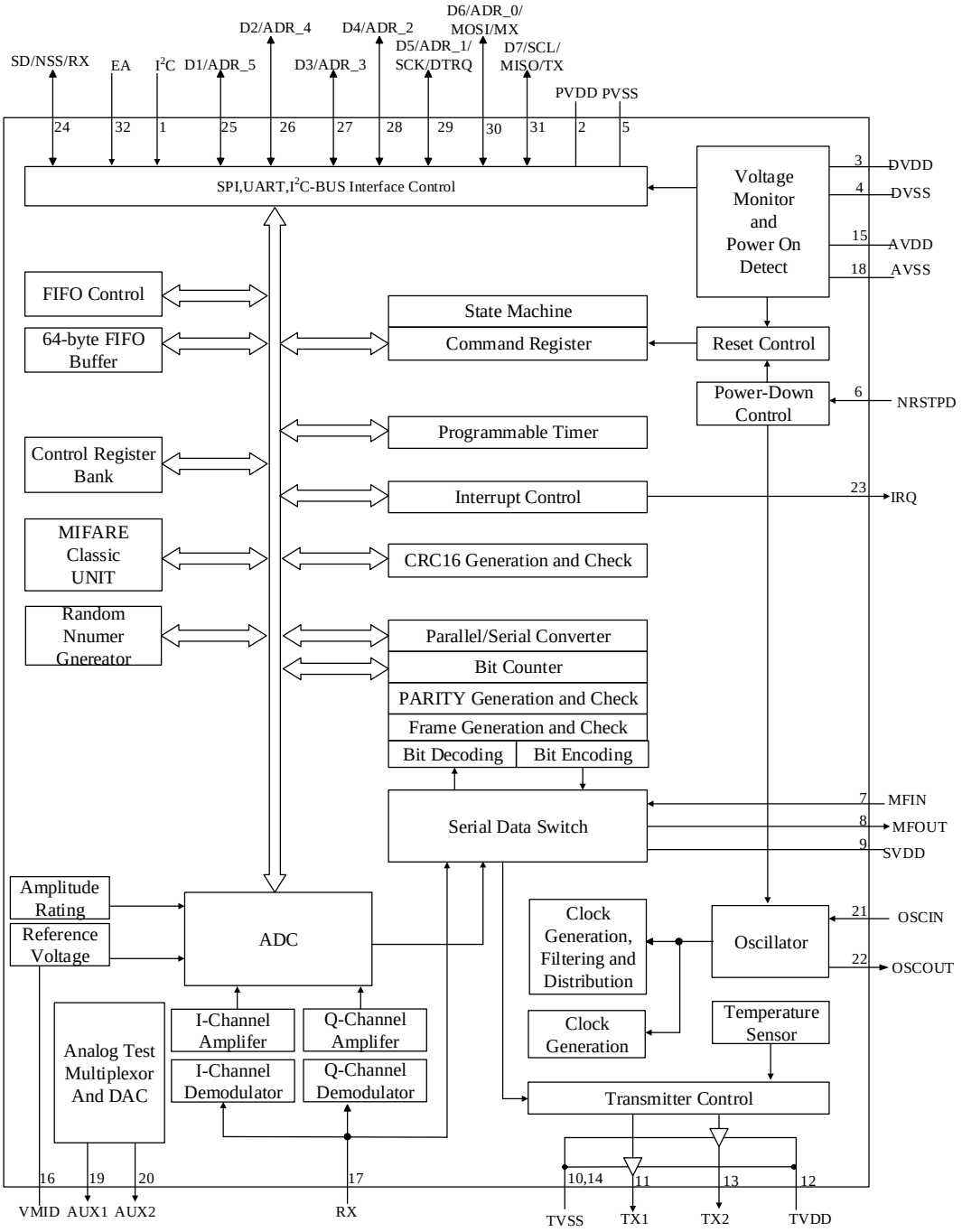


Figure 4.2 Detailed block diagram of the Si512

5 Pinning information

Si512 Pinning ：

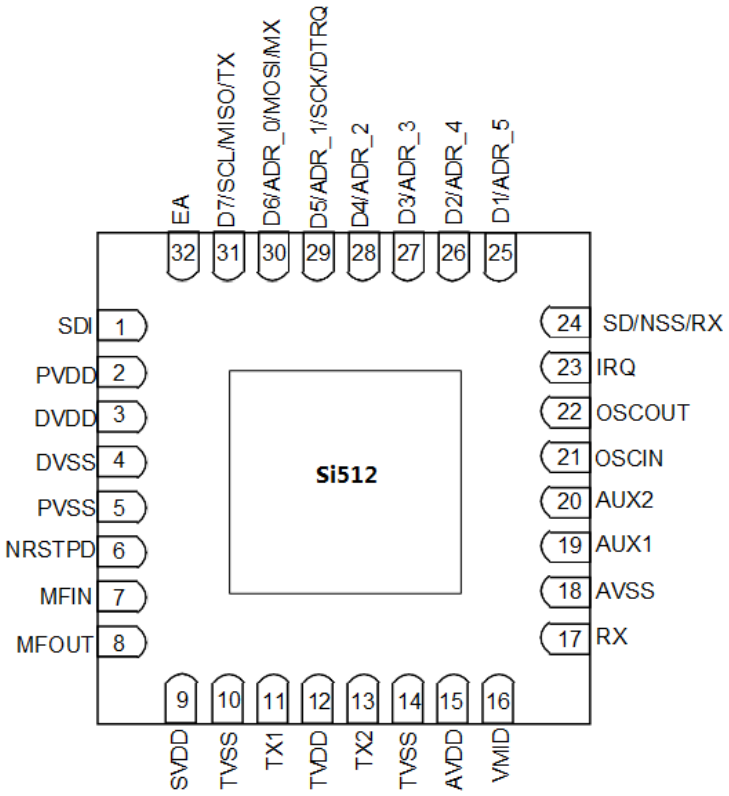


Figure 5.1 Pinning configuration

Table5-1 Pinning configuration

Pin	Symbol	Type[1]	Description
1	SDI	I	I2C bus input[2]
2	PVDD	P	Pad power supply
3	DVDD	P	Digital Power Supply
4	DVSS	P	Digital Ground
5	PVSS	P	Pad power supply ground
6	NRSTPD	I	Not Reset and Power Down: Power Down: When LOW, internal current sinks are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. Reset:With a positive edge on this pin the internal reset phase starts.
7	MFIN	I	Communication Interface Input: accepts a digital, serial data stream

8	MFOUT	O	Communication Interface Output: delivers a serial data stream
9	SVDD	P	Provides power to the MFIN/MFOUT
10	TVSS	P	Transmitter Ground: supplies the output stage of TX1 and TX2
11	TX1	O	Transmitter 1: delivers the modulated 13.56 MHz energy carrier
12	TVDD	P	Transmitter Power Supply: supplies the output stage of TX1 and TX2
13	TX2	O	Transmitter 2: delivers the modulated 13.56 MHz energy carrier
14	TVSS	P	Transmitter Ground: supplies the output stage of TX1 and TX2
15	AVDD	P	Analog Power Supply
16	VMID	P	Internal Reference Voltage: This pin delivers the internal reference voltage.
17	RX	I	Receiver Input
18	AVSS	P	Analog Ground
19	AUX1	O	Auxiliary Outputs: These pins are used for testing.
20	AUX2	O	
21	OSCIN	I	Crystal Oscillator Input: input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (fosc = 27.12 MHz).
22	OSCOUT	O	Crystal Oscillator Output: Output of the inverting amplifier of the oscillator.
23	IRQ	O	Interrupt Request: output to signal an interrupt event
24	SD	I/O	I2C bus serial data input and output[2]
	NSS	I	SPI input[2]
	RX	I	UART Address input[2]
25	D1	I/O	Test port[2]
	ADR_5	I/O	I2C bus address5 input[2]
26	D2	I/O	Test port
	ADR_4	I	I2C bus address4 input[2]
27	D3	I/O	Test port
	ADR_3	I	I2C bus address3 input[2]
28	D4	I/O	Test port
	ADR_2	I	I2C bus address2 input[2]
29	D5	I/O	Test port
	ADR_1	I	I2C bus address1 input[2]
	SCK	I	SPI seria clock input l[2]

	DTRQ	O	UART makes a request to controller[2]
30	D6	I/O	Test port
	ADR_0	I	I2C bus address0 input[2]
	MOSI	I/O	SPI Master Out Slave In[2]
	MX	O	UART for the output of the controller[2]
31	D7	I/O	Test port
	SCL	I/O	I2C bus clock input/output[2]
	MISO	I/O	SPI Master In Slave Out [2]
	TX	O	UART Data output to controller[2]
32	EA	I	External address input：can be used to define the I2C address

NOTE: [1] Pin type:I=Input, O=Output, P=Power

[2] The functions of these pins are also shown in chapter 8 digital interfaces

6 Functional description

The Si512 transmission module supports the Read/Write mode for ISO/IEC 14443 A and ISO/IEC 14443B using various transfer speeds and modulation protocols.

Si512 NFC frontend supports the following operating modes:

- Reader/Writer mode supporting ISO/IEC 14443A and FeliCa scheme
- Card Operation mode supporting ISO/IEC 14443A and FeliCa scheme
- NFCIP-1 mode
- ACD mode

The modes support different transfer speeds and modulation schemes.

NOTE: All indicated modulation indices and modes in this chapter are system parameters.

This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.

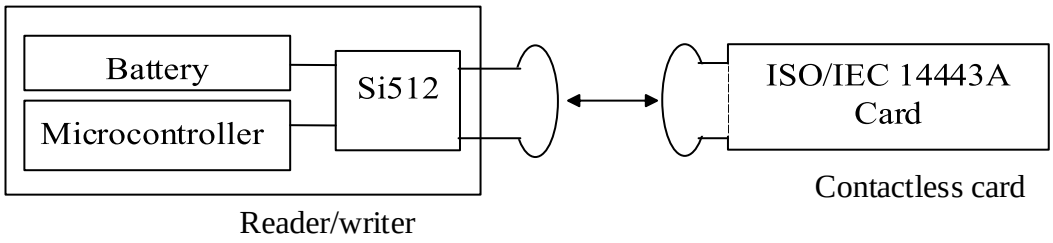


Figure 6.1 Si512 Read/Write mode

6.1 ISO/IEC 14443 A functionality

The physical level communication is shown below.

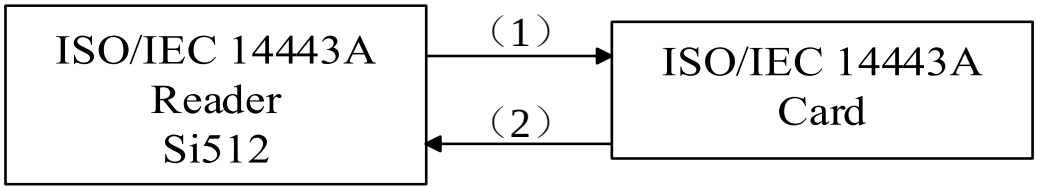


Figure 6.2 ISO/IEC 14443ARead/Write mode communication diagram

The physical parameters are described in Table 6-1.

Table 6-1 Communication overview for ISO/IEC 14443 A reader/writer

Communication direction	Signal type	Transfer speed		
		106kBd	212kBd	424kBd
Reader to card (send data from the Si512 to a card)	Reader side modulation	100%ASK	100%ASK	100%ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit length	(128/13.56)μs	(64/13.56)μs	(32/13.56)μs
Card to reader (Si512 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56MHz/16	13.56MHz/16	13.56MHz/16
	bit encoding	Manchester	BPSK	BPSK

The Si512's contactless UART and dedicated external host must manage the complete ISO/IEC 14443 A protocol. The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally according to the transfer speed.

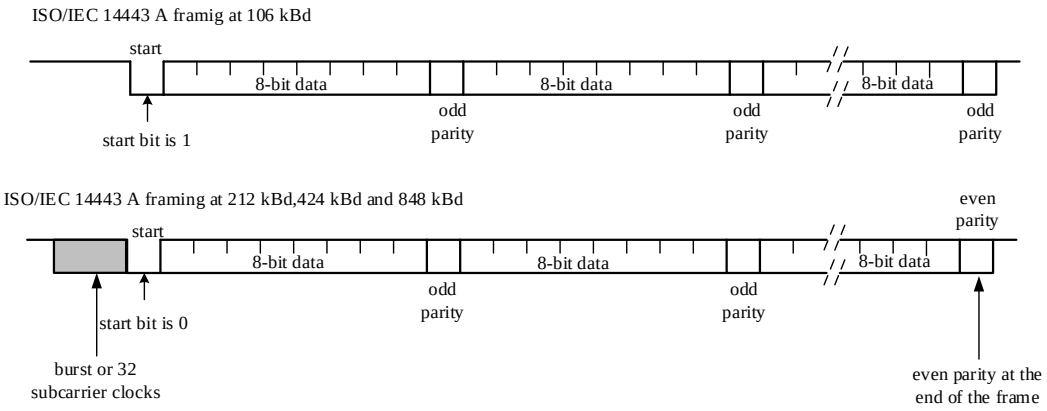


Figure 6.3 Data coding and framing according to ISO/IEC 14443 A

6.2 ISO/IEC 14443 B functionality

Si512 supports the reading and writing of ISO/IEC 14443 B card, and the relevant physical layer parameters are shown in the table below.

Table 6-2 Communication overview for ISO 14443B reader/writer

Communication direction	Signal type	Transfer speed		
		106kBd	212kBd	424kBd
Reader to card (send data from the Si512 to a card)	Reader side modulation	10%ASK	100%ASK	10%ASK
	bit encoding	NRZ-L	NRZ-L	NRZ-L
	bit length	(128/13.56)μs	(64/13.56)μs	(32/13.56)μs
Card to reader (Si512 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56MHz/16	13.56MHz/16	13.56MHz/16
	bit encoding	BPSK	BPSK	BPSK

6.3 FeliCa reader/writer functionality

The following diagram describes the communication on a physical level for FeliCa.

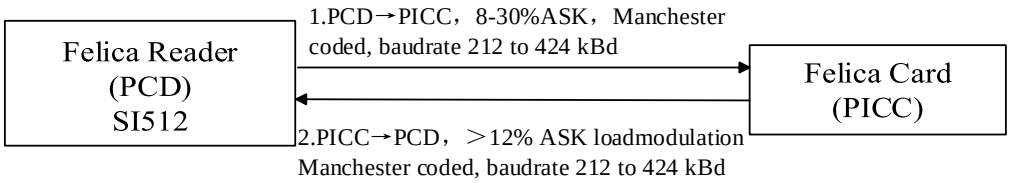


Figure 6.4 FeliCa reader/writer communication diagram

Table 6-3 Communication overview for FeliCa reader/writer

Communication direction	Signal type	Transfer speed	
		212kBd	424kBd
Reader to card (send data from the Si512 to a card)	Reader side modulation	8-30%ASK	8-30%ASK
	bit encoding	Manchester	Manchester
	bit length	(64/13.56)μs	(32/13.56)μs
Card to reader (Si512 receives data from a card)	card side modulation	>12%ASK	>12%ASK
	bit encoding	Manchester	Manchester

The contactless UART of Si512 and a dedicated external host controller are required to handle the complete FeliCa protocol.

6.3.1 FeliCa framing and coding

Table 6-4 Felicaframing and coding

Preamble						Sync		Len	Data	CRC	
00h	00h	00h	00h	00h	00h	B2h	4Dh		N bytes		

To enable the FeliCa communication a 6 byte preamble (00h, 00h, 00h, 00h, 00h, 00h) and 2 bytes Sync bytes (B2h, 4Dh) are sent to synchronize the receiver. The following Len byte indicates the length of the sent data bytes plus the LEN byte itself.

The CRC calculation is done according to the FeliCa definitions with the MSB first.

To transmit data on the RF interface, the host controller has to send the Len- and databytes to the Si512's FIFO-buffer. The preamble and the sync bytes are generated by the Si512 automatically and must not be written to the FIFO by the host controller. The Si512 performs internally the CRC calculation and adds the result to the data frame.

6.4 NFCIP-1 mode

The NFCIP-1 communication differentiates between an active and a Passive Communication mode.

- Active Communication mode means both the initiator and the target are using their own RF field to transmit data.
- Passive Communication mode means that the initiator generates RF field at 13.56 MHz, and the target answers to an initiator command in a load modulation scheme.

In order to fully support the NFCIP-1 standard the Si512 supports the Active and Passive Communication mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s.

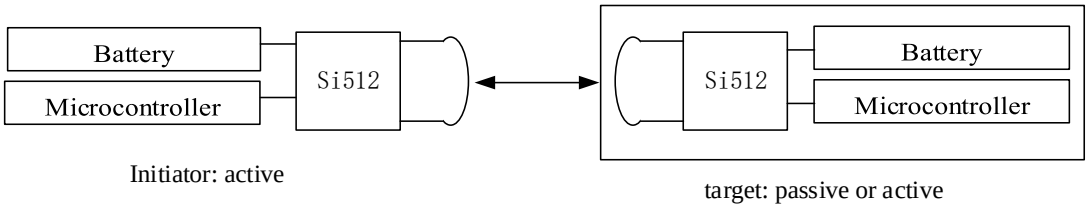


Figure 6.5 NFCIP-1mode

6.4.1 Active communication mode

Active communication mode means both the initiator and the target are using their own RF field to transmit data. The following diagram describes the communication on a physical level.

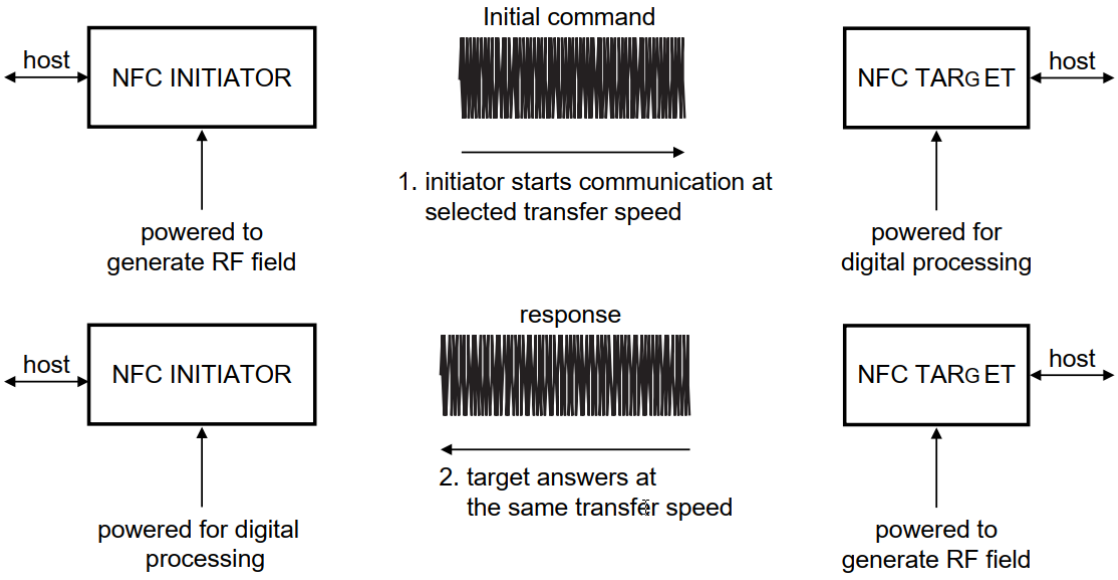


Figure 6.7 Active communication mode

Table 6-5 Communication overview for Active communication mode

Communication direction	106kbits/s	212kbits/s	424kbits/s	848kbits/s	1.69Mbits/s, 3.39Mbits/s
Initiato→ Targe	According to ISO/IEC 14443A, 100 % ASK, Modified Miller Coded	According to FeliCa, 8-30 % ASK Manchester Coded		digital capability to handle this communication	
Targ→ Initiator					

The contactless UART of Si512 and a dedicated host controller are required to handle the NFCIP-1 protocol. Transfer Speeds above 424 kbit/s are not defined in the NFCIP-1 standard. The Si512 supports these transfer speeds only with dedicated external circuits.

6.4.2 Passive communication mode

Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The following diagram describes the communication on a physical level.

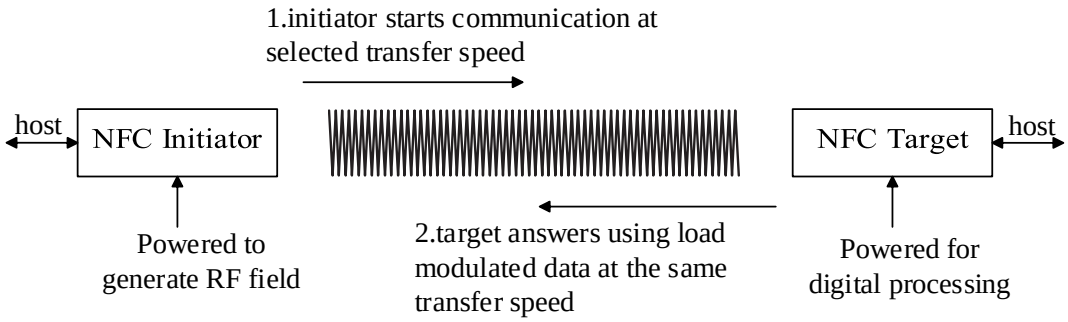


Figure 6.8 Passive communication mode

Table6-6 Communication overview for Passive communication mode：

Communication direction	106kbits/s	212kbits/s	424kbits/s	848kbits/s	1.69Mbits/s, 3.39Mbits/s
Initiator→ Target	According to ISO/IEC 14443A 100 % ASK, Modified Miller Coded	According to FeliCa, 8-30% ASK Manchester Coded		Digital capability to handle this communication	
Target→ Initiator	According to ISO/IEC 14443A Subcarrier load modulation, Manchester Coded	According to FeliCa, > 12% ASK Manchester Coded			

The contactless UART of Si512 and a dedicated host controller are required to handle the NFCIP-1 protocol. Transfer Speeds above 424 kbit/s are not defined in the NFCIP-1 standard. The Si512 supports these transfer speeds only with dedicated external circuits.

6.4.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive Communication mode is defined in the NFCIP-1 standard.

Table 6-7 Framing and coding overview

Transfer speed	Framing and Coding
106kbits/s	According to the ISO/IEC 14443A scheme
212kbits/s	According to the FeliCa scheme
424kbits/s	According to the FeliCa scheme

For detailed explanation of the protocol refer to the NFCIP-1 standard. However the datalink layer is according to the following policy:

- Speed shall not be changed while continuum data exchange in a transaction.
- Transaction includes initialization and anticollision methods and data exchange (in continuous way, meaning no interruption by another transaction).

6.4.4 NFCIP-1 protocol support

NFCIP-1 communication are defined in the following way.

- Per default NFCIP-1 device is in Target mode meaning its RF field is switched off. When specific application needs, the initiator pattern can be opened.
- The RF level detector is active.
- Initiator shall only switch on its RF field if no external RF field is detected by RF Level detector during a time of TIDT.
- The initiator performs initialization according to the selected mode.

6.4.5 FeliCa Card operation mode

Table 6-9 FeliCa Card operation mode

Communication direction	Signal type	Transfer speed	
		212kBd	424kBd
reader/writer→ Si512	Modulation on reader side	8-30%ASK	8-30%ASK
	Bit coding	Manchester	Manchester
	Bit length	(64/13.56)μs	(32/13.56)μs
Si512→ reader/writer	Load modulation on Si512 side	>12%ASK	>12%ASK
	Bit coding	Manchester	Manchester

6.5 Auto Low Power Polling Loop

Auto Low Power Polling Loop consists of 3 parts ——listen、polling and sleep, where listen and sleep can be enabled separately and can achieve extremely low power consumption automatic field and card inspection.Under a 500ms polling cycle,its

average current is only 7.8uA.

The schematic diagram is as follows：

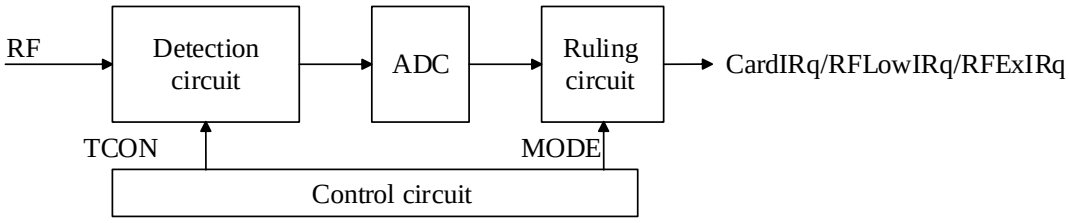


Figure 6.9 ACD function diagram

The implementation principle of polling and listening functions can be found in the description of the detection circuit.T_CON during the polling and listening stages can be configured separately.

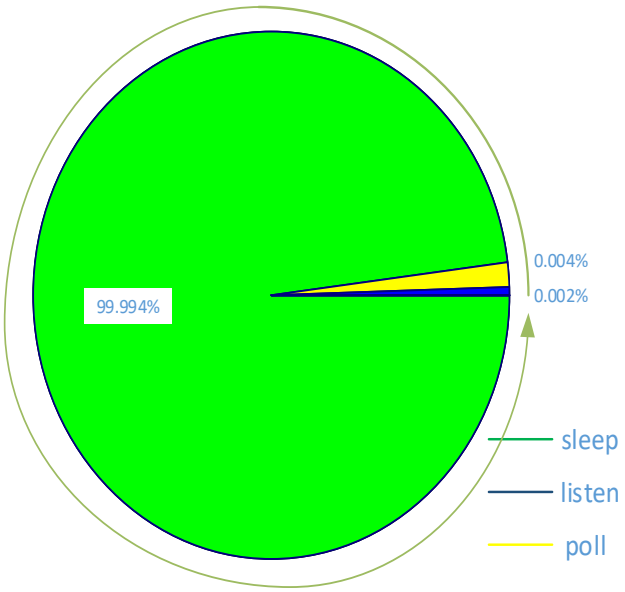


Figure 6.1 Schematic diagram of the polling process

According to user settings, 2~5 listening polls after entering polling mode can be ignored.

1) Listening stage

Si512 is searching for readers at this stage. Si512 does not transmit carriers and detects if there are 13.56MHz carriers transmitted by other external readers. If its amplitude is greater than RFExTreshold, stop executing Loop and generate an interrupt.

2) Polling stage

Si512 is searching for RF cards at this stage. Si512 first transmits the carrier and

then detects the amplitude change of the 13.56MHz carrier. If the amplitude change of the carrier exceeds the set threshold, it is determined as stuck and an interrupt is generated.

(1) Card checking mode: can be set to automatic mode and absolute value mode

- Automatic mode - Compare the carrier amplitude detected this time with the carrier amplitude detected last time, and if the difference exceeds the set threshold, it will be determined that there is a card.
- Absolute value mode - Compare the detected carrier amplitude with the set value, and if the difference exceeds the set threshold, it is determined that there is a card.

(2) Card checking direction: The card checking direction can be set to three modes as needed:

- rising edge: carrier amplitude with card is greater than that without card
- Falling edge: carrier amplitude with card is smaller than that without card
- double edge: carrier amplitude with card is greater or smaller than that without card
- field abnomal judgment

(3) Sleep stage: The chip is in a sleep state.

Related registers：0x01，0x0F_A/B/C/D/E/F/G/I/J/K/L/M/N/O/P

6.5.1 RF reference value automatic acquisition method

Automatically obtain through commands：

- By writing ADC_ EXCUTE command with a command code of 0110b
- waiting for more than 100us
- Writing ADC_ EXCUTE again, read 0X0F_ G is the required reference value

6.5.2 Detection circuit

The principle of the detection circuit is as follows:

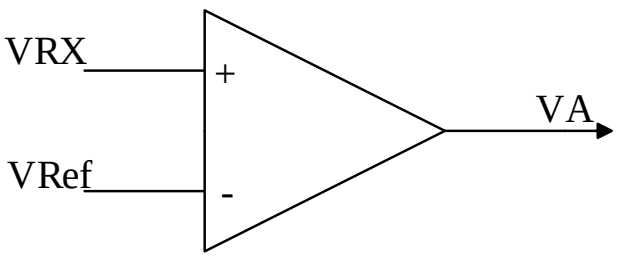


Figure 6.11 Detection circuit diagram

VRX:antenna field strength,VRef：ADC reference voltage，controlled by T_ CON；VA:The voltage sent by the detection module to the ADC

6.5.3 Oscillator monitoring

During the polling process, when the crystal oscillator fails to start up for 4 consecutive times, a crystal oscillator failure interrupt is generated. After an interrupt occurs, the chip does not wake up, but continues to execute Pog Loop. Once the OSC vibrates, the internal counter will reset.

The relevant registers：0x0F_F/0x0F_O/0x0F_P.

6.5.4 3K RC

(1) Timed wake-up is driven by 3K RC, which only operates in Polling Loop.

(2) Clock calibration - divided into Automatic calibration and Manual calibration:

- Automatic calibration: Automatically correct by writing the MStart command with the command code 0101b；
- Manual calibration: Perform manual calibration by configuring registers.

Related register：0x0F_A/0x0F_E/0x0F_F.

6.5.5 ARI

This function is used to indicate whether the RF field is turned on during card search. ARI opens 1 us earlier than the RF field and closes 1 us later than the RF field. ARI and D1 pin reuse.

Related register：0x0F_L/0x0F_J.

6.5.6 ACD Configuration Monitoring

Before entering polling mode, set ACCEn to 1 to enable configuration of monitoring Description. Once the data is lost, ACCErr will be generated and transmitted through IRQ. Before updating the polling configuration, ACCEn must be set low. Set ACCEn low, ACCErr will be automatically cleared.

7 Register SET

7.1 registers overview

Table 7-1 registers overview

Address(HEX)	Register Name	Function
PAGE0：Command and Status		
0	PageReg	Selects the register page and Polling configuration access
1	CommandReg	Starts and stops command execution
2	ComlEnReg	Controls bits to enable and disable the passing of Interrupt Requests
3	DivlEnReg	Controls bits to enable and disable the passing of Interrupt Requests
4	ComIrqReg	Contains Interrupt Request bits
5	DivIrqReg	Contains Interrupt Request bits
6	ErrorReg	Error bits showing the error status of the last command executed
7	Status1Reg	Contains status bits for communication
8	Status2Reg	Contains status bits of the receiver and transmitter
9	FIFODataReg	In and output of 64 byte FIFO-buffer
A	FIFOLevelReg	Indicates the number of bytes stored in the FIFO
B	WaterLevelReg	Defines the level for FIFO under- and overflow warning
C	ControlReg	Contains miscellaneous Control Registers
D	BitFramingReg	Adjustments for bit oriented frames
E	CollReg	Bit position of the first bit collision detected on the RF-interface
F_A	RCCfg1	3K RC configuration1
F_B	ACRDCfg	RF card and RF field detection
F_C	ManRefVal	Manual mode reference value
F_D	ValDelta	Field strength variation range
F_E	ADCCfg	Polling ADC configuration
F_F	RCCfg2	3K RC configuration2
F_G	ADCVal	Polling ADC sanmple value
F_H	WdtCnt	Watchdog interval setting
F_I	ARI	ACRD
F_J	ACC	ACRD configuration verification
F_K	LPDCfg1	Detector configuration1

F_L	LPDCfg2	Detector configuration2
F_M	RFLowDetect	Low RF detection configuration during ACD
F_N	ExRFDetect	External RF detection configuration during ACD
F_O	ACRDIRqEn	ACD interrupt enable
F_P	ACRDIRq	ACD interrupt
PAGE1：Command		
0	PageReg	Selects the register page and Polling configuration access
1	ModeReg	Defines general modes for transmitting and receiving
2	TxModeReg	Defines the data rate and framing during transmission
3	RxModeReg	Defines the data rate and framing during receiving
4	TxControlReg	Controls the logical behavior of the antenna driver pins TX1 and TX2
5	TxAutoReg	Controls the setting of the antenna drivers
6	TxSelReg	Selects the internal sources for the antenna driver
7	RxSelReg	Selects internal receiver settings
8	RxThresholdReg	Selects thresholds for the bit decoder
9	DemodReg	Defines demodulator settings
A	FelNFC1Reg	Defines the length of the valid range for the receive package
B	FelNFC2Reg	Defines the length of the valid range for the receive package
C	MifNFCReg	Controls the communication in ISO/IEC 14443 and NFC target mode at 106 kbit
D	ManualRCVReg	Allows manual fine tuning of the internal receiver
E	TypeBReg	Configure the ISO/IEC 14443 type B
F	SerialSpeedReg	Selects the speed of the serial UART interface
PAGE2：Configuration		
0	PageReg	Selects the register page
1	CRCResultReg	Shows the actual MSB and LSB values of the CRC calculation
2		
3	GsNOffReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation, when the driver is switched off
4	ModWidthReg	Controls the setting of the ModWidth
5	TxBitPhaseReg	Adjust the TX bit phase at 106 kbit
6	RFCfgReg	Configures the receiver gain and RF level
7	GsNOnReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation when the drivers are switched on

8	CWGsPReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation during times of no modulation
9	ModGsPReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation during modulation
A	TModeReg	Defines settings for the internal timer
B	TPrescalerReg	
C	TReloadReg	Describes the 16-bit timer reload value
D		
E	TCounterValReg	Shows the 16-bit actual timer value
F		
PAGE3：TestRegister		
0	PageReg	Selects the register page
1	TestSel1Reg	General test signal configuration
2	TestSel2Reg	General test signal configuration and PRBS control
3	TestPinEnReg	Enables pin output driver on 8-bit parallel bus (NOTE: For serial interfaces only)
4	TestPinValueReg	Defines the values for the 8-bit parallel bus when it is used as I/O bus
5	TestBusReg	Shows the status of the internal testbus
6	AutoTestReg	Controls the digital selftest
7	VersionReg	Shows the version
8	AnalogTestReg	Controls the pins AUX1 and AUX2
9	TestDAC1Reg	Defines the test value for the TestDAC1
A	TestDAC2Reg	Defines the test value for the TestDAC2
B	TestADCReg	Shows the actual value of ADC I and Q
C-E	RFT	Reserved for production tests
F	PollLPReg	Manual configuration reduces ACD mode power consumption

Depending on the functionality of a register, the access conditions to the register can vary. In principle bits with same behavior are grouped in common registers. In Table 7-2 the access conditions are described.

Table 7-2 Behavior of register bits and its designation

Abbreviation	Behavior	Description
r/w	read and write	These bits can be written and read by the µ-Controller. Since they are used only for control means, there content is not influenced by internal state machines,

		e.g. the ComIrqReg may be written and read by the µ-Controller. It will also be read by internal state machines, but never changed by them.
dy	dynamic	These bits can be written and read by the µ-Controller. Nevertheless, they may also be written automatically by internal state machines,e.g. the Command-Register changes its value automatically after the execution of the actual command.
r	Read only	These registers hold bits, which value is determined by internal states only, e.g. the CRCReady bit can not be written from external but shows internal states.
w	Write only	Reading these registers returns always ZERO.
RFU	-	These registers are reserved for future use and shall not be changed.
RFT	-	These registers are reserved for production tests and shall not be changed.

7.2 PAGE0：Command and status

7.2.1 PageReg

Table7-2 PageReg Address：00h reset value：00h

	7	6	5	4	3	2	1	0
	UsePageSelect	Regbank Select	RegSelect				PageSelect	
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-3 Description of PageReg bits

Bit	Symbol	Description
7	UsePageSelect	Set to logic 1, the value of PageSelect is used as register address A5 and A4. The LSB-bits of the register address are defined by the address pins or the internal address latch, respectively. Set to logic 0, the whole content of the internal address latch defines the register address. The address pins are used as described in SectionAutomatic microcontroller interface detection.
6	RegbankSelect	When set to 1，it is used to read/write 0Fh register
5-2	RegSelect	0000：read/write register set A； 0001：read/write register set B； … 1111：read/write register set P
1-0	PageSelect	The value of PageSelect is used only if UsePageSelect is set to logic 1. In this case it specifies the register page (which is A5 and A4 of the register address).

7.2.2 CommandReg

Starts and stops command execution.

Table7-4 CommandReg address:01h reset value:20h

	7	6	5	4	3	2	1	0
	AutoPoll	0	RcvOff	Power Down	Command			
Access	dy	RFU	r/w	dy	dy	dy	dy	dy

Table7-5 Description of CommandReg bits

Bit	Symbol	Description
7	AutoPoll	0: Off 1: On In ACD mode,the polling is automatically initiated whenever an external periodic signal rising edge is detected.During the polling, AutoPoll is set to 0 whenever field strength interrupt is detected.Otherwise enter powerdown mode and wait for the next external periodic signal.
6	-	Reserved for future use
5	RcvOff	Set to logic 1, the analog part of the receiver is switched off.
4	PowerDown	Set to logic 1, Soft Power-down mode is entered. Set to logic 0, the Si512 starts the wake up procedure. During this procedure this bit still shows a 1. A 0 indicates that the Si512 is ready for operations. NOTE: The bit Power Down cannot be set, when the command SoftReset has been activated.
3-0	Command	Activates a command according to the Command Code. Reading this register shows, which command is actually executed.See Command overview.

7.2.3 ComlEnReg

Control bits to enable and disable the passing of interrupt requests.

Table7-6 ComlEnReg Address：02h reset value：80h

	7	6	5	4	3	2	1	0
	IRqInv	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 7-7 Description of CommlEnReg bits

Bit	Symbol	Description
7	IRqInv	Set to logic 1, the signal on pin IRQ is inverted with respect to bit IRq in the register Status1Reg. Set to logic 0, the signal on pin IRQ is equal to bit IRq. In combination with bit IRqPushPull in register DivIEnReg, the default value of 1 ensures, that the output level on pin IRQ is 3-state.
6	TxIEn	Allows the transmitter interrupt request (indicated by bit TxIRq) to be propagated to pin IRQ.

5	RxIEn	Allows the receiver interrupt request (indicated by bit RxIRq) to be propagated to pin IRQ.
4	IdleIEn	Allows the idle interrupt request (indicated by bit IdleIRq) to be propagated to pin IRQ.
3	HiAlertIEn	Allows the high alert interrupt request (indicated by bit HiAlertIRq) to be propagated to pin IRQ.
2	LoAlertIEn	Allows the low alert interrupt request (indicated by bit LoAlertIRq) to be propagated to pin IRQ.
1	ErrIEn	Allows the error interrupt request (indicated by bit ErrIRq) to be propagated to pin IRQ.
0	TimerIEn	Allows the timer interrupt request (indicated by bit TimerIRq) to be propagated to pin IRQ.

7.2.4 DivlEnReg

Control bits to enable and disable the passing of interrupt requests.

Table 7-8 DivIEnReg address：03h reset value：00h

	7	6	5	4	3	2	1	0
	IRQPushPull	CardIRqEn	WdtIRqEn	MFINActIEn	ModeIEn	CRCIEn	RFOnIEn	RFOffIEn
Access	r/w	r/w	/w	r/w	r/w	r/w	r/w	r/w

Table 7-9 Description of DivIEnReg bits

Bit	Symbol	Description
7	IRQPushPull	Set to logic 1, the pin IRQ works as standard CMOS output pad. Set to logic 0, the pin IRQ works as open drain output pad.
6	CardIRqEn	Field strength interrupt enbable 1：enable 0：disable
5	WdtIRqEn	Timed wake-up enable 1：enable 0：disable
4	SiginActIEn	Allows the SIGIN active interrupt request to be propagated to pin IRQ.
3	ModelEn	Allows the mode interrupt request (indicated by bit ModeIRq) to bepropagated to pin IRQ.
2	CRCIEn	Allows the CRC interrupt request (indicated by bit CRCIRq) to be propagated to pin IRQ.
1	RFOnIEn	Allows the RF field on interrupt request (indicated by bit RfOnIRq) to be propagated to pin IRQ.
0	RFOffIEn	Allows the RF field off interrupt request (indicated by bit RfOffIRq) to be propagated to pin IRQ.

7.2.5 ComIrqReg

Contains Interrupt Request bits.

Table 7-10 ComIrqReg address：04h reset value：14h

	7	6	5	4	3	2	1	0
	Set1	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
AccessRights	w	dy	dy	dy	dy	dy	dy	dy

Table 7-11 Description of ComIrqReg

Bit	Symbol	Description
7	Set1	Use with the interrupt flag bit to set interrupt flag 1 or 0. Set to logic 1, Set1 defines that the marked bits in the register CommIRqReg are set. Set to logic 0, Set1 defines, that the marked bits in the register CommIRqReg are cleared.
6	TxIRq	Set to logic 1 immediately after the last bit of the transmitted data was sent out.
5	RxIRq	Set to logic 1 when the receiver detects the end of a valid datastream. If the bit RxNoErr in register RxModeReg is set to logic 1, bit RxIRq is only set to logic 1 when data bytes are available in the FIFO.
4	IdleIRq	Set to logic 1, when a command terminates by itself e.g. when the CommandReg changes its value from any command to the Idle Command.If an unknown command is started, the CommandReg changes its content to the idle state and the bit IdleIRq is set. Starting the Idle Command by the µ-Controller does not set bit IdleIRq.
3	HiAlertIRq	Set to logic 1, when bit HiAlert in register Status1Reg is set. In opposition to HiAlert, HiAlertIRq stores this event and can only be reset as indicated by bit Set1.
2	LoAlertIRq	Set to logic 1, when bit LoAlert in register Status1Reg is set. In opposition to LoAlert, LoAlertIRq stores this event and can only be reset as indicated by bit Set1.
1	ErrIRq	Set to logic 1 if any error bit in the Error Register is set.
0	TimerIRq	Set to logic 1 when the timer decrements the TimerValue Register to zero.

7.2.6 DivIrqReg

Contains Interrupt Request bits。

Table 7-12 DivIrqReg address：05h reset value：xxh，000x00xxb

	7	6	5	4	3	2	1	0
	Set2	CardIRq	WdtIRq	MFINActIRq	ModeIRq	CRCIRq	RFOnIRq	RFOffIRq
Access	w	dy	dy	dy	dy	dy	dy	dy

Table7-13 Description of DivIRqReg bits

Bit	Symbol	Description
7	Set2	Use with the interrupt flag bit to set interrupt flag 1 or 0. Set to logic 1, Set2 defines that the marked bits in the register DivIRqReg are set. Set to logic 0, Set2 defines, that the marked bits in the register DivIRqReg are cleared
6	CardIRq	Field strength interrupt 1：card present 0：no card
5	WdtIRq	Timed wake-up interrupt 1：occurrence timed wake-up interrupt 0：not occurred timed wake-up interrupt
4	SiginActIRq	Set to logic 1, when SIGIN is active. This interrupt is set when either a rising or falling signal edge is detected.
3	ModeIRq	Set to logic 1, when the mode has been detected by the Data mode detector. NOTE: The Data mode detector can only be activated by the AutoColl command and is terminated automatically having detected the Communication mode. NOTE: The Data mode detector is automatically restarted after each RF Reset.
2	CRCIRq	Set to logic 1, when the CRC command is active and all data are processed.
1	RFOnIRq	Set to logic 1, when an external RF field is detected.
0	RFOffIRq	Set to logic 1, when a present external RF field is switched off.

7.2.7 ErrorReg

Error bit register showing the error status of the last command executed.

Table7-14 ErrorReg register Address：06h reset value：00h

	7	6	5	4	3	2	1	0
	WrErr	TempErr	RFErr	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocolErr
Access	r	r	r	r	r	r	r	r

Table7-15 Description of ErrorReg bits

Bit	Symbol	Description
7	WrErr	Set to logic 1, when data is written into FIFO by the host controller during the AutoColl command command or if data is written into FIFO by the host controller during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface.
6	TempErr	Set to logic 1, if the internal temperature sensor detects overheating. In this case, the antenna drivers are switched off automatically.
5	RFErr	Set to logic 1, if in Active Communication mode the counterpart does not switch off the RF field in time as defined in NFCIP-1 standard. NOTE: RFErr is only used in Active Communication mode. The bits RxFraming or the bits TxFraming has to be set to 01 to enable this functionality.
4	BufferOvfl	Set to logic 1, if the host controller or a Si512's internal state machine (e.g. receiver) tries to write data into the FIFO-buffer although the FIFO-buffer is already full.
3	CollErr	Set to logic 1, if a bit-collision is detected. It is cleared automatically at receiver start-up phase. This bit is only valid during the bitwise anticollision at 106 kbits/s. During communication schemes at 212 and 424 kbits/s this bit is always set to logic 0.
2	CRCErr	Set to logic 1, if bit RxCRCEn in register RxModeReg is set and the CRC calculation fails. It is cleared to 0 automatically at receiver start-up phase.
1	ParityErr	Set to logic 1, if the parity check has failed. It is cleared automatically at receiver start-up phase. Only valid for ISO/IEC 14443A or NFCIP-1 communication at 106 kbits/s.
0	ProtocolErr	Set to logic 1, if one out of the following cases occur: • Set to logic 1 if the SOF is incorrect. It is cleared automatically at receiver start-up phase. The bit is only valid for 106 kbits/s in Active and Passive Communication mode.

		• If bit DetectSync in register ModeReg is set to logic 1 during FeliCa communication or active communication with transfer speeds higher than 106 kbits/s, the bit ProtocolErr is set to logic 1 in case of a byte length violation. • During the AutoColl command, bit ProtocolErr is set to logic 1, if the bit Initiator in register ControlReg is set to logic 1. • Set to logic 1, if the Miller Decoder detects 2 pulses below the minimum time according to the ISO/IEC 14443A definitions.

NOTEs：Command execution will clear all error bits except for bit TempErr. A setting by software is impossible.

7.2.8 Status1Reg

Contains status bits of the CRC, Interrupt and FIFO-buffer.

Table7-16 Status1Reg Address：07h reset value：xxh，x100x01xb

	7	6	5	4	3	2	1	0
	RFFreqOK	CRCOk	CRCReady	IRq	TRunning	RFOn	HiAlert	LoAlert
Access	r	r	r	r	r	r	r	r

Table7-17 Description of Status1Reg bits

Bit	Symbol	Description
7	RFFreqOK	Indicates if the frequency detected at the RX pin is in the range of 13.56 MHz. Set to logic 1, if the frequency at the RX pin is in the range 12 MHz < RX pin frequency < 15 MHz. NOTE: The value of RFFreqOK is not defined if the external RF frequency is in the range from 9 to 12 MHz or in the range from 15 to 19 MHz.
6	CRCOk	Set to logic 1, if the CRC Result is zero. For data transmission and reception the bit CRCOk is undefined (use CRCErr in register ErrorReg). CRCOk indicates the status of the CRC co-processor, during calculation the value changes to ZERO, when the calculation is done correctly, the value changes to ONE.
5	CRCReady	Set to logic 1, when the CRC calculation has finished. This bit is only valid for the CRC co-processor calculation using the command CalcCRC.
4	IRq	This bit shows, if any interrupt source requests attention (with respect to the setting of the interrupt enable bits, see register ComIrqReg and DivIEnReg).

3	TRunning	Set to logic 1, if the Si512's timer unit is running, e.g. the timer will decrement the TCounterValReg with the next timer clock. NOTE: In the gated mode the bit TRunning is set to logic 1, when the timer is enabled by the register bits. This bit is not influenced by the gated signal.
2	RFOn	Set to logic 1, if an external RF field is detected. This bit does not store the state of the RF field.
1	HiAlert	Set to logic 1, when the number of bytes stored in the FIFO-buffer fulfills the following equation: HiAlert = (64-FIFOLength)≤WaterLevel
0	LoAlert	Set to logic 1, when the number of bytes stored in the FIFO-buffer fulfills the following equation: LoAlert = FIFOLength≤WaterLevel

7.2.9 Status2Reg

Status bits of receiver, transmitter, and data detectors

Table7-18 Status2Reg Address：08h reset value：00h

	7	6	5	4	3	2	1	0
	TempSensClear	I2CForceHS	0	TargetActivated	0	Modem State		
Access	r/w	r/w	RFU	dy	RFU	r	r	r

Table7-19 Description of Status2Reg bits

Bit	Symbol	Description
7	TempSensClear	Set to logic 1, this bit clears the temperature error, if the temperature is below the alarm limit of 125℃.
6	I2CForceHS	I2C input filter settings. Set to logic 1, the I2C input filter is set to the High-speed mode independent of the I2C protocol. Set to logic 0, the I2C input filter is set to the used I2C protocol.
5	-	Reserved for future use.
4	TargetActivated	Set to logic 1 if the Select command or if the Polling command was answered. NOTE: This bit can only be set during the AutoColl command in Passive Communication mode. NOTE: This bit is cleared automatically by switching off the external RF field.
3	-	Reserved for future use.
2-0	Modem State	ModemState shows the state of the transmitter and receiver state machines.

		Value 000 001 010 011 100 101 110	Description 000 IDLE Wait for StartSend in register BitFramingReg TxWait: Wait until RF field is present, if the bit TxWaitRF is set to logic 1. The minimum time for TxWait is defined by the TxWaitReg register. Sending RxWait: Wait until RF field is present, if the bit RxWaitRF is set to logic 1. The minimum time for RxWait is defined by the RxWait in the RxSelReg register. Wait for data Receiving

7.2.10 FIFODataReg

In- and output of 64 byte FIFO-buffer.

Table7-20 FIFODataReg Address：09h reset value：xxh，xxxxxxxxb

	7	6	5	4	3	2	1	0
	FIFOData							
Access	dy	dy	dy	dy	dy	dy	dy	dy

Table7-21 Description of FIFODataReg bits

Bit	Symbol	Description
7-0	FIFOData	Data input and output port for the internal 64 byte FIFO-buffer. The FIFO-buffer acts as parallel in/parallel out converter for all serial data stream in- and outputs.

7.2.11 FIFOLevelReg

Indicates the number of bytes stored in the FIFO.

Table7-22 PageReg Address：0Ah reset value：00h

	7	6	5	4	3	2	1	0
	FlushBuffer	FIFOLevel						
Access	w	r	r	r	r	r	r	r

Table7-23 Description of FIFOLevelReg bits

Bit	Symbol	Description
7	FlushBuffer	Set to logic 1, this bit clears the internal FIFO-buffer's read- and write-pointer and the bit BufferOvfl in the register ErrReg immediately.Reading this bit will always return 0.
6-0	FIFOLevel	Indicates the number of bytes stored in the FIFO-buffer. Writing to the FIFODataReg increments, reading decrements the FIFOLevel.

7.2.12 WaterLevelReg

Defines the level for FIFO under- and overflow warning.

Table7-24 WaterLevelReg Address：0Bh reset value：08h

	7	6	5	4	3	2	1	0
	0	0	WaterLevel					
Access	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table7-25 Description of WaterLevelReg bits

Bit	Symbol	Description
7-6	-	Reserved for future use.
5-0	WaterLevel	This register defines a warning level to indicate a FIFO-buffer over- or underflow: The bit HiAlert in Status1Reg is set to logic 1, if the remaining number of bytes in the FIFO-buffer space is equal or less than the defined number of WaterLevel bytes. The bit LoAlert in Status1Reg is set to logic 1, if equal or less than WaterLevel bytes are in the FIFO.

7.2.13 ControlReg

Control bit.

Table7-26 ControlReg Address：0Ch reset value：00h

	7	6	5	4	3	2	1	0
	TStopNow	TStartNow	WrNFCIDtoFIFO	Initiator	0	RxLastBits		
Access	w	w	dy	r/w	RFU	r	r	r

Table7-27 Description of ControlReg bits

Bit	Symbol	Description
7	TStopNow	Set to logic 1, the timer stops immediately. Reading this bit will always return 0.
6	TStartNow	Set to logic 1 starts the timer immediately. Reading this bit will always return 0.
5	WrNFCIDtoFIFO	Set to logic 1, the internal stored NFCID (10 bytes) is copied into the FIFO. Afterwards the bit is cleared automatically
4	Initiator	Set to logic 1, the Si512 acts as initiator, otherwise it acts as target
3	-	Reserved for future use.
2-0	RxLastBits	Shows the number of valid bits in the last received byte. If zero, the whole byte is valid.

7.2.14 BitFramingReg

Adjustments for bit oriented frames.

Table7-28 BitFramingReg Address：0Dh reset value：00h

	7	6	5	4	3	2	1	0
	StartSend	RxAlign			0	TxLastBits		
Access	w	r/w	r/w	r/w	RFU	r/w	r/w	r/w

Table7-29 Description of BitFramingReg bits

Bit	Symbol	Description
7	StartSend	Set to logic 1, the transmission of data starts. This bit is only valid in combination with the Transceive command.
6-4	RxAlign	Used for reception of bit oriented frames: RxAlign defines the bit position for the first bit received to be stored in the FIFO. Further received bits are stored at the following bit positions. Example: RxAlign = 0: the LSB of the received bit is stored at bit 0, the second received bit is stored at bit position 1.

		RxAlign = 1: the LSB of the received bit is stored at bit 1, the second received bit is stored at bit position 2. RxAlign = 7: the LSB of the received bit is stored at bit 7, the second received bit is stored in the following byte at bit position 0.
3	-	Reserved for future use.
2-0	TxLastBits	Used for transmission of bit oriented frames: TxLastBits defines the number of bits of the last byte that shall be transmitted. A 000 indicates that all bits of the last byte shall be transmitted.

7.2.15 CollReg

Defines the first bit collision detected on the RF interface.

Table7-30 CollReg Address：0Eh reset value：xxh，101xxxxxb

	7	6	5	4：0
	ValuesAfterColl	0	CollPosNotValid	CollPos
Access	r/w	RFU	r	r

Table7-31 Description of CollReg bits

Bit	Symbol	Description
7	ValuesAfterColl	If this bit is set to logic 0, all receiving bits will be cleared after a collision. This bit shall only be used during bitwise anticollision at 106 kbit, otherwise it shall be set to logic 1.
6	-	Reserved for future use.
5	CollPosNotValid	Set to logic 1, if no Collision is detected or the Position of the Collision is out of the range of bits CollPos. This bit shall only be interpreted in Passive Communication mode at 106 kbit or ISO/IEC 14443A Reader/Writer mode.
4-0	CollPos	These bits show the bit position of the first detected collision in a received frame, only data bits are interpreted. Example: 00h: indicates a bit collision in the 32th bit 01h: indicates a bit collision in the 1st bit 08h: indicates a bit collision in the 8th bit

		These bits shall only be interpreted in Passive Communication mode at 106 kbit or ISO/IEC 14443A Reader/Writer mode if bit CollPosNotValid is set to logic 0.

7.2.16 PollReg

Address 0x0f multiplexes 16 sets of registers, which is selected by the address 0x00/0x10/0x20/0x30 register.

Table7-32 PollReg Address：0Fh reset value：xxh，See the table below

Address	Bit	Symbol	Access	reset value	Description
0F_A		RCCfg1		05h	3K RC configuration 1
	7	Trimsel	r/w	0b	1：manual correction 0：automatic correction
	6	Max	r/w	0b	1：rectification
	5:0	mdelay	r/w	000101b	ACD wake up interval (mdelay+1)*100ms， min:100ms，max:6400ms
0F_B		ACRDCfg		02h	3K RC configuration1
	7:6	ACDEdge	r/w	00b	Definition： LSample: last sampling value CSample: sampling value for this card inspection ValSet: value of 0F_C[6:0] ValDelta: value of 0F_D[6:0] Absolute value mode card decision condition 00/11：CSample > ValSet + ValDelta or CSample < ValSet – ValDelta 01：CSample > ValSet + ValDelta 10：CSample < ValSet – ValDelta Relative value mode card decision condition 00/11：CSample > LSample+ ValDelta or CSample < LSample– ValDelta 01：CSample > LSample+ ValDelta 10：CSample < LSample– ValDelta
	5	ACDMode	r/w	0b	0：absolute value comparison 1：relative value comparison

	4:3	ACDRFEn	r/w	00b	01：enable low-power card detection 10：enable low-power RF detection 00/11：enable low-power card detection and RF detection at same time.
	2:1	MaskACD	r/w	01b	Under the ACD mode 00：from the 3rd round of polling to detect the card or RF field 01：from the 4th round of polling to detect the card or RF field 10：from the 5th round of polling to detect the card or RF field 11：from the 6th round of polling to detect the card or RF field
	0	-			reserved
0F_C		ValSet		70h	Manual mode reference value
	7	-	RFU	0b	
	6:0	ValSet	r/w	1110000b	Manually setting the reference value for card free field strength
0F_D		ValDelta		0fh	Field strength variation range
	7	-	RFU	0	
	6:0	ValDelta	r	0001111b	Setting the range of field strength variation
0F_E		-	-	03h	reserved
	7	-	-	-	reserved
	6	-	-		reserved
	5	-	-		reserved
	4:3	-	-		reserved
	2:0	-	-		reserved
0F_F		RCCFG1		c0h	3K RC configuration2
	7	OMEN	r/w	1b	1：enable OSC detecting 0：disable OSC detecting
	6:0	TRIMSET	r/w	1000000b	Manually setting correction values of RCOSC
0F_G		ADCVal		xx	Polling ADC sampling values
	7	-	RFU	0b	
	6:0	VAL_ADC	r	x	ADC sampling values

0F_H		WdtCnt		26h	Watchdog interrupt generation interval setting
	7:0	WdtCnt	r/w	00100110b	In polling mode,the watchdog counter is added by 1 every time the card is checked.When the watchdog counter value is equall to WdtCnt,a watchdog interrupt is generated,while watchdog counts is recounting but it des not wake the chip.
0F_I		ARI		00h	
	7:6	-	-	-	
	5:4	TK	r/w	00b	Detection front-end amplifier control 00/11: detection front-end amplifier OFF 01: detect front-end amplification by 10 10: detect front-end amplification by 21
	3	-	-	-	
	2	ARIPol	r/w	0b	ARI polarity control 1: ARI low level indication RF is on in ACD mode 0: ARI high level indication RF is on in ACD mode
	1	ARIEn	r/w	0b	ARI enable 1: enable,D1 output ARI 0: disable,don't affect the status of pin D1
	0	ARI	r	x	In ACD mode RF status indication
0F_J		ACC	-	-	Whether detecting configuration lost in ACD mode.
	7	ACCErr	r	0	0：polling configuration data is not lost 1：polling configuration data is lost Only ACCEn=1,enable
	6	ACCEn	r/w	0	ACC enable,this bit must be reset before configure the ACD register 0：write 55h set to 0 1：write not 55h set to 1
	5:0	-	-	0	reserved
0F_K		LPDCFG1		0fh	
	7	-	-	-	reserved
	6:5	TR	r/w	00b	Subtractor gain control word in detection circuit

					00：1 time 01：3 times 10：7 times 11：15 times
	4:3	TI	r/w	01b	Front detection operational amplifier slope control word in detection circuit 00：0.5 01：1 10：1.5 11：2
	2:0	VCON	r/w	111b	The ADC reference voltage control when detection. The detection module output is located within the ADC range by configuring this bit. 000：1.407V 001：1.472V 010：1.537V 011：1.603V 100：1.66V 101：1.718V 110：1.8V 111：1.9V
0F_L		-	-	-	reserved
0F_M		RFLowDetect		08h	Low RF monitoring configuration during ACD
	7	RFLowDetectEn	r/w	0b	1：enable RF anomaly detection sent by Reader 0：close RF anomaly detection sent by Reader
	6:0	RFLowThreshold	r/w	0001000b	Determine if RF is too slow during card checking Threshold optional range 0~128. Threshold calculation formula：RFLowThreshold
0F_N		ExRFDetect		08h	External RF monitoring configuration during ACD
	7	-	RFU	0	
	6:0	RFNoThreshold	r/w	0001000b	Determine whether there is any other RF threshold in the surrounding area
0F_O		ACRDIRqEn		00h	ACD related interrupt enable
	7:4	-	RFU	0b	

	3	OSCMonIrqEn	r/w	0b	1:enable OSCMonIrqEn interrupt
	2	-	RFU	0b	
	1	RFLowIrqEn	r/w	0b	1: enable RFLowIrq interrupt
	0	RFExIrqEn	r/w	0b	1: enable RFExIrq interrupt
0F_P		ACRDIRq		00h	ACD related interrupt enable
	7	set3	w	0b	cooperate with the interrupt bit,it is used to set or reset interrupt position. 0: the corresponding interrupt bit is cleared by writing 1 1: the corresponding interrupt bit is set by writing 1
	6:4	-	RFU	0b	
	3	OSCMonIrq	dy	0b	1：OSC four consecutive wake-up failures
	2	-	RFU	0b	reserved
	1	RFLowIrq	dy	0b	1：RF value too low during card detecting
	0	RFExIrq	dy	0b	1：external RF detected

7.3 PAGE1：communication

7.3.1 PageReg

Table7-33 PageReg Address：10h reset value：00h

	7	6	5：2	1	0
	UsePage Select	Regbank Select	RegSelect	PageSelect	
Access	r/w	r/w	r/w	r/w	r/w

Table7-34 Description of PageReg bits

Bit	Symbol	Description
7	UsePageSelect	Set to logic 1, the value of PageSelect is used as register address A5 and A4. The LSB-bits of the register address are defined by the address pins or the internal address latch, respectively. Set to logic 0, the whole content of the internal address latch defines the register address. The address pins are used as described in Automatic microcontroller interface detection.
6	RegbankSelect	Set to logic 1，it is used to read/write 0Fh register set
5-2	RegSelect	0000：read/write register set A； 0001：read/write register set B； … 1111：read/write register set P
1-0	PageSelect	The value of PageSelect is used only, if UsePageSelect is set to logic 1. In this case it specifies the register page (which is A5 and A4 of the register address).

7.3.2 ModeReg

Defines general mode settings for transmitting and receiving.

Table7-35 ModeReg Address：11h reset value：3Bh

	7	6	5	4	3	2	1：0
	MSBFirst	Detect Sync	TxWaitRF	RxWaitRF	PolMFIN	ModeDetOff	CRCPreset
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-36 Description of ModeReg bits

Bit	Symbol	Description
7	MSBFirst	Set to logic 1, the CRC co-processor calculates the CRC with MSB first and the CRCResultMSB and the CRCResultLSB in the CRCResultReg register are bit reversed. NOTE: During RF communication this bit is ignored.
6	Detect Sync	If set to logic 1, the contactless UART waits for the value F0h before the receiver is activated and F0h is added as a Sync-byte for transmission. This bit is only valid for 106 kbit during NFCIP-1 data exchange protocol.

		In all other modes it shall be set to logic 0.
5	TxWaitRF	Set to logic 1 the transmitter in reader/writer or initiator mode for NFCIP-1 can only be started, if an RF field is generated.
4	RxWaitRF	Set to logic 1, the counter for RxWait starts only if an external RF field is detected in Target mode for NFCIP-1 or in Card Communication mode.
3	PolSigin	PolSigin defines the polarity of the SIGIN pin. Set to logic 1, the polarity of SIGIN pin is active high. Set to logic 0 the polarity of SIGIN pin is active low. NOTE: The internal envelope signal is coded active low. NOTE: Changing this bit will generate a SiginActIRq event.
S	ModeDetOff	Set to logic 1, the internal mode detector is switched off. NOTE: The mode detector is only active during the AutoColl command.
1-0	CRCPreset	Defines the preset value for the CRC co-processor for the command CalCRC. NOTE: During any communication, the preset values is selected automatically according to the definition in the bits RxMode and TxMode.

Value	Description
00	0000
01	6363
10	A671
11	FFFF

7.3.3 TxModeReg

Defines the data rate and framing during transmission

Table7-37 TxModeReg Address：12h reset value：00h

	7	6	5	4	3	2	1	0
	TxCRCEn	TxSpeed			InvMod	TxMix	TxFraming	
Access	r/w	dy	dy	dy	r/w	r/w	dy	dy

Table7-38 Description of TxModeReg bits

Bit	Symbol	Description	
7	TxCRCEn	Set to logic 1, this bit enables the CRC generation during data transmission. NOTE: This bit shall only be set to logic 0 at 106 kbit.	
6-4	TxSpeed	Defines the bit rate while data transmission.	
		Value	Description
		000	106kbits/s
		001	212kbits/s
		010	424kbits/s
		011	Reserved
		100	Reserved
		101	Reserved
		110	Reserved
		111	Reserved
3	InvMod	Set to logic 1, the modulation for transmitting data is inverted.	
2	TxMix	Set to logic 1, the signal at pin MFIN is mixed with the internal coder	
1-0	TxFraming	Defines the framing used for data transmission.	
		Value	Description
		00	ISO/IEC 14443A and Passive Communication mode 106 kbit
		01	Active Communication mode
		10	FeliCa and Passive communication mode 212 and 424 kbit
		11	ISO/IEC 14443B

7.3.4 RxModeReg

Defines the data rate and framing during reception.

Table7-39 RxModeReg Address：13h reset value：00h

	7	6	5	4	3	2	1	0
	RxCRCEn	RxSpeed			RxNoErr	RxMultiple	RxFraming	
Access	r/w	dy	dy	dy	r/w	r/w	dy	dy

Table7-40 Description of RxModeReg bits

<table>
<tr><td>Bit</td><td>Symbol</td><td colspan="2">Description</td></tr>
<tr><td>7</td><td>RxCRCEn</td><td colspan="2">Set to logic 1, this bit enables the CRC calculation during reception.
NOTE: This bit shall only be set to logic 0 at 106 kbit.</td></tr>
<tr><td rowspan="2">6-4</td><td rowspan="2">RxSpeed</td><td colspan="2">Defines the bit rate while data transmission.
The Si512’s analog part handles only transfer speeds up to 424 kbit internally, the digital UART handles the higher transfer speeds as well.</td></tr>
<tr><td>Value
000
001
010
011
100
101
110
111</td><td>Description
106kbits/s
212kbits/s
424kbits/s
Reserved
Reserved
Reserved
Reserved
Reserved</td></tr>
<tr><td>3</td><td>RxNoErr</td><td colspan="2">If set to logic 1 a not valid received data stream (less than 4 bits received) will be ignored. The receiver will remain active. For ISO/IEC14443B also RxSOFReq logic 1 is required to ignore a non valid datastream.</td></tr>
<tr><td>2</td><td>RxMultiple</td><td colspan="2">Set to logic 0, the receiver is deactivated after receiving a data frame.
Set to logic 1, it is possible to receive more than one data frame. Having set this bit, the receive and transceive commands will not terminate automatically. In this case the multiple receiving can only be deactivated by writing any command (except the Receive command) to the CommandReg register or by clearing the bit by the host controller. At the end of a received data stream an error byte is added to the FIFO. The error byte is a copy of the ErrorReg register.</td></tr>
<tr><td rowspan="2">1-0</td><td rowspan="2">RxFraming</td><td colspan="2">Defines the expected framing for data reception.</td></tr>
<tr><td>Value
00
01
10
11</td><td>Description
ISO/IEC 14443A and Passive Communication mode 106 kbit
Active Communication mode
FeliCa and Passive Communication mode 212 and 424 kbit
ISO 14443B</td></tr>
</table>

7.3.5 TxControlReg

Controls the logical behavior of the antenna driver pins Tx1 and Tx2.

Table7-41 TxControlReg Address：14h reset value：80h

	7	6	5	4	3	2	1	0
	InvTx2RFOn	InvTx1RFOn	InvTx2RFOff	InvTx1RFOff	Tx2CW	CheckRF	Tx2RFEn	Tx1RFEn
Access	r/w	r/w	r/w	r/w	r/w	w	r/w	r/w

Table7-42 Description of TxControlReg bits

Bit	Symbol	Description
7	InvTx2RFOn	Set to logic 1, the output signal at pin TX2 will be inverted, if driver TX2 is enabled.
6	InvTx1RFOn	Set to logic 1, the output signal at pin TX1 will be inverted, if driver TX1 is enabled.
5	InvTx2RFOff	Set to logic 1, the output signal at pin TX2 will be inverted, if driver TX2 is disabled.
4	InvTx1RFOff	Set to logic 1, the output signal at pin TX1 will be inverted, if driver TX1 is disabled.
3	Tx2CW	Set to logic 1, the output signal on pin TX2 will deliver continuously the un-modulated 13.56 MHz energy carrier. Set to logic 0, Tx2CW is enabled to modulate the 13.56 MHz energy carrier.
2	CheckRF	Set to logic 1, Tx2RFEn and Tx1RFEn can not be set if an external RF field is detected. Only valid when using in combination with bit Tx2RFEn or Tx1RFEn
1	Tx2RFEn	Set to logic 1, the output signal on pin TX2 will deliver the 13.56 MHz energy carrier modulated by the transmission data.
0	Tx1RFEn	Set to logic 1, the output signal on pin TX1 will deliver the 13.56 MHz energy carrier modulated by the transmission data.

7.3.6 TxAutoReg

Controls the settings of the antenna driver.

Table7-43 TxAutoReg Address：15h reset value：00h

	7	6	5	4	3	2	1	0
	AutoRFOFF	Force100ASK	Auto WakeUp	0	CAOn	InitialRFOn	Tx2RFAutoEn	Tx1RFAutoEn
Access	r/w	r/w	r/w	RFU	r/w	r/w	r/w	r/w

Table7-44 Description of TxAutoReg bits

Bit	Symbol	Description
7	AutoRFOFF	Set to logic 1, all active antenna drivers are switched off after the last data bit has been transmitted as defined in the NFCIP-1.
6	Force100ASK	Set to logic 1, Force100ASK forces a 100% ASK modulation independent of the setting in register ModGsPReg.
5	AutoWakeUp	Set to logic 1, the Si512 in soft Power-down mode will be started by the RF level detector.
4	-	Reserved for future use
3	CAOn	Set to logic 1, the collision avoidance is activated and internally the value n is set in accordance to the NFCIP-1 Standard.
2	InitialRFOn	Set to logic 1, the initial RF collision avoidance is performed and the bit InitialRFOn is cleared automatically, if the RF is switched on. NOTE: The driver, which should be switched on, has to be enabled by bit Tx2RFAutoEn or bit Tx1RFAutoEn.
1	Tx2RFAutoEn	Set to logic 1, the driver Tx2 is switched on after the external RF field is switched off according to the time TADT. If the bits InitialRFOn and Tx2RFAutoEn are set to logic 1, Tx2 is switched on if no external RF field is detected during the time TIDT.The times TADT and TIDT are defined in the NFC IP-1 standard (ISO/IEC 18092).
0	Tx1RFAutoEn	Set to logic 1, the driver Tx1 is switched on after the external RF field is switched off according to the time TADT. If the bit InitialRFOn and Tx1RFAutoEn are set to logic 1, Tx1 is switched on if no external RF field is detected during the time TIDT.

		NOTE: The times TADT and TIDT are defined in the NFC IP-1 standard (ISO/IEC 18092).

7.3.7 TxSelReg

Selects the sources for the analog part.

Table7-45 TxSelReg Address：16h reset value：10h

	7	6	5	4	3	2	1	0
	0	0	DriverSel		MFOUTSel			
Access	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table7-46 Description of TxSelReg bits

Bit	Symbol	Description	
7-6	-	Reserved for future use.	
5-4	DriverSel	Selects the input of driver Tx1 and Tx2.	
		value	Description
		00	Tristate NOTE: In soft power down the drivers are only in Tristate mode if DriverSel is set to Tristate mode.
		01	Modulation signal (envelope) from the internal coder
		10	Modulation signal (envelope) from SIGIN
		11	HIGH NOTE: The HIGH level depends on the setting of InvTx1RFOn/ InvTx1RFOff and InvTx2RFOn/InvTx2RFOff.
3-0	SigOUTSel	Selects the input for the SIGOUT Pin.	
		value	Description
		0000	Tristate
		0001	Low
		0010	High
		0011	TestBus signal as defined by bit TestBusBitSel in register
		0100	TestSel1Reg.
		0101	Modulation signal (envelope) from the internal coder
		0110	Serial data stream to be transmitted

			Output signal of the receiver circuit (card modulation signal regenerated and delayed). This signal is used as data output signal for SAM interface connection using 3 lines. NOTE: To have a valid signal the Si512 has to be set to the receiving mode by either the Transceive or Receive command. The bit RxMultiple can be used to keep the Si512 in receiving mode.
		0111	NOTE: Manchester coding as data collisions will not be transmitted on the SIGOUT line. Serial data stream received.
		1000-1011	NOTE: Miller coding parameters as the bit length can vary. FeliCa Sam modulation 1000 RX* 1001 TX 1010 Demodulator comparator output 1011 RFU NOTE: * To have a valid signal the Si512 has to be set to the receiving mode by either the Transceive or Receive command. The bit RxMultiple can be used to keep the Si512 in receiving mode.
		1100-1111	Sam modulation 1100 RX* with RF carrier 1101 TX with RF carrier 1110 RX with RF carrier un-filtered 1111 RX envelope un-filtered NOTE: *To have a valid signal the Si512 has to be set to the receiving mode by either the Transceive or Receive command. The bit RxMultiple can be used to keep the Si512 in receiving mode.

7.3.8 RxSelReg

Selects internal receiver settings.

Table7-47 RxSelReg Address：17h reset value：84h

	7	6	5	4	3	2	1	0
	UartSel		RxWait					
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-48 Description of RxSelReg bits

Bit	Symbol	Description	
7-6	UartSel	Selects the input of the contactless UARTDescription	
		Value	Description
		00	Constant Low
		01	Envelope signal at SIGIN
		10	Modulation signal from the internal analog part
		11	Modulation signal from SIGIN pin. Only valid for transfer speeds above 424 kbit
5-0	RxWait	After data transmission, the activation of the receiver is delayed for RxWait bit-clocks. During this ‘frame guard time’any signal at pin RX is ignored. This parameter is ignored by the Receive command. All other commands (e.g.Transceive, Autocoll) use this parameter. Depending on the mode of the Si512, the counter starts different. In Passive Communication mode the counter starts with the last modulation pulse of the transmitted data stream. In Active Communication mode the counter starts immediately after the external RF field is switched on.	

7.3.9 RxThresholdReg

Selects thresholds for the bit decoder.

Table7-49 RxThresholdReg Address：18h reset value：84h

	7	6	5	4	3	2	1	0
	MinLevel				0	CollLevel		
Access	r/w	r/w	r/w	r/w	RFU	r/w	r/w	r/w

Table7-50 Description of RxThresholdReg bits

Bit	Symbol	Description
7-4	MinLevel	Defines the minimum signal strength at the decoder input that shall be accepted. If the signal strength is below this level, it is not evaluated.
3	-	Reserved for future use.
2-0	CollLevel	Defines the minimum signal strength at the decoder input that has to be reached by the weaker half-bit of the Manchester-coded signal to generate a bit-collision relatively to the amplitude of the stronger half-bit.

7.3.10 DemodReg

Defines demodulator settings.

Table7-51 DemodReg Address：19h reset value：4Dh

	7	6	5	4	3	2	1	0
	AddIQ		FixIQ	TPrescal Even	TauRcv		TauSync	
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-52 Description of DemodReg bits

Bit	Symbol	Description	
7-6	AddIQ	Defines the use of I and Q channel during reception NOTE: FixIQ has to be set to logic 0 to enable the following settings.	
		Value	Description
		00	Select the stronger channel
		01	Select the stronger and freeze the selected during communication
		10	combines the I and Q channel
		11	Reserved
5	FixIQ	If set to logic 1 and the bits of AddIQ are set to X0, the reception is fixed to I channel. If set to logic 1 and the bits of AddIQ are set to X1, the reception is fixed to Q channel. NOTE: If SIGIN/SIGOUT is used as S2C interface FixIQ set to 1 and AddIQ set to X0 is rewired.	
4	TPrescalEven	If set to logic 0 the following formula is used to calculate fTimer of the prescaler: fTimer = 13.56 MHz / (2 * TPreScaler + 1). If set to logic 1 the following formula is used to calculate fTimer of the prescaler:	

		fTimer = 13.56 MHz / (2 * TPreScaler + 2). (Default TPrescalEven is logic 0)
3-2	TauRcv	Changes the time constant of the internal during data reception. NOTE: If set to 00, the PLL is frozen during data reception.
1-0	TauSync	Changes the time constant of the internal PLL during burst.

7.3.11 FelNFC1Reg

Defines the length of the FeliCa Sync bytes and the minimum length of the received packet.

Table7-53 FelNFC1Reg Address：00h reset value：00h

	7	6	5	4	3	2	1	0
	FelSyncLen		DataLenMin					
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-54 Description of FelNFC1Reg bits

Bit	Symbol	Description	
7-6	FelSyncLen	Defines the length of the Sync bytes.	
		Value	Sync- bytes in hex
		00	B2 4D
		01	00 B2 4D
		10	00 00 B2 4D
		11	00 00 00 B2 4D
5-0	DataLenMin	These bits define the minimum length of the accepted packet length: DataLenMin * 4 ≤ data packet length This parameter is ignored at 106 kbit if the bit DetectSync in register ModeReg is set to logic 0. If a received data packet is shorter than the defined DataLenMin value, the data packet will be ignored.	

7.3.12 FelNFC2Reg

Defines the maximum length of the received packet.

Table7-55 FelNFC2Reg Address：1Bh reset value：00h

	7	6	5：0
	WaitForSelected	ShortTimeSlot	DataLenMax
Access	r/w	r/w	r/w

Table7-56 Description of FelNFC2Reg bits

Bit	Symbol	Description
7	WaitForSelected	Set to logic 1, the AutoColl command is only terminated automatically when: 1. A valid command has been received after performing a valid Select procedure according ISO/IEC 14443A. 2. A valid command has been received after performing a valid Polling procedure according to the FeliCa specification. NOTE: If this bit is set, no active communication is possible. NOTE: Setting this bit reduces the host controller interaction in case of a communication to another device in the same RF field during Passive Communication mode.
6	ShortTimeSlot	Defines the time slot length for Passive Communication mode at 424 kbit. Set to logic 1 a short time slot is used (half of the timeslot at 212 kbit). Set to logic 0 a long timeslot is used (equal to the timeslot for 212 kbit).
5-0	DataLenMax	These bits define the maximum length of the accepted packet length: DataLenMax * 4 ≥ data packet length NOTE: If set to logic 0 the maximum data length is 256 bytes. This parameter is ignored at 106 kbit if the bit DetectSync in register ModeReg is set to logic 0. If a received packet is larger than the defined DataLenMax value, the packet will be ignored.

7.3.13 MifNFCReg

Defines ISO/IEC 14443A/NFC specific settings in target or Card Operating mode.

Table7-57 MifNFCReg Address：1Ch reset value：62h

	7	6	5	4	3	2	1	0
	SensMiller			TauMiller		MFHalted	Txwait	
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-58 Description of MifNFCReg bits

Bit	Symbol	Description
7-5	SensMiller	These bits define the sensitivity of the Miller decoder.
4-3	TauMiller	These bits define the time constant of the Miller decoder.
2	MFHalted	Set to logic 1, this bit indicates that the Si512 is set to HALT mode in Card Operation mode at 106 kbit. This bit is either set by the host controller or by the internal state machine and indicates that only the code 52h is accepted as a request command. This bit is cleared automatically by a RF reset.
1-0	Txwait	These bits define the minimum response time between receive and transmit in number of data bits + 7 data bits. The shortest possible minimum response time is 7 data bits. (TxWait=0). The minimum response time can be increased by the number of bits defined in TxWait. The longest minimum response time is 10 data bits (TxWait = 3). If a transmission of a frame is started before the minimum response time is over, the Si512 waits before transmitting the data until the minimum response time is over. If a transmission of a frame is started after the minimum response time is over, the frame is started immediately if the data bit synchronization is correct. (adjustable with TxBitPhase).

7.3.14 ManualRCVReg

Allows manual fine tuning of the internal receiver.

NOTE: For standard applications it is not recommended to change this register settings.

Table7-59 ManualRCVReg Address：1Dh reset value：00h

	7	6	5	4	3	2	1：0
	0	FastFilt MF_SO	Delay MF_SO	Parity Disable	LargeBWPLL	Manual HPCF	HPCF
Access	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table7-60 Description of ManualRCVReg bits

Bit	Symbol	Description
7	-	Reserved for future use.
6	FastFilt MF_SO	If this bit is set to logic 1, the internal filter for the Miller-Delay Circuit is set to Fast mode. NOTE: This bit should only set to logic 1, if Millerpulses of less than 400 ns Pulse length are expected. At 106 kBaud the typical value is 3 us.
5	Delay MF_SO	If this bit is set to logic 1, the Signal at SIGOUT-pin is delayed, so that in SAM mode the Signal at SIGIN must be 128/fc faster compared to the ISO/IEC 14443A, to reach the ISO/IEC 14443A restrictions on the RF-Field. NOTE: This delay shall only be activated for setting bits SigOUTSel to (1110b) or (1111b) in register TxSelReg.
4	ParityDisable	If this bit is set to logic 1, the generation of the Parity bit for transmission and the Parity-Check for receiving is switched off. The received Parity bit is handled like a data bit.
3	LargeBWPLL	Set to logic 1, the bandwidth of the internal PLL used for clock recovery is extended.
2	ManualHPCF	Set to logic 0, the HPCF bits are ignored and the HPCF settings are adapted automatically to the receiving mode. Set to logic 1, values of HPCF are valid.
1-0	HPCF	Selects the High Pass Corner Frequency (HPCF) of the filter in the internal receiver chain. 00: For signals with frequency spectrum down to 106 kHz. 01: For signals with frequency spectrum down to 212 kHz. 10: For signals with frequency spectrum down to 424 kHz. 11: For signals with frequency spectrum down to 848 kHz

7.3.15 TypeBReg

Table7-61 TypeBReg Address：1Eh reset value：00h

	7	6	5	4	3	2	1：0
	RxSOF Req	RxEOF Req	0	EOFSOF Width	NoTxSOF	NoTxEOF	TxEGT
Access	r/w	r/w	RFU	r/w	r/w	r/w	r/w

Table7-62 Description of TypeBReg bits

Bit	Symbol	Description
7	RxSOFReq	If this bit is set to logic 1, the SOF is required. A datastream starting without SOF is ignored. If this bit is cleared, a datastream with and without SOF is accepted. The SOF will be removed and not written into the FIFO.
6	RxEOFReq	If this bit is set to logic 1, the EOF is required. A datastream ending without EOF will generate a Protocol-Error. If this bit is cleared, a datastream with and without EOF is accepted. The EOF will be removed and not written into the FIFO.
5	-	Reserved for future use.
4	EOFSOFWidth	If this bit is set to logic 1 and EOFSOFAdjust bit is logic 0, the SOF and EOF will have the maximum length defined in ISO/IEC 14443B.If this bit is cleared and EOFSOFAdjust bit is logic 0, the SOF and EOF will have the minimum length defined in ISO/IEC 14443B. If this bit is set to 1 and the EOFSOFadjust bit is logic 1 will result in SOF low = (11etu − 8 cycles)/fc SOF high = (2 etu + 8 cycles)/fc EOF low = (11 etu − 8 cycles)/fc If this bit is set to 0 and the EOFSOFAdjust bit is logic 1 will result in an incorrect system behavior in respect to ISO specification.
3	NoTxSOF	If this bit is set to logic 1, the generation of the SOF is suppressed.
2	NoTxEOF	If this bit is set to logic 1, the generation of the EOF is suppressed.
1-0	TxEGT	These bits define the length of the EGT. Value Description 00 0bit 01 1bit 10 2bit 11 3bit

7.3.16 SerialSpeedReg

Selects the speed of the serial UART interface.

Table7-63 SerialSpeedReg Address：1Fh reset value：EBh

	7	6	5	4	3	2	1	0
	BR_T0			BR_T1				
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-64 Description of SerialSpeedReg bits

Bit	Symbol	Description
7-5	BR_T0	Factor BR_T0 to adjust the transfer speed, for description see Section Selectable UART transfer speeds
4-0	BR_T1	Factor BR_T1 to adjust the transfer speed, for description see Section Selectable UART transfer speeds

7.4 PAGE2：configuration

7.4.1 PageReg

Table7-65 PageReg Address：20h reset value：00h

	7	6	5	4	3	2	1	0
	UsePage Select	Regbank Select	RegSelect				PageSelect	
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-66 Description of PageReg bits

Bit	Symbol	Description
7	UsePageSelect	Set to logic 1, the value of PageSelect is used as register address A5 and A4. The LSB-bits of the register address are defined by the address pins or the internal address latch, respectively. Set to logic 0, the whole content of the internal address latch defines the register address. The address pins are used as described in SectionAutomatic microcontroller interface detection
6	RegbankSelect	Set to logic 1，it is used to read/write 0Fh register set

5-2	RegSelect	0000：read/write register set A； 0001：read/write register set B； … 1111：read/write register set P
1-0	PageSelect	The value of PageSelect is used only if UsePageSelect is set to logic 1. In this case, it specifies the register page (which is A5 and A4of the register address).

7.4.2 CRCResultReg

Shows the actual MSB and LSB values of the CRC calculation.

NOTE: The CRC is split into two 8-bit register.

NOTE: Setting the bit MSBFirst in ModeReg register reverses the bit order, the byte order is not changed.

Table7-67 CRCResultReg Address：21h reset value：FFh

	7	6	5	4	3	2	1	0
	CRCResultMSB							
Access	r	r	r	r	r	r	r	r

Table7-68 Description of CRCResultReg bits

Bit	Symbol	Description
7:0	CRCResultMSB	This register shows the actual value of the most significant byte of the CRCResultReg register. It is valid only if bit CRCReady in register Status1Reg is set to logic 1.

Table7-69 CRCResultReg Address：22h reset value：FFh

	7	6	5	4	3	2	1	0
	CRCResultLSB							
Access	r	r	r	r	r	r	r	r

Table7-70 Description of CRCResultReg bits

Bit	Symbol	Description
7:0	CRCResultLSB	This register shows the actual value of the least significant byte of the CRCResultReg register. It is valid only if bit CRCReady in register Status1Reg is set to logic 1.

7.4.3 GsNOffReg

Selects the conductance for the N-driver of the antenna driver pins TX1 and TX2 when the driver is switched off.

Table7-71 GsNOffReg Address：23h reset value：88h

	7	6	5	4	3	2	1	0
	CWGsNOff				ModGsNOff			
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-72 Description of GsNOffReg bits

Bit	Symbol	Description
7-4	CWGsNOff	The value of this register defines the conductance of the output N-driver during times of no modulation. NOTE: The conductance value is binary weighted. NOTE: During soft Power-down mode the highest bit is forced to 1. NOTE: The value of the register is only used if the driver is switched off. Otherwise the bit value CWGsNOn of register GsNOnReg is used
3-0	ModGsNOff	The value of this register defines the conductance of the output N-driver for the time of modulation. This may be used to regulate the modulation index. NOTE: The conductance value is binary weighted. NOTE: During soft Power-down mode the highest bit is forced to 1. NOTE: The value of the register is only used if the driver is switched off. Otherwise the bit value ModGsNOn of register GsNOnReg is used.

7.4.4 ModWidthReg

Controls the modulation width settings.

Table7-73 ModWidthReg Address：24h reset value：26h

	7	6	5	4	3	2	1	0
	ModWidth							
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-74 Description of ModWidthReg bits

Bit	Symbol	Description
7-0	ModWidth	These bits define the width of the Miller modulation as initiator in Active and Passive Communication mode as multiples of the carrier frequency (ModWidth + 1/fc). The maximum value is half the bit period. The resulting number of carrier periods are calculated according to the following formulas: LOW value: #clocksLOW = (ModWidth modulo 8) + 1. HIGH value: #clocksHIGH = 16-#clocksLOW. Acting as a target in Passive Communication mode at 106 kbit or in Card Operating mode for ISO/IEC 14443A these bits are used to change the duty cycle of the subcarrier frequency.

7.4.5 TxBitPhaseReg

Configures the receiver gain and RF level detector sensitivity

Table7-75 TxBitPhaseReg Address：25h reset value：87h

	7	6：0
	RcvClkChange	TxBitPhase
Access	r/w	r/w

Table7-76 Description of TxBitPhaseReg bits

Bit	Symbol	Description
7	RcvClkChange	Set to logic 1, the demodulator’s clock is derived by the external RF field.
6-0	TxBitPhase	These bits are representing the number of carrier frequency clock cycles, which are added to the waiting period before transmitting data in all communication modes.

		TXBitPhase is used to adjust the TX bit synchronization during passive NFCIP-1 communication mode at 106 kbit and in ISO/IEC 14443A card mode.

7.4.6 RFCfgReg

Configures the receiver gain and RF level detector sensitivity.

Table7-77 RFCfgReg Address：26h reset value：48h

	7	6：3	2	1	0
	RFLevelAmp	RxGain	RFLevel		
Access	r/w	r/w	r/w	r/w	r/w

Table7-78 Description of RFCfgReg bits

Bit	Symbol	Description	
7	RFLevelAmp	Set to logic 1, this bit activates the RF level detectors' amplifier.	
6-3	RxGain	This register defines the receivers signal voltage gain factor:	
		Value	Gain
		000	18dB
		001	23dB
		010	18dB
		011	23dB
		100	33dB
		101	38dB
		110	43dB
		111	48dB
2-0	RFLevel	Defines the sensitivity of the RF level detector, for description see Section RF level detector	

7.4.7 GsNOnReg

Selects the conductance for the N-driver of the antenna driver pins TX1 and TX2 when the driver is switched on.

Table7-79 GsNOnReg Address：27h reset value：88h

	7	6	5	4	3	2	1	0
	CWGsNOn				ModGsNOn			
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-80 Description of GsNOnReg bits

Bit	Symbol	Description
7-4	CWGsNOn	The value of this register defines the conductance of the output N-driver during times of no modulation. This may be used to regulate the output power and subsequently current consumption and operating distance. NOTE: The conductance value is binary weighted. NOTE: During soft Power-down mode the highest bit is forced to 1. NOTE: This value is only used if the driver TX1 or TX2 are switched on. Otherwise the value of the bits CWGsNOff of register GsNOffReg is Used..
3-0	ModGsNOn	The value of this register defines the conductance of the output N-driver for the time of modulation. This may be used to regulate the modulation index. NOTE: The conductance value is binary weighted. NOTE: During soft Power-down mode the highest bit is forced to 1. NOTE: This value is only used if the driver TX1 or Tx2 are switched on. Otherwise the value of the bits ModsNOff of register GsNOffReg is used.

7.4.8 CWGsPReg

Defines the conductance of the P-driver during times of no modulation

Table7-81 CWGsPReg Address：28h reset value：20h

	7	6	5	4	3	2	1	0
	0	0	CWGsP					
Access	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table7-82 Description of CWGsPReg bits

Bit	Symbol	Description
7-6	-	Reserved for future use.
5-0	CWGsP	The value of this register defines the conductance of the output P-driver. This may be used to regulate the output power and subsequently current consumption and operating distance. NOTE: The conductance value is binary weighted. NOTE: During soft Power-down mode the highest bit is forced to 1.

7.4.9 ModGsPReg

Defines the driver P-output conductance during modulation.

Table7-83 ModGsPReg Address：29h reset value：20h

	7	6	5	4	3	2	1	0
	0	0	ModGsP					
Access	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table7-84 Description of ModGsPReg bits

Bit	Symbol	Description
7-6	-	Reserved for future use.
5-0	ModGsP	The value of this register defines the conductance of the output P-driver for the time of modulation. This may be used to regulate the modulation index. NOTE: The conductance value is binary weighted. NOTE: During soft Power-down mode the highest bit is forced to 1.

7.4.10 TModeReg，TPrescalerReg

Defines settings for the timer.

NOTE: The Prescaler value is split into two 8-bit registers

Table7-85 TModeReg Address：2Ah reset value：00h

	7	6	5	4	3：0
	TAuto	TGated		TAutoRestart	TPrescaler_Hi
Access	r/w	r/w	r/w	r/w	r/w

Table7-86 Description of TModeReg bits

Bit	Symbol	Description
7	TAuto	Set to logic 1, the timer starts automatically at the end of the transmission in all communication modes at all speeds or when bit InitialRFOn is set to logic 1 and the RF field is switched on. In ISO14443-B 106kbit/s the timer stops after the 5th bit (1 startbit, 4 databits) if the bit RxMultiple in the register RxModeReg is not set. In all other modes, the timer stops after the 4th bit if the bit RxMultiple the register RxModeReg is not set. If RxMultiple is set to logic 1, the timer never stops. In this case the timer can be stopped by setting the bit TStopNow in register ControlReg to 1. Set to logic 0 indicates, that the timer is not influenced by the protocol.
6-5	TGated	The internal timer is running in gated mode. NOTE: In the gated mode, the bit TRunning is 1 when the timer is enabled by the register bits. This bit does not influence the gating signal.
		Value: 00 — Description: Non gated mode Value: 01 — Description: Gated by SIGIN Value: 10 — Description: Gated by AUX1 Value: 11 — Description: Gated by A3
4	TAutoRestart	Set to logic 1, the timer automatically restart its count-down from TReloadValue, instead of counting down to zero. Set to logic 0 the timer decrements to ZERO and the bit TimerIRq is set to logic 1.
3-0	TPrescaler_Hi	Defines higher 4 bits for TPrescaler.

		The following formula is used to calculate f_{Timer} if TPrescalEven bit in Demot Reg is set to logic 0: f_{Timer} = 13.56MHz/(2*TPreScaler + 1) Where TPreScaler = [TPrescaler_Hi: TPrescaler_Lo] (TPrescaler value on 12 bits) (Default TPrescalEven is logic 0) The following formula is used to calculate fTimer if TPrescalEven bit in Demot Reg is set to logic 1: f_{Timer} = 13.56MHz/(2*TPreScaler + 2)

Table7-87 TPrescalerReg Address：2Bh reset value：00h

	7	6	5	4	3	2	1	0
	TPrescaler_Lo							
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-88 Description of TPrescalerReg bits

Bit	Symbol	Description
7-0	TPrescaler_Lo	Defines lower 8 bits for TPrescaler. The following formula is used to calculate f_{Timer} if TPrescalEven bit in Demot Reg is set to logic 0: f_{Timer} = 13.56 MHz/(2*TPreScaler+1). Where TPreScaler = [TPrescaler_Hi: TPrescaler_Lo] (TPrescaler value on 12 bits) The following formula is used to calculate fTimer if TPrescalEven bit in Demot Reg is set to logic 1: f_{Timer} = 13.56 MHz/(2*TPreScaler+2). Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits).

7.4.11 TReloadReg

Describes the 16-bit long timer reload value.

NOTE: The Reload value is split into two 8-bit registers.

Table7-89 TReloadReg(Higher bits) Address：2Ch reset value：00h

	7	6	5	4	3	2	1	0
	TReloadVal_Hi							
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-90 Description of TReloadReg bits

Bit	Symbol	Description
7-0	TReloadVal_Hi	Defines the higher 8 bits for the TReloadReg.With a start event the timer loads the TReloadVal. Changing this register affects the timer only at the next start event.

Table7-91 TReloadReg(Lower bits) Address：2Dh reset value：00h

	7	6	5	4	3	2	1	0
	TReloadVal_Lo							
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-92 Description of TReloadReg bits

Bit	Symbol	Description
7-0	TReloadVal_Lo	Defines the lower 8 bits for the TReloadReg.With a start event the timer loads the TReloadVal. Changing this register affects the timer only at the next start event.

7.4.12 TCounterValReg

Contains the current value of the timer.

NOTE: The Counter value is split into two 8-bit register.

Table7-93 TCounterValReg（Higher bits） Address：2Eh reset value：xxh xxxxxxxxb

	7	6	5	4	3	2	1	0
	TcntVal_Hi							
Access	r	r	r	r	r	r	r	r

Table7-94 Description of TCounterValRegBit

Bit	Symbol	Description
7-0	TcntVal_Hi	Current value of the timer, higher 8 bits.

Table7-95 TCounterValReg（Lower bits） Address：2Fh reset value：xxh xxxxxxxxb

	7	6	5	4	3	2	1	0
	TcntVal_Lo							
Access	r	r	r	r	r	r	r	r

Table7-96 Description of TCounterValRegBit

Bit	Symbol	Description
7-0	TcntVal_Lo	Current value of the timer, lower 8 bits.

7.5 PAGE3：Test

7.5.1 PageReg

Table7-97 PageReg Address：30h reset value：00h

	7	6	5	4	3	2	1	0
	UsePage Select	Regbank Select	RegSelect				PageSelect	
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-98 Description of PageReg bits

Bit	Symbol	Description

7	UsePageSelect	Set to logic 1, the value of PageSelect is used as register address A5 and A4. The LSB-bits of the register address are defined by the address pins or the internal address latch, respectively. Set to logic 0, the whole content of the internal address latch defines the register address. The address pins are used as described in Automatic microcontroller interface detection
6	RegbankSelect	Set to logic 1，it is used to read/write 0Fh register set
5-2	RegSelect	0000：read/write register set A； 0001：read/write register set B； … 1111：read/write register set P
1-0	PageSelect	The value of PageSelect is used only if UsePageSelect is set to logic 1. In this case, it specifies the register page (which is A5 and A4 of the register address).

7.5.2 TestSel1Reg

General test signal configuration.

Table7-99 TestSel1Reg Address：31h reset value：00h

	7	6	5	4	3	2	1	0
	-	-	SAMClockSel		SAMClkD1	TstBusBitSel		
Access	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table7-100 Description of TestSel1Reg bits

Bit	Symbol	Description	
7-6	-	Reserved for future use.	
5-4	SAMClockSel	Defines the source for the 13.56 MHz SAM clock	
		Value	Description
		00	GND- Sam Clock switched off
		01	clock derived by the internal oscillator
		10	internal UART clock
		11	clock derived by the RF field
3	SAMClkD1	Set to logic 1, the SAM clock is delivered to D1. NOTE: Only possible if the 8bit parallel interface is not used.	

2-0	TstBusBitSel	Select the TestBus bit from the testbus to be propagated to SIGOUT.

7.5.3 TestSel2Reg

General test signal configuration and PRBS control

Table7-101 TestSel2Reg Address：32h reset value：00h

	7	6	5	4	3	2	1	0
	TstBusFlip	PRBS9	PRBS15	TstBusSel				
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-102 Description of TestSel2Reg bits

Bit	Symbol	Description
7	TstBusFlip	If set to logic 1, the testbus is mapped to the parallel port by the following order: D4，D3，D2，D6，D5，D0，D1
6	PRBS9	Starts and enables the PRBS9 sequence according ITU-TO150. NOTE: All relevant registers to transmit data have to be configured before entering PRBS9 mode. NOTE: The data transmission of the defined sequence is started by the send command.
5	PRBS15	Starts and enables the PRBS15 sequence according ITU-TO150. NOTE: All relevant registers to transmit data have to be configured before entering PRBS15 mode. NOTE: The data transmission of the defined sequence is started by the send command.
4-0	TstBusSel	Selects the testbus.

7.5.4 TestPinEnReg

Enables the pin output driver on the 8-bit parallel bus.

Table7-103 TestPinEnReg Address：33h reset value：80h

	7	6	5	4	3	2	1	0
	RS232LineEn	TestPinEn						
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-104 Description of TestPinEnReg bits

Bit	Symbol	Description
7	RS232LineEn	Set to logic 0, the lines MX and DTRQ for the serial UART are disabled.
6-0	TestPinEn	Enables the pin output driver on the 8-bit parallel interface. Example: Setting bit 0 to 1 enables D0 Setting bit 5 to 1 enables D5 NOTE: Only valid if one of serial interfaces is used. If the SPI interface is used only D0 to D4 can be used. If the serial UART interface is used and RS232LineEn is set to logic 1 only D0 to D4 can be used.

7.5.5 TestPinValueReg

Defines the values for the 7-bit parallel port when it is used as I/O.

Table7-105 TestPinValueReg Address：34h reset value：00h

	7	6	5	4	3	2	1	0
	UseIO	TestPinValue						
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-106 Description of TestPinValueReg bits

Bit	Symbol	Description
7	UseIO	Set to logic 1, this bit enables the I/O functionality for the 7-bit parallel port in case one of the serial interfaces is used. The input/output behavior is defined by TestPinEn in register TestPinEnReg. The value for the output behavior is defined in the bits TestPinVal. NOTE: If SAMClkD1 is set to logic 1, D1 can not be used as I/O.
6-0	TestPinValue	Defines the value of the 7-bit parallel port, when it is used as I/O. Each output has to be enabled by the TestPinEn bits in register TestPinEnReg. NOTE: Reading the register indicates the actual status of the pins D6 - D0 if UseIO is set to logic 1. If UseIO is set to logic 0, the value of the register TestPinValueReg is read back.

7.5.6 TestBusReg

Shows the status of the internal testbus.

Table7-107 TestBusReg Address：35h reset value：xxh，xxxxxxxxh

	7	6	5	4	3	2	1	0
	TestBus							
Access	r	r	r	r	r	r	r	r

Table7-108 Description of TestBusReg bits

Bit	Symbol	Description
7-0	TestBus	Shows the status of the internal testbus. The testbus is selected by the register TestSel2Reg.

7.5.7 AutoTestReg

Controls the digital selftest.

Table7-109 AutoTestReg Address：36h reset value：40h

	7	6	5	4	3	2	1	0
	0	AmpRcv	EOFSOF Adjust	-	SelfTest			
Access	RFT	r/w	RFU	RFU	r/w	r/w	r/w	r/w

Table7-110 Description of AutoTestReg bits

Bit	Symbol	Description
7	-	Reserved for production tests.
6	AmpRcv	If set to logic 1, the internal signal processing in the receiver chain is performed non-linear. This increases the operating distance in communication modes at 106 kbit. NOTE: Due to the non linearity the effect of the bits MinLevel and CollLevel in the register RxThreshholdReg are as well non linear.
5	EOFSOFAdjust	If set to logic 0 and the EOFSOFwidth is set to 1 will result in the Maximum length of SOF and EOF according to ISO/IEC14443B.

		If set to logic 0 and the EOFSOFwidth is set to 0 will result in the Minimum length of SOF and EOF according to ISO/IEC14443B. If this bit is set to 1 and the EOFSOFwidth bit is logic 1 will result in SOF low = (11 etu − 8 cycles)/fc SOF high = (2 etu + 8 cycles)/fc EOF low = (11 etu − 8 cycles)/fc
4	-	Reserved for future use.
3-0	SelfTest	Enables the digital self test. The selftest can be started by the selftest command in the command register. The selftest is enabled by 1001. NOTE: For default operation the selftest has to be disabled by 0000.

7.5.8 VersionReg

Shows the version.

Table7-111 VersionReg Address：37h reset value：xxh，xxxxxxxxb

	7	6	5	4	3	2	1	0
	Version							
Access	r	r	r	r	r	r	r	r

Table7-112 Description of VersionReg bit

Bit	Symbol	Description
7-0	Version	82h

7.5.9 AnalogTestReg

Controls the pins AUX1 and AUX2.

Table7-113 AnalogTestReg Address：38h reset value：00h

	7	6	5	4	3	2	1	0
	AnalogSelAux1				AnalogSelAux2			
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table7-114 Description of AnalogTestReg bits

Bit	Symbol	Description

7-4 3-0	AnalogSelAux1 AnalogSelAux2	Controls the AUX pin	
		Value	Description
		0000	Tristate
		0001	Output of TestDAC1 (AUX1), output of TestDAC2 (AUX2) NOTE: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0010	Testsignal Corr1 NOTE: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0011	Testsignal Corr2 NOTE: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0100	Testsignal MinLevel NOTE: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0101	Testsignal ADC channel I NOTE: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0110	Testsignal ADC channel Q NOTE: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		0111	Testsignal ADC channel I combined with Q NOTE: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		1000	Testsignal for production test NOTE: Current output. The use of 1 kΩ pull-down resistor on AUX is recommended.
		1001	SAM clock (13.56 MHz)
		1010	HIGH
		1011	LOW
		1100	TxActive At 106 kbit: HIGH during Startbit, Data bit, Parity and CRC. At 212 and 424 kbit: High during Preamble, Sync, Data and CRC.
		1101	RxActive

			At 106 kbit: High during databit, Parity and CRC. At 212 and 424 kbit: High during data and CRC.
		1110	Subcarrier detected 106 kbit: not applicable 212 and 424 kbit: High during last part of Preamble, Sync data and
		1111	CRC
			TestBus-Bit as defined by the TstBusBitSel in register TestSel1Reg.

7.5.10 TestDAC1Reg

Defines the testvalues for TestDAC1.

Table7-115 TestDAC1Reg Address：39h reset value：xxh，00xxxxxxb

	7	6	5	4	3	2	1	0
	0	0	TestDAC1					
Access	RFT	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table7-116 Description of TestDAC1Reg bits

Bit	Symbol	Description
7	-	Reserved for production tests.
6	-	Reserved for future use.
5-0	TestDAC1	Defines the testvalue for TestDAC1. The output of the DAC1 can be switched to AUX1 by setting AnalogSelAux1 to 0001 in register AnalogTestReg.

7.5.11 TestDAC2Reg

Defines the testvalue for TestDAC2.

Table7-116 TestDAC2Reg Address：3Ah reset value：xxh，00xxxxxxb

	7	6	5	4	3	2	1	0
	0	0	TestDAC2					
Access	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table7-117 Description of TestDAC2Reg bits

Bit	Symbol	Description
7-6	-	Reserved for future use.
5-0	TestDAC2	Defines the testvalue for TestDAC2. The output of the DAC2 can be switched to AUX2 by setting AnalogSelAux2 to 0001 in register AnalogTestReg.

7.5.12 TestADCReg

Shows the actual value of ADC I and Q channel.

Table7-118 TestADCReg Address：3Bh reset value：xxh，xxxxxxxxb

	7	6	5	4	3	2	1	0
	ADC_I				ADC_Q			
Access	r	r	r	r	r	r	r	r

Table7-119 Description of TestADCReg bits

Bit	Symbol	Description
7-4	ADC_I	Shows the actual value of ADC I channel.
3-0	ADC_Q	Shows the actual value of ADC Q channel.

7.5.13 RFTReg

Table7-120 RFTReg Address：3Ch reset value：FFh

	7	6	5	4	3	2	1	0
	1	1	1	1	1	1	1	1
Access	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT

Table7-121 Description of RFTReg bits

Bit	Symbol	Description
7-0	-	Reserved for production tests.

Table7-122 RFTReg Address：3D reset value：00h

	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0
Access	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT

Table7-123 Description of RFTReg bits

Bit	Symbol	Description
7-0	-	Reserved for production tests.

Table7-124 RFTReg Address：3Eh reset value：03h

	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	1	1
Access	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT

Table7-125 Description of RFTReg bits

Bit	Symbol	Description
7:0		RFT

7.5.14 PollLPReg

Manual configuration further reduces power consumption in ACD mode

Table7-126 PollLPReg Address：3Fh reset value：03h

	7	6	5	4	3	2	1	0

	0	0	0	PollLPEn	0	0	1	1
Access	RFT	RFT	RFT	r/w	RFT	RFT	RFT	RFT

Table7-127 Description of PollLPReg bits

Bit	Symbol	Description
7:5	-	RFT
4	PollLPEn	When set to 1, reduce the power consumption of ACD mode further
3:2	-	RFT
1		VMID switch 1：off 0：on
0	-	RFT

8 Digital interfaces

8.1 Automatic microcontroller interface detection

The Si512 supports direct interfacing of hosts using SPI, I2C-bus or serial UART interfaces. The Si512 resets its interface and checks the current host interface type automatically after performing a power-on or hard reset. The Si512 identifies the host interface by sensing the logic levels on the control pins after the reset phase. This is done using a combination of fixed pin connections. Table 8-1 shows the different connection configurations.

Table 8-1 Connection protocol for detecting different interface types

Pin	Interface type		
	UART（input）	SPI（output）	I2C（input/output）
SDA	RX	NSS	SDA
I2C	0	0	1
EA	0	1	EA
D7	TX	MISO	SCL
D6	MX	MOSI	ADR_0
D5	DTRQ	SCK	ADR_1
D4	-	-	ADR_2
D3	-	-	ADR_3
D2	-	-	ADR_4
D1	-	-	ADR_5

8.2 SPI

A serial peripheral interface (SPI compatible) is supported to enable high-speed communication to the host. The interface can handle data speeds up to 10 Mbit/s. When communicating with a host, the Si512 acts as a slave, receiving data from the external host for register settings, sending and receiving data relevant for RF interface communication.

An interface compatible with SPI enables high-speed serial communication between the Si512 and a microcontroller. The implemented interface is in accordance

with the SPI standard.

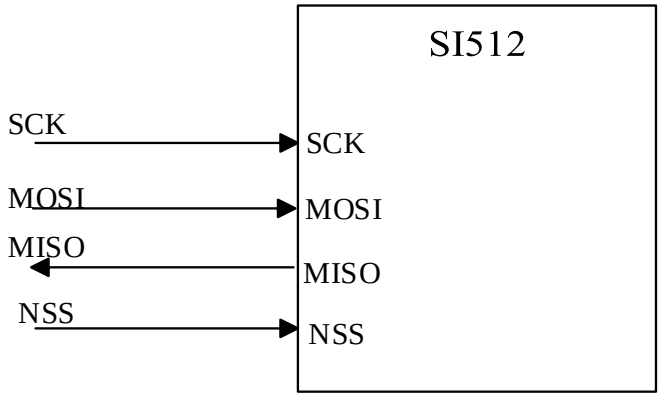


Figure 8.1 SPI connection to host

The Si512 acts as a slave during SPI communication. The SPI clock signal SCK must be generated by the master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the Si512 to the master. Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge.

8.2.1 SPI read data

Reading data using SPI requires the byte order shown in Table 8-2 to be used. It is important that the MSbit is sent first. The first byte sent defines both the mode and the address.

Table8-2 MOSI and MISO byte order

Line	Byte0	Byte1	Byte2	…	Byten	Byten+1
MOSI	Address0	Address1	Address2	…	Addressn	00
MISO	X*	data0	data1	…	datan-1	datan

NOTE: X = Do not care. The MSB must be sent first.

8.2.2 SPI write data

To write data to the Si512 using SPI requires the byte order shown in Table 8-3. The first send byte defines both the mode and the address byte.

Table 8-3 MOSI and MISOByte order

Line	Byte0	Byte1	Byte2	…	Byten	Byten+1
MOSI	Address0	data0	data1	…	datan-1	datan
MISO	X*	X*	X*	…	X*	X*

NOTE: X = Do not care. The MSB must be sent first.

8.2.3 SPI address byte

The address byte has to meet the following format.

Table 8-4 Address byte0 register; address MOSI

7（MSB）	6：1	0（LSB）
1=read/0=write	Address	0

The MSB of the first byte defines the mode used. To read data from the Si512 the MSB is set to logic 1. To write data to the Si512 the MSB must be set to logic 0. Bits 6 to 1 define the address and the LSB is set to logic 0.

8.3 UART

8.3.1 Connection to a host

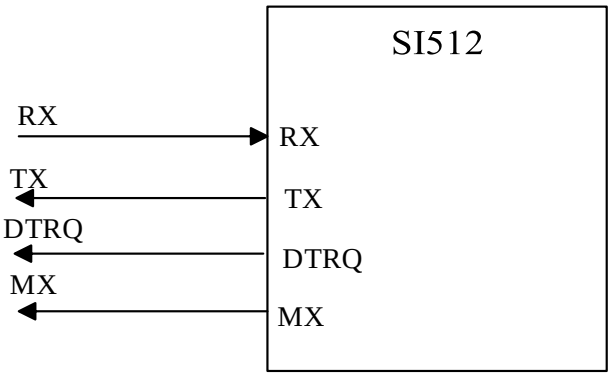


Figure 8.2 UART connection to microcontrollers

NOTE: Signals DTRQ and MX can be disabled by clearing TestPinEnReg register's RS232LineEn bit.

8.3.2 Selectable UART transfer speeds

The internal UART interface is compatible with an RS232 serial interface.

The default transfer speed is 8.6kBd. To change the transfer speed, the host controller must write a value for the new transfer speed to the SerialSpeedReg register. Bits BR_T0[2:0] and BR_T1[4:0] define the factors for setting the transfer speed in the SerialSpeedReg register. The BR_T0[2:0] and BR_T1[4:0] settings are described in Table 8-5.

Table 8-5 BR_T0 and BR_T1 settings

BR_Tn	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
BR_T0	1	1	2	4	8	16	32	64
BR_T1	1-32	33-64	33-64	33-64	33-64	33-64	33-64	33-64

Examples of different transfer speeds and the relevant register settings are given in Table 8-6.

Table 8-6 Selectable UART transfer speeds

Transfer speed（kBd）	SeriaSpeedReg value		Transfer speed accuracy（%）*
	Decimal	Hexadecimal	
7.2	250	FAh	-0.25
8.6	235	EBh	0.32
14.4	218	DAh	-0.25
19.2	203	CBh	0.32
38.4	171	ABh	0.32
57.6	154	9Ah	-0.25
115.2	122	7Ah	-0.25
128	116	74h	-0.06
230.4	90	5Ah	-0.25
460.8	58	3Ah	-0.25
921.6	28	1Ch	1.45
1228.8	21	15h	0.32

NOTE：The resulting transfer speed error is less than 1.5 % for all described transfer speeds

The selectable transfer speeds shown in Table 8-6 are calculated according to the following equations:

If BR_T0[2:0]=0：

$$\text{transfer speed} = \frac{27.12 \times 10^6}{BR_{T0} + 1}$$

If BR_T0[2:0]＞0：

$$\text{transfer speed} = \frac{27.12 \times 10^6}{\frac{(BR\_T1 + 33)}{2^{BR_{T0}-1}}}$$

8.3.3 UART framing

Table8-7 UART framing

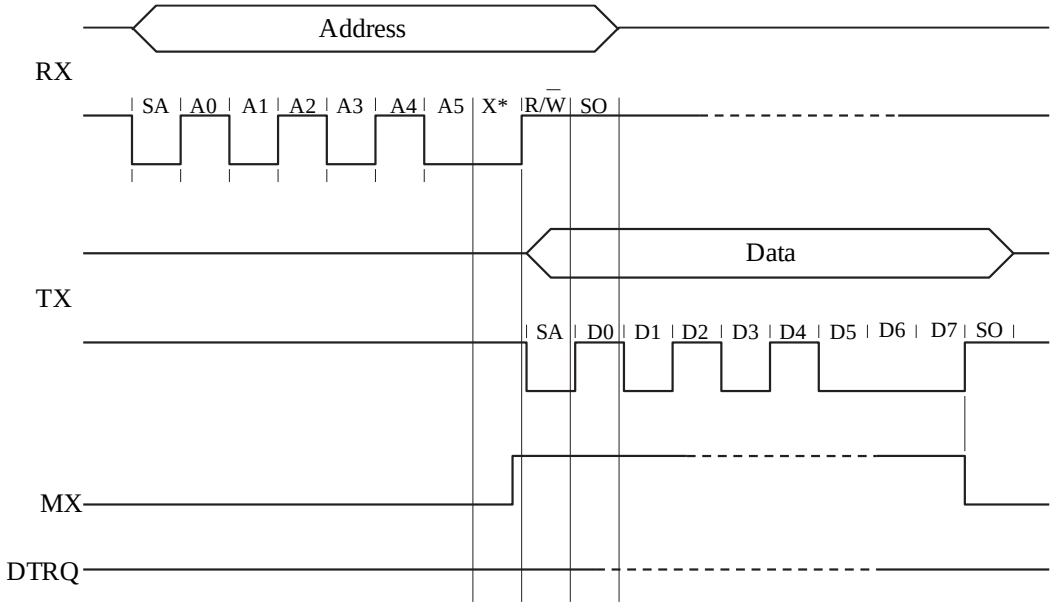
Bit	Length	Value
Start	1bit	0
Data	8bits	data
Stop	1bit	1

NOTE: The LSB for data and address bytes must be sent first. No parity bit is used during transmission.

To read data using the UART interface, the flow shown in Table 8-8 must be used. The first byte sent defines both the mode and the address.

Table8-8 Read data byte order

Pin	Byte 0	Byte 1
RX	address	-
TX	-	Data 0



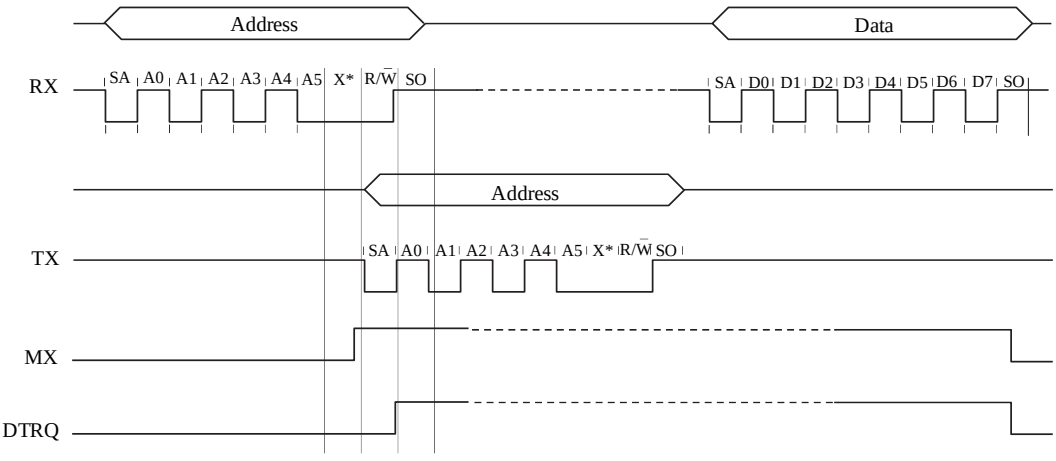
X*：Reserved value

Figure 8.3 UART read data timing diagram

To write data to the Si512 using the UART interface, the structure shown in Table 8-9 must be used. The first byte sent defines both the mode and the address.

Table 8-9 Write data byte order

Pin	Byte0	Byte1
RX	Address0	data0
TX	-	Address0



X*：Reserved Value

Figure 8.4 UART write data timing diagram

NOTE: The data byte can be sent directly after the address byte on pin RX.

The address byte has to meet the following format:

The MSB of the first byte sets the mode used. To read data from the Si512, the MSB is set to logic 1. To write data to the Si512 the MSB is set to logic 0. Bit 6 is reserved for future use, and bits 5 to 0 define the address.

Table8-10 Address byte0 register ； MOSI

7（MSB）	6	5：1	0（LSB）
1=read/0= write	reserved	address	

8.4 I2C

An I2C-bus (Inter-IC) interface is supported to enable a low-cost, low pin count serial bus interface to the host. The I2C-bus interface is implemented according to I2C-bus interface specification, rev. 2.1, January 2000. The interface can only act in Slave mode. Therefore the Si512 does not implement clock generation or access arbitration.

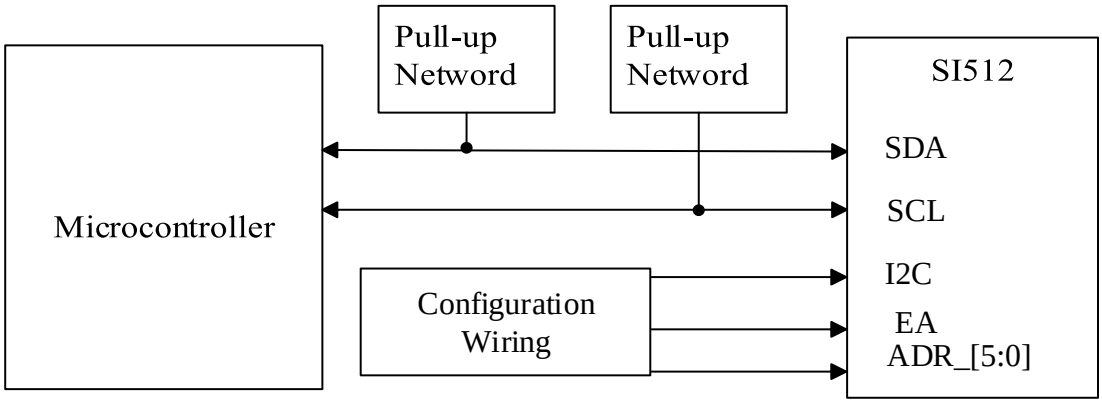


Figure 8.5 I2C-bus interface

The Si512 can act either as a slave receiver or slave transmitter in Standard mode, Fast mode and High-speed mode.

SDA is a bidirectional line connected to a positive supply voltage using a current source or a pull-up resistor. Both SDA and SCL lines are set HIGH when data is not transmitted. The Si512 has a 3-state output stage to perform the wired-AND function. Data on the I2C-bus can be transferred at data rates of up to 100kBd in Standard mode, up to 400kBd in Fast mode or up to 3.4 Mbit/s in High-speed mode.

If the I2C-bus interface is selected, spike suppression is activated on lines SCL and SDA as defined in the I2C-bus interface specification.

8.4.1 Data validity

Data on the SDA line must be stable during the HIGH clock period. The HIGH or LOW state of the data line must only change when the clock signal on SCL is LOW.

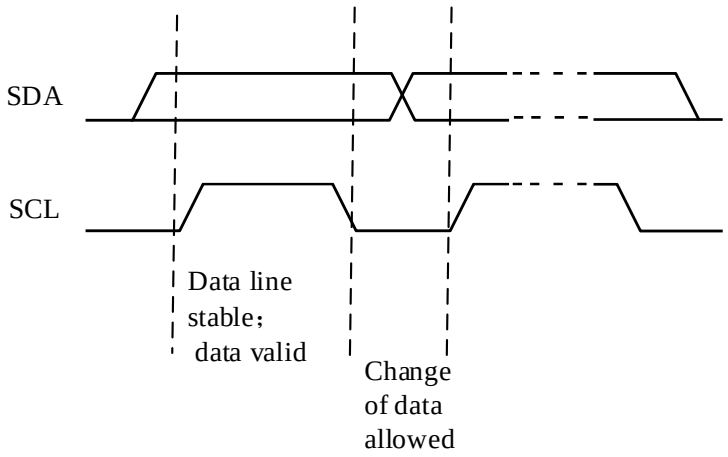


Figure 8.6 Bit transfer on the I2C-bus

8.4.2 START and STOP conditions

To manage the data transfer on the I2C-bus, unique START (S) and STOP (P) conditions are defined.

• A START condition is defined with a HIGH-to-LOW transition on the SDA line while SCL is HIGH.

• A STOP condition is defined with a LOW-to-HIGH transition on the SDA line while SCL is HIGH.

The I2C-bus master always generates the START and STOP conditions. The bus is busy after the START condition. The bus is free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition.

The START (S) and repeated START (Sr) conditions are functionally identical. Therefore, S is used as a generic term to represent both the START (S) and repeated START (Sr) conditions.

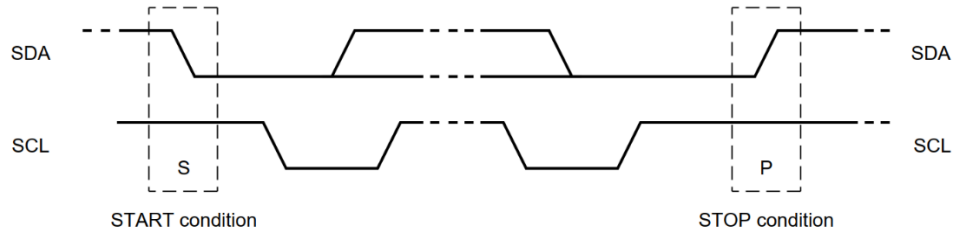


Figure 8.7 START and STOP conditions

8.4.3 Byte format

Each byte must be followed by an acknowledge bit. Data is transferred with the MSB first; see Figure 8.10. The number of transmitted bytes during one data transfer is unrestricted but must meet the read/write cycle format.

8.4.4 Acknowledge

An acknowledge must be sent at the end of one data byte. The acknowledge-related clock pulse is generated by the master. The transmitter of data, either master or slave, releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver pulls down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

The master can then generate either a STOP (P) condition to stop the transfer or a repeated START (Sr) condition to start a new transfer.

A master-receiver indicates the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out by the slave. The slave-transmitter releases the data line to allow the master to generate a STOP (P) or repeated START (Sr) condition.

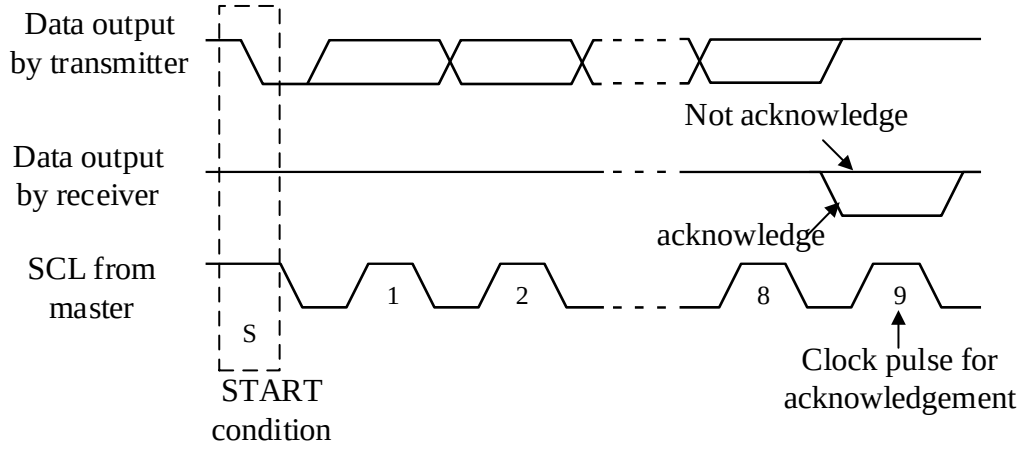


Figure 8.8 Acknowledge on the I2C-bus

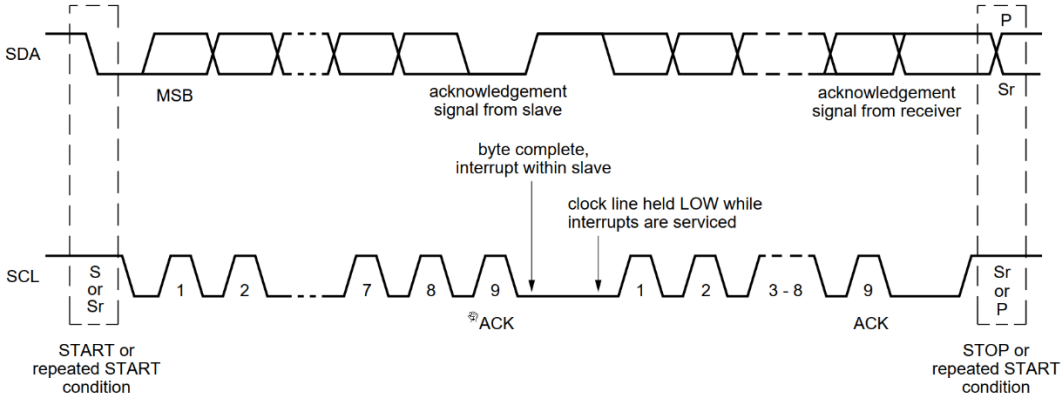


Figure 8.9 Data transfer on the I2C-bus

8.4.5 7-Bit addressing

During the I2C-bus address procedure, the first byte after the START condition is used to determine which slave will be selected by the master.

Several address numbers are reserved. During device configuration, the designer must ensure that collisions with these reserved addresses cannot occur. Check the I^2C-bus specification for a complete list of reserved addresses.

The I2C-bus address specification is dependent on the definition of pin EA. Immediately after releasing pin NRSTPD or after a power-on reset, the device defines the I2C-bus address according to pin EA.If pin EA is set LOW, the upper 4 bits of the device bus address are set to 0101b. The remaining 3 bits (ADR_0, ADR_1, ADR_2) of the slave address can be freely configured by the customer to prevent collisions with

other I2C-bus devices.If pin EA is set HIGH, ADR_0 to ADR_5 can be completely specified at the external pins and ADR_6 is always set to logic 0.

In both modes, the external address coding is latched immediately after releasing the reset condition. Further changes at the used pins are not taken into consideration. Depending on the external wiring, the I2C-bus address pins can be used for test signal outputs.

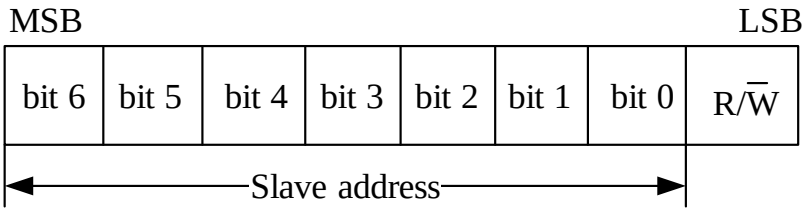


Figure 8.10 First byte following the START procedure

8.4.6 Register write access

To write data from the host controller using the I2C-bus to a specific register in the Si512 the following frame format must be used.

• The first byte of a frame indicates the device address according to the I2C-bus rules.

• The second byte indicates the register address followed by up to n-data bytes.

In one frame all data bytes are written to the same register address. This enables fast FIFO buffer access. The Read/Write (R/$\overline{W}$) bit is set to logic 0.

8.4.7 Register read access

To read out data from a specific register address in the Si512, the host controller must use the following procedure:

- Firstly, a write access to the specific register address must be performed as indicated in the frame that follows
- The first byte of a frame indicates the device address according to the I2C-bus rules
- The second byte indicates the register address. No data bytes are added
- The Read/Write bit is 0

After the write access, read access can start. The host sends the device address of

the Si512. In response, the Si512 sends the content of the read access register. In one frame all data bytes can be read from the same register address. This enables fast FIFO buffer access or register polling.

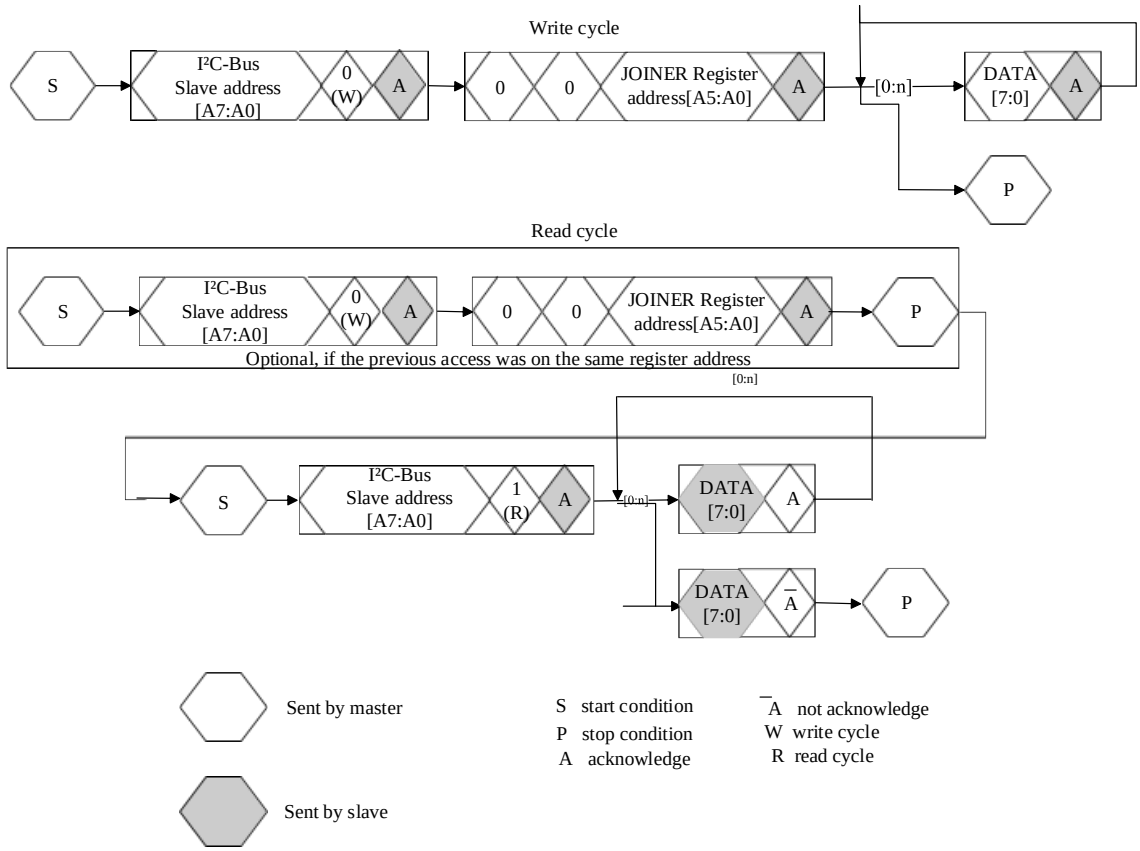


Figure 8.11 Register read and write access

8.4.8 High-speed mode

In High-speed mode (HS mode), the device can transfer information at data rates of up to 3.4 Mbit/s, while remaining fully downward-compatible with Fast or Standard mode (F/S mode) for bidirectional communication in a mixed-speed bus system.

8.4.9 High-speed transfer

To achieve data rates of up to 3.4 Mbit/s the following improvements have been made to I^2C-bus operation.

- The inputs of the device in HS mode incorporate spike suppression, a Schmitt trigger on the SDA and SCL inputs and different timing constants when compared to F/S mode
- The output buffers of the device in HS mode incorporate slope control of the falling edges of the SDA and SCL signals with different fall times compared to F/S mode

8.4.10 Serial data transfer format in HS mode

The HS mode serial data transfer format meets the Standard mode I2C-bus specification:

(1) START condition (S)

(2) 8-bit master code (00001xxxb)

(3) Not-acknowledge bit ($\overline{A}$)

When HS mode starts, the active master sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/W bit address and receives an acknowledge bit (A) from the selected Si512.

Data transfer continues in HS mode after the next repeated START (Sr), only switching back to F/S mode after a STOP condition (P). To reduce the overhead of the master code, a master links a number of HS mode transfers, separated by repeated START conditions (Sr).

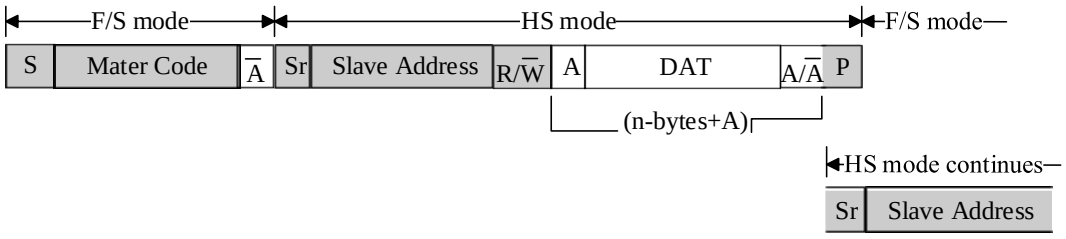


Figure 8.12 I2C-bus HS mode protocol switch

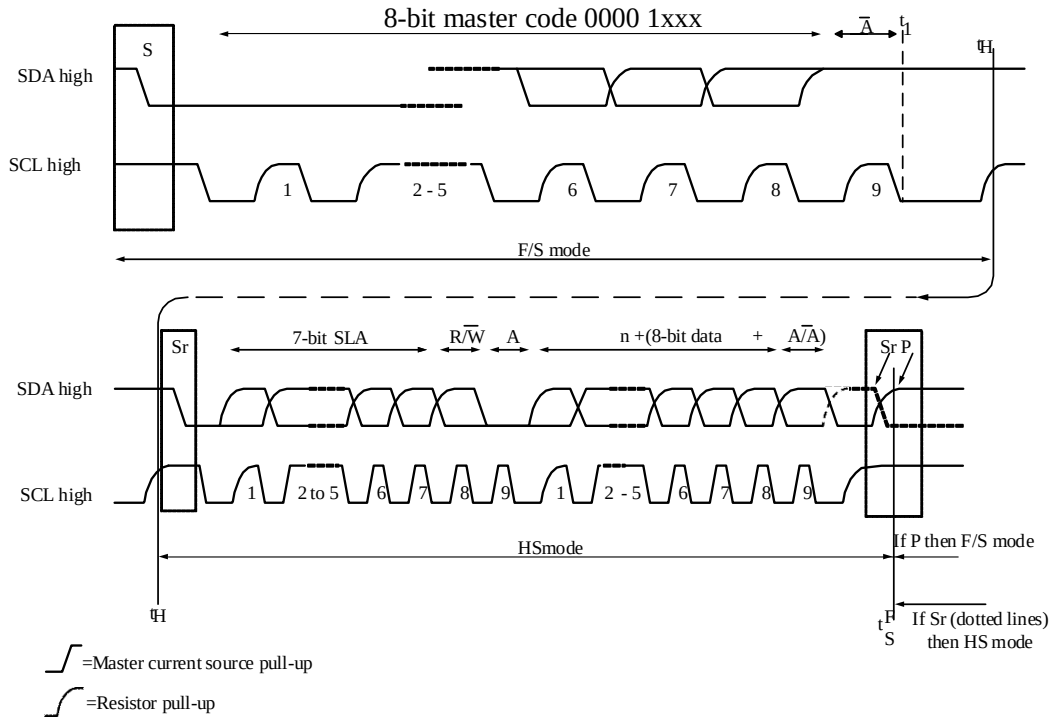


Figure 8.13 I2C-bus HS mode protocol frame

8.4.11 Switching between F/S mode and HS mode

After reset and initialization, the Si512 is in Fast mode (which is in effect F/S mode as Fast mode is downward-compatible with Standard mode). The connected Si512 recognizes the “S 00001XXX A” sequence and switches its internal circuitry from the Fast mode setting to the HS mode setting.

The following actions are taken:

(1) Adapt the SDA and SCL input filters according to the spike suppression requirement in HS mode.

(2) Adapt the slope control of the SDA output stages.

It is possible for system configurations that do not have other I2C-bus devices involved in the communication to switch to HS mode permanently. This is implemented by setting Status2Reg register’s I2CForceHS bit to logic 1. In permanent HS mode, the master code is not required to be sent. This is not defined in the specification and must only be used when no other devices are connected on the bus. In addition, spikes on the I2C-bus lines must be avoided because of the reduced spike suppression.

8.4.12 Si512 at lower speed modes

Si512 is fully downward-compatible and can be connected to an F/S mode I2C-bus system. The device stays in F/S mode and communicates at F/S mode speeds because a master code is not transmitted in this configuration.

9 8-bit parallel interface

The Si512 supports two different types of 8-bit parallel interfaces, Intel and Motorola compatible modes.

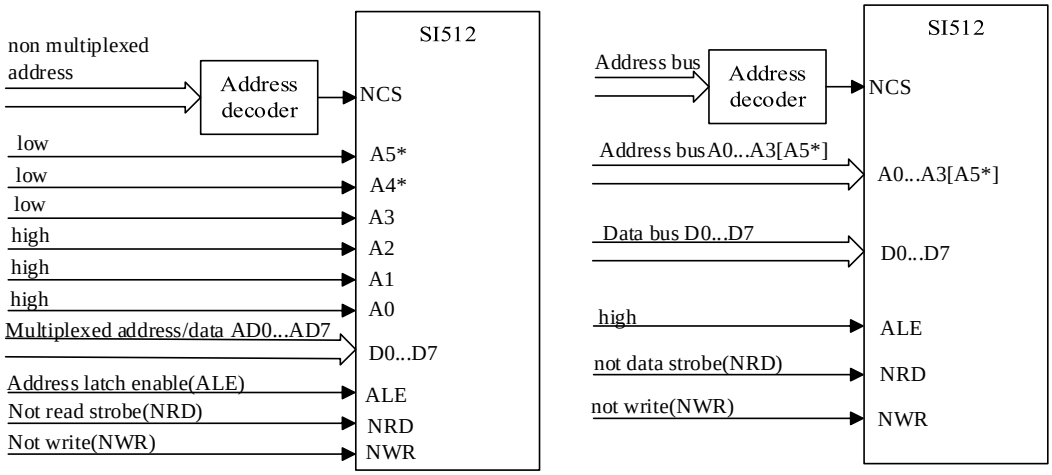
9.1 Overview of supported host controller interfaces

The Si512 supports direct interfacing to various µ-Controllers. The following table shows the parallel interface types supported by the Si512.

Table 9-1 Supported interface types

Supported interface types	Bus	Separated Address and Data Bus	Multiplexed Address and Data Bus
Separated Read and Write Strobes(INTEL compatible)	control	NRD，NWR，NCS	NRD，NWR，NCS，ALE
	Address	A0...A3[..A5*]	AD0...AD7
	data	D0...D7	AD0...AD7
Multiplexed Read and Write Strobe (Motorola compatible)	control	R/NW，NDS，NCS	R/NW，NDS，NCS，AS
	Address	A0...A3[..A5*]	AD0...AD7
	data	D0...D7	AD0...AD7

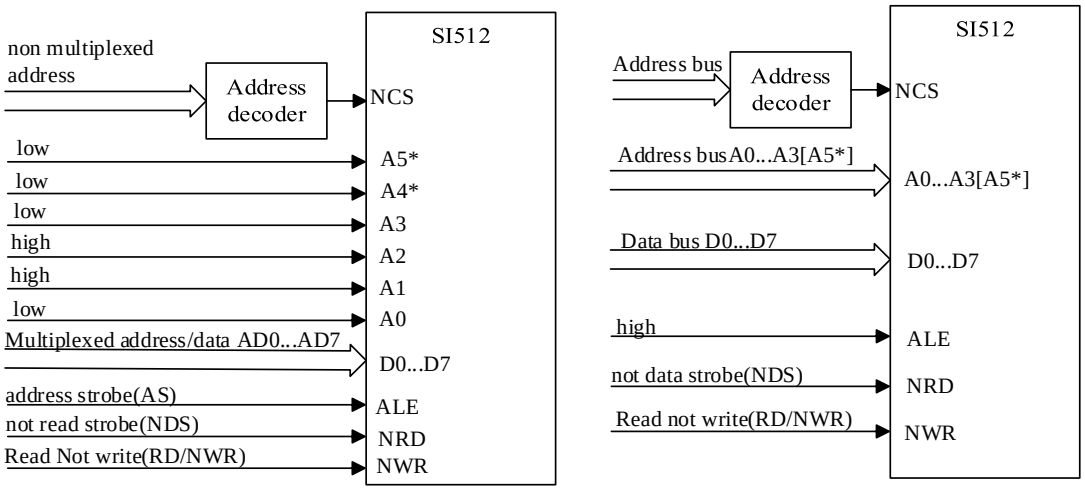
9.2 Separated Read/Write strobe



Note：*depending on the package type

Figure 9.1 Connection to host controller with separated Read/Write strobes

9.3 Common Read/Write strobe



Note：*depending on the package type

Figure 9.2 Connection to host controller with common Read/Write strobes

10 UART analog interface and contactless UART

10.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 848 kBd. An external circuit can be connected to the communication interface pins MFIN and MFOUT to modulate and demodulate the data.

The contactless UART handles the protocol requirements for the communication protocols in cooperation with the host. Protocol handling generates bit and byte-oriented framing. In addition, it handles error detection such as parity and CRC, based on the various supported contactless communication protocols.

NOTE: The size and tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

10.2 TX driver

The signal on pins TX1 and TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly using a few passive components for matching and filtering. The signal on pins TX1 and TX2 can be configured using the TxControlReg register.

The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured using registers CWGsPReg and ModGsPReg. The impedance of the n-driver can be configured using the GsNReg register. The modulation index also depends on the antenna design and tuning.

The TxModeReg and TxSelReg registers control the data rate and framing during transmission and the antenna driver setting to support the different requirements at the different modes and transfer speeds.

Table 10-1 Register and bit settings controlling the signal on pin TX1

Bit Tx1RFEn	Bit Force 100ASK	Bit InvTx1RFOn	Bit InvTx1RFOff	Envelope	Pin TX1	GSPMos	GSNMos	NOTEs
0	X*	X*	X*	X*	X*	CWGsNOff	CWGsNOff	RF is switched off
1	0	0	X*	0	RF	pMod	nMod	100 % ASK: pin TX1 pulled to logic 0, independent of the InvTx1RFOff bit
				1	RF	pCW	nCW	
	0	1	X*	0	RF	pMod	nMod	
				1	RF	pCW	nCW	
	1	1	X*	0	0	pMod	nMod	
				1	RF_n	pCW	nCW	

X = Do not care*

Table 10-2 Register and bit settings controlling the signal on pin TX2

Bit Tx1RFEn	Bit Force 100ASK	Bit Tx2CW	Bit InvTx2RFOn	Bit InvTx2RFOff	Envelope	Pin TX2	GSPMos	GSNMos	NOTEs
0	X*	X*	X*	X*	X*	X*	CWGsNOff	CWGsNOff	RF is switched off
1	0	0	0	X*	0	RF	pMod	nMod	-
					1	RF	pCW	nCW	
			1	X*	0	RF_n	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X*	X*	RF	pCW	nCW	conductance always CW for the Tx2CW bit
			1	X*	X*	RF_n	pCW	nCW	
	1	0	0	X*	0	0	pMod	nMod	100 % ASK: pin TX2 pulled to logic 0(independent of theInvTx2RFOn/ InvTx2RFOff bits)
					1	RF	pCW	nCW	
			1	X*	0	0	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X*	X*	RF	pCW	nCW	
			1	X*	X*	RF_n	pCW	nCW	

X = Do not care*

The following abbreviations have been used in Table 10-1 and Table 10-2:

(1) RF: 13.56 MHz clock derived from 27.12 MHz quartz crystal oscillator divided by 2

(2) RF_n: inverted 13.56 MHz clock

(3) GSPMos: conductance, configuration of the PMOS array

(4) GSNMos: conductance, configuration of the NMOS array

(5) pCW: PMOS conductance value for continuous wave defined by the CWGsPReg register

(6) pMod: PMOS conductance value for modulation defined by the ModGsPReg register

(7) nCW: NMOS conductance value for continuous wave defined by the GsNReg register's CWGsN[3:0] bits

(8) nMod: NMOS conductance value for modulation defined by the GsNReg register's ModGsN[3:0] bits

(9) X = do not care.

NOTE: If only one driver is switched on, the values for CWGsPReg, ModGsPReg and GsNReg registers are used for both drivers

10.3 RF level detector

The RF level detector is integrated to fulfill NFCIP1 protocol requirements (e.g. RF collision avoidance). Furthermore the RF level detector can be used to wake up the Si512 and to generate an interrupt.

The sensitivity of the RF level detector is adjustable in a 4-bit range using the bits RFLevel in register RFCfgReg. The sensitivity itself depends on the antenna configuration and tuning.

Possible sensitivity levels at the RX pin are listed in the follow table.

Table 10-3 Setting of the bits RFlevel in register RFCfgReg (RFLevel amplifier deactivated)

V~RX[Vpp]	RFLevel
~2	1111
~1.4	1110
~0.99	1101
~0.69	1100
~0.49	1011

~0.35	1010
~0.24	1001
~0.17	1000
~0.12	0111
~0.083	0110
~0.058	0101
~0.041	0100
~0.029	0011
~0.020	0010
~0.014	0001
~0.010	0000

To increase the sensitivity of the RF level detector an amplifier can be activated by setting the bit RFLevelAmp in register RFCfgReg to 1.

NOTE: During soft Power-down mode the RF level detector amplifier is automatically switched off to meet low power consumption demand. With typical antennas lower sensitivity levels can provoke misleading results because of intrinsic noise in the environment. It is recommended to use the bit RFLevelAmp only with higher RF level settings.

10.4 Data mode detector

The Data mode detector gives the possibility to detect received signals according to the ISO/IEC 14443A, FeliCa or NFCIP-1 schemes at the standard transfer speeds for 106 kbit, 212 kbit and 424 kbit in order to prepare the internal receiver in a fast and convenient way for further data processing.

The Data mode detector can only be activated by the AutoColl command. The mode detector resets, when no external RF field is detected by the RF level detector. The Data mode detector could be switched off during the AutoColl command by setting bit ModeDetOff in register ModeReg to 1.

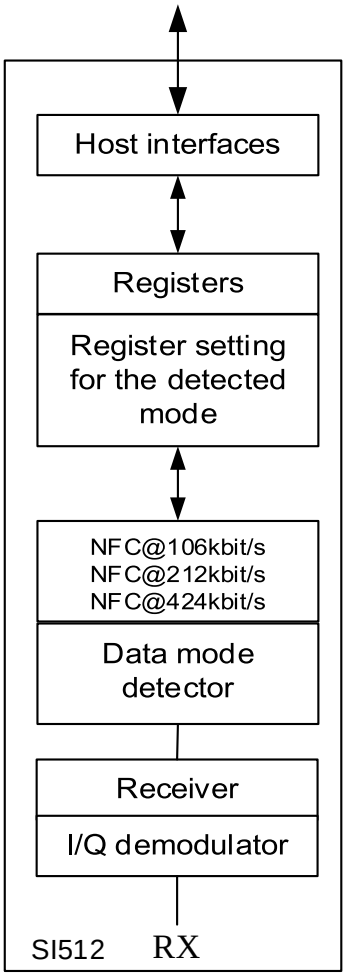


Figure 10.1 Data mode detector

10.5 Serial data switch

Two main blocks are implemented in the Si512. The digital block comprises the state machines, encoder/decoder logic. The analog block comprises the modulator and antenna drivers, the receiver and amplifiers. The interface between these two blocks can be configured in the way, that the interfacing signals may be routed to the pins MFIN and MFOUT. MFIN is capable of processing digital NFC signals on transfer speeds above 424 kbit. The MFOUT pin can provide a digital signal that can be used with an additional external circuit to generate transfer speeds above 424 kbit (including 106, 212 and 424 kbit). Furthermore, MFOUT and MFIN can be used to enable the S^2C interface in the card SAM mode to emulate a card functionality with the Si512 and a secure IC.

This topology allows the analog block of the Si512 to be connected to the digital block of another device.

The serial signal switch is controlled by the TxSelReg and RxSelReg registers.

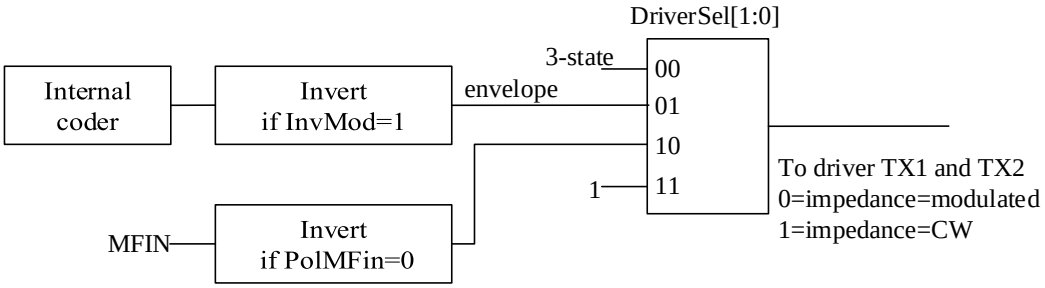


Figure 10.2 Serial data switch for TX1 and TX2

10.6 S²C interface support

The S²C provides the possibility to directly connect a secure IC to the Si512 in order act as a contactless smart card IC via the Si512. The interfacing signals can be routed to the pins MFIN and MFOUT. MFIN can receive either a digital FeliCa or digitized ISO/IEC 14443A signal sent by the secure IC. The MFOUT pin can provide a digital signal and a clock to communicate to the secure IC.

The Si512 has an extra supply pin (SVDD and PVSS as Ground line) for the MFIN and MFOUT pads. Figure 10.3 outlines possible ways of communications via the Si512 to the secure IC.

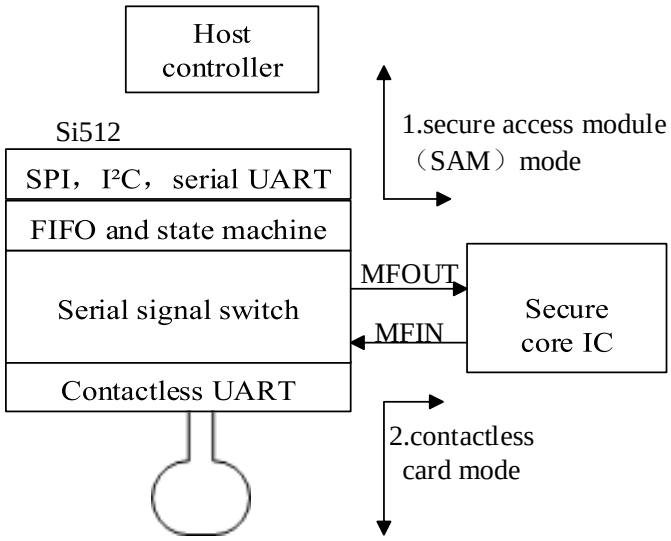


Figure 10.3 Communication flows using the S²C interface

Configured in the Secure Access Mode the host controller can directly

communicate to the Secure IC via MFIN/MFOUT. In this mode the Si512 generates the RF clock and performs the communication on the MFOUT line. To enable the Secure Access module mode the clock has to be derived by the internal oscillator of the Si512, see bits SAMClockSel in register TestSel1Reg.

Configured in Contactless Card mode the secure IC can act as contactless smart card IC via the Si512. In this mode the signal on the MFOUT line is provided by the external RF field of the external reader/writer. To enable the Contactless Card mode the clock derived by the external RF field has to be used.

The configuration of the S^2C interface differs for the FeliCa scheme as outlined in the following chapters.

10.6.1 Signal shape for Felica S^2C interface support

The FeliCa secure IC is connected to the Si512 via the pins MFOUT and MFIN.

The signal at MFOUT contains the information of the 13.56 MHz clock and the digitized demodulated signal. The clock and the demodulated signal is combined by using the logical function exclusive or.

To ensure that this signal is free of spikes, the demodulated signal is digitally filtered first. The time delay for that digital filtering is in the range of one bit length. The demodulated signal changes only at a positive edge of the clock.

The register TxSelReg controls the setting at MFOUT

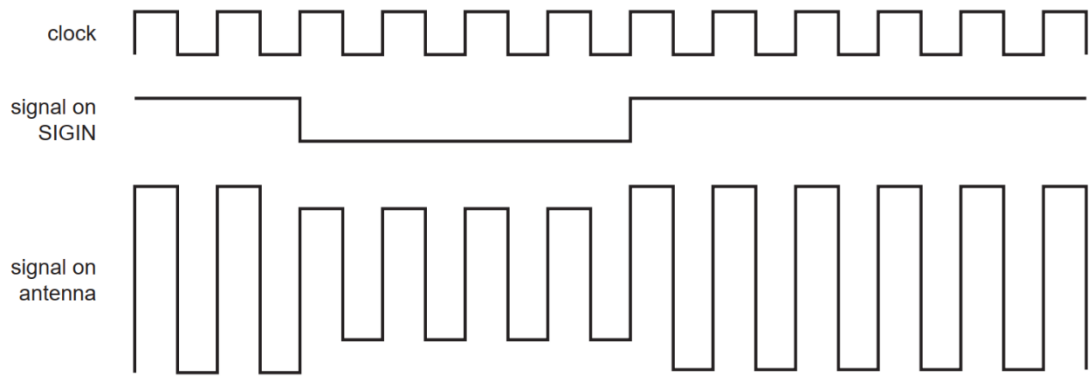


Figure 10.4 Signal shape for MFOUT in FeliCa card SAM mode

The answer of the FeliCa SAM is transferred from MFIN directly to the antenna driver. The modulation is done according to the register settings of the antenna drivers.

The clock is switched to AUX1 or AUX2 (see AnalogSelAux).

NOTE: A HIGH signal on AUX1 and AUX2 has the same level as AVDD. A HIGH signal at MFOUT has the same level as SVDD. Alternatively it is possible to use pin D0 as clock output if a serial interface is used. The HIGH level at D0 is the same as PVDD.

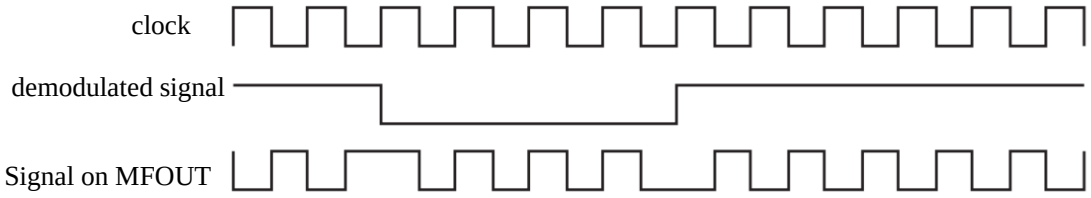


Figure 10.5 Signal shape for MFIN in SAM mode

NOTE: The signal on the antenna is shown in principle only. In reality the waveform is sinusoidal.

10.6.2 Waveform shape for ISO/IEC 14443A S²C support

The secure IC, e.g. the SmartMX is connected to the Si512 via the pins MFOUT and MFIN.

The waveform shape at MFOUT is a digital 13.56 MHz Miller coded signal with levels between PVSS and PVDD derived out of the external 13.56 MHz carrier signal in case of the Contactless Card mode or internally generated in terms of Secure Access mode.

The register TxSelReg controls the setting at MFOUT.

NOTE: The clock settings for the Secure Access mode and the Contactless Card mode differ, refer to the description of the bits SAMClockSel in register TestSel1Reg.

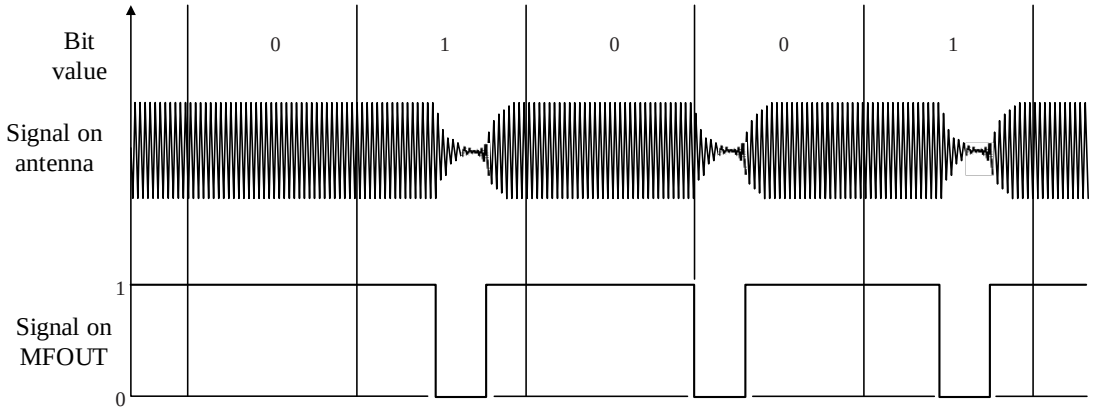


Figure 10.6 Signal shape for MFOUT in SAM mode

The signal at MFIN is a digital Manchester coded signal according to the requirements of the ISO/IEC 14443A with the subcarrier frequency of 847.5 kHz generated by the secure IC.

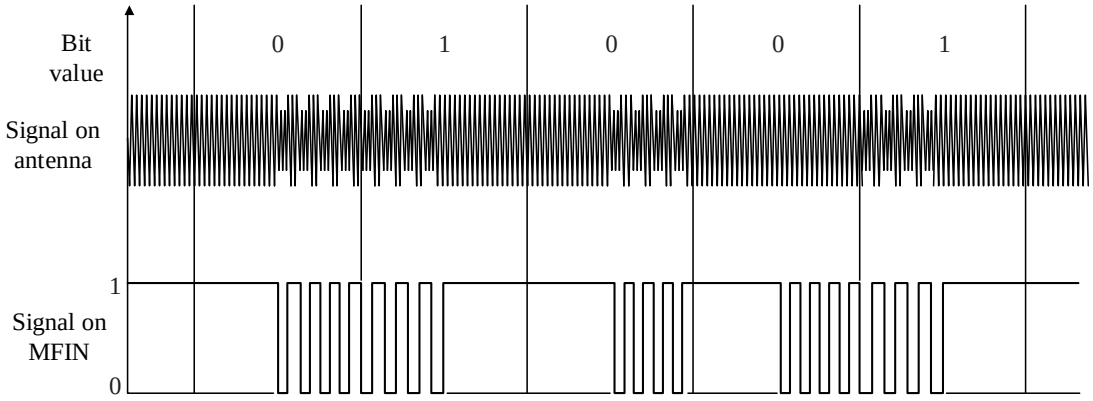


Figure 10.7 Signal shape for MFIN in SAM mode

10.7 Hardware support for FeliCa and NFC polling

10.7.1 Polling sequence functionality for initiator

1. Timer: The Si512 has a timer, which can be programmed in a way that it generates an interrupt at the end of each timeslot, or if required an interrupt is generated at the end of the last timeslot.
2. The receiver can be configured in a way to receive continuously. In this mode it can receive any number of packets. The receiver is ready to receive the next packet directly after the last packet has been received. This mode is active by setting the

bit RxMultiple in register RxModeReg to 1 and has to be stopped by software.

3. The internal UART adds one byte to the end of every received packet, before it is transferred into the FIFO-buffer. This byte indicates if the received byte packet is correct (see register ErrReg). The first byte of each packet contains the length byte of the packet.
4. The length of one packet is 18 or 20 bytes (+ 1 byte Error-Info). The FIFO has a length of 64 bytes. This means three packets can be stored in the FIFO at the same time. If more than three packets are expected, the host controller has to empty the FIFO, before the FIFO is filled completely. In case of a FIFO-overflow data is lost (See bit BufferOvfl in register ErrorReg).

10.7.2 Polling sequence functionality for target

1. The host controller has to configure the Si512 with the correct polling response parameters for the polling command.
2. To activate the automatic polling in Target mode, the AutoColl Command has to be activated.
3. The Si512 receives the polling command send out by an initiator and answers with the polling response. The timeslot is selected automatically (The timeslot itself is randomly generated, but in the range 0 to TSN, which is defined by the Polling command). The Si512 compares the system code, stored in byte 17 and 18 of the Config Command with the system code received by the polling command of an initiator. If the system code is equal, the Si512 answers according to the configured polling response. The system code FF (hex) acts as a wildcard for the system code bytes, i.e. a target of a system code 1234 (hex) answers to the polling command with one of the following system codes 1234 (hex), 12FF (hex), FF34 (hex) or FFFF (hex). If the system code does not match no answer is sent back by the Si512.

If a valid command is received by the Si512, which is not a Polling command, no answer is sent back and the command AutoColl is stopped. The received packet is stored in the FIFO.

10.7.3 Additional hardware support for FeliCa and NFC

Additionally to the polling sequence support for the Felica mode, the Si512

supports the check of the Len-byte. The received Len-byte in accordance to the registers FelNFC1Reg and FelNFC2Reg: DataLenMin in register FelNFC1Reg defines the minimum length of the accepted packet length. This register is six bit long. Each bit represents a length of four bytes. DataLenMax in register FelNFC2Reg defines the maximum length of the accepted package. This register is six bit long. Each bit represents a length of four bytes. If the length is not in the supposed range, the packet is not transferred to the FIFO and receiving is kept active.

Example 1:

- DataLenMin=4：The length shall be greater or equal 16.
- DataLenMax=5：The length shall be smaller than 20. Valid area: 16, 17, 18, 19

Example 2：

- DataLenMin=9：The length shall be greater or equal 36.
- DataLenMax=0：The length shall be smaller than 256. Valid area: 36 to 255

10.7.4 CRC coprocessor

The following CRC coprocessor parameters can be configured:

- The CRC preset value can be either 0000h, 6363h, A671h or FFFFh depending on the ModeReg register's CRCPreset[1:0] bits setting
- The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$
- The CRCResultReg register indicates the result of the CRC calculation. This register is split into two 8-bit registers representing the higher and lower bytes.
- The ModeReg register's MSBFirst bit indicates that data will be loaded with the MSB first.

Table10-4 CRC coprocessor parameters

Parameter	Value
CRC register length	16 bit
CRC algorithm	algorithm according to ISO/IEC 14443 A and ITU-T
CRC preset value	0000h, 6363h, A671h or FFFFh depending on the setting of the ModeReg register's CRCPreset[1:0] bits

11 FIFO

An 8 × 64 bit FIFO buffer is used in the Si512. It buffers the input and output data stream between the host and the Si512's internal state machine. This makes it possible to manage data streams up to 64 bytes long without the need to take timing constraints into account.

11.1 Accessing the FIFO buffer

The FIFO buffer input and output data bus is connected to the FIFODataReg register. Writing to this register stores one byte in the FIFO buffer and increments the internal FIFO buffer write pointer. Reading from this register shows the FIFO buffer contents stored in the FIFO buffer read pointer and decrements the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the FIFOLevelReg register.

When the microcontroller starts a command, the Si512 can, while the command is in progress, access the FIFO buffer according to that command. Only one FIFO buffer has been implemented which can be used for input and output. The microcontroller must ensure that there are not any unintentional FIFO buffer accesses.

11.2 Controlling the FIFO buffer

The FIFO buffer pointers can be reset by setting FIFOLevelReg register's FlushBuffer bit to logic 1. Consequently, the FIFOLevel[6:0] bits are all set to logic 0 and the ErrorReg register's BufferOvfl bit is cleared. The bytes stored in the FIFO buffer are no longer accessible allowing the FIFO buffer to be filled with another 64 bytes.

11.3 FIFO buffer status information

The host can get the following FIFO buffer status information:

1) Number of bytes stored in the FIFO buffer: FIFOLevelReg register's FIFOLevel[6:0]
2) FIFO buffer almost full warning: Status1Reg register's HiAlert bit

3) FIFO buffer almost empty warning: Status1Reg register's LoAlert bit
4) FIFO buffer overflow warning: ErrorReg register's BufferOvfl bit. The BufferOvfl bit can only be cleared by setting the FIFOLevelReg register's FlushBuffer bit.

The Si512 can generate an interrupt signal when:

1) ComIEnReg register's LoAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's LoAlert bit changes to logic 1.
2) ComIEnReg register's HiAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's HiAlert bit changes to logic 1.

If the maximum number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the HiAlert bit is set to logic 1.

HiAlert = (64-FIFOLength)≤WaterLevel

If the number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the LoAlert bit is set to logic 1.

LoAlert = FIFOLength≤WaterLevel

12 Interrupt request system

The Si512 indicates certain events by setting the Status1Reg register's IRq bit and, if activated, by pin IRQ. The signal on pin IRQ can be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

12.1 Interrupt sources overview

Table 12-1 shows the available interrupt bits, the corresponding source and the condition for its activation. The ComIrqReg register's TimerIRq interrupt bit indicates an interrupt set by the timer unit which is set when the timer decrements from 1 to 0.

The ComIrqReg register's TxIRq bit indicates that the transmitter has finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit automatically sets the interrupt bit. The CRC coprocessor sets the DivIrqReg register's CRCIRq bit after processing all the FIFO buffer data which is indicated by CRCReady bit = 1. The ComIrqReg register's RxIRq bit indicates an interrupt when the end of the received data is detected. The ComIrqReg register's IdleIRq bit is set if a command finishes and the Command[3:0] value in the CommandReg register changes to idle.

The ComIrqReg register's HiAlertIRq bit is set to logic 1 when the Status1Reg register's HiAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.The ComIrqReg register's LoAlertIRq bit is set to logic 1 when the Status1Reg register's LoAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's ErrIRq bit indicates an error detected by the contactless UART during send or receive. This is indicated when any bit is set to logic 1 in register ErrorReg.

Table12-1 Interrupt sources

Interrupt flag	Interrupt source	Trigger action
TimerIRq	timer unit	the timer counts from 1 to 0
TxIRq	transmitter	a transmitted data stream ends
CRCIRq	CRC coprocessor	all data from the FIFO buffer has been processed
RxIRq	receiver	a received data stream ends
IdleIRq	ComIRqReg	command execution finishes and the Command[3:0] value in the CommandReg register changes to idle
HiAlertIRq	FIFO	the FIFO buffer is almost full and HiAlert is set
LoAlertIRq	FIFO	the FIFO buffer is almost empty and LoAlert is set
ErrIRq	Contactless UART	an error is detected
CardIRq	ACD	Card detected
RFExIRq	ACD	Detected other 13.56 Mhz RF signal
RFlowIRq	ACD	Sent RF too low
OscMonIRq	OSC monitoring	Osc has failed four times in a row
WdtIRq	Watchdog	Watchdog timer reaches the set time

13 Timer unit

A timer unit is implemented in the Si512. The external host controller may use this timer to manage timing relevant tasks. The timer unit may be used in one of the following configurations:

- Time-out counter
- Watch-dog counter
- Stop watch
- Programmable one-shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events which will be explained in the following, but the timer itself does not influence any internal event (e.g. A time-out during data reception does not influence the reception process automatically). Furthermore, several timer related bits are set and these bits can be used to generate an interrupt.

The timer has an input clock of 13.56 MHz (derived from the 27.12 MHz quartz). The timer consists of two stages: 1 prescaler and 1 counter.The prescaler is a 12-bit counter. The reload value for TPrescaler can be defined between 0 and 4095 in register TModeReg and TPrescalerReg.The reload value for the counter is defined by 16 bits in a range of 0 to 65535 in the register TReloadReg.The current value of the timer is indicated by the register TCounterValReg.

If the counter reaches 0 an interrupt will be generated automatically indicated by setting the TimerIRq bit in the register CommonIRqReg. If enabled, this event can be indicated on the IRQ line. The bit TimerIRq can be set and reset by the host controller. Depending on the configuration the timer will stop at 0 or restart with the value from register TReloadReg.

The status of the timer is indicated by bit TRunning in register Status1Reg.

The timer can be manually started by TStartNow in register ControlReg or manually stopped by TStopNow in register ControlReg.Furthermore the timer can be activated automatically by setting the bit TAuto in the register TModeReg to fulfill dedicated protocol requirements automatically

The time delay of a timer stage is the reload value +1. If TPrescaleEven bit is 0,the definition of total time is：t=(TPrescaler*2+1)*(TRload+1)/13.56MHz

if TPrescaleEven bit is set: t =(TPrescaler*2+2)*(TRload+1)/13.56MHz.

Maximum time：TPrescaler = 4095，TReloadVal = 65535

=>(2*4095+2)*65536/13.56MHz = 39.59s

Example:

To indicate 25 us it is required to count 339 clock cycles. This means the value for TPrescaler has to be set to TPrescaler = 169.The timer has now an input clock of 25 us. The timer can count up to 65535 timeslots of each 25 µs.

14 Power reduction modes

14.1 Hard power-down

Hard power-down is enabled when pin NRSTPD is LOW. This turns off all internal current sinks including the oscillator. All digital input buffers are separated from the input pins and clamped internally (except pin NRSTPD). The output pins are frozen at either a HIGH or LOW level.

14.2 Soft power-down mode

Soft Power-down mode is entered immediately after the CommandReg register's PowerDown bit is set to logic 1. All internal current sinks are switched off, including the oscillator buffer. However, the digital input buffers are not separated from the input pins and keep their functionality. The digital output pins do not change their state.

During soft power-down, all register values, the FIFO buffer content and the configuration keep their current contents.

After setting the PowerDown bit to logic 0, it takes 1024 clocks until the Soft power-down mode is exited indicated by the PowerDown bit. Setting it to logic 0 does not immediately clear it. It is cleared automatically by the Si512 when Soft power-down mode is exited.

NOTE: If the internal oscillator is used, you must take into account that it is supplied by pin AVDD and it will take a certain time (t_{osc}) until the oscillator is stable and the clock cycles can be detected by the internal logic. It is recommended for the serial UART, to first send the value 55h to the Si512. The oscillator must be stable for further access to the registers. To ensure this, perform a read access to address 0 until the Si512 answers to the last read command with the register content of address 0. This indicates that the Si512 is ready.

14.3 Transmitter power-down mode

The Transmitter Power-down mode switches off the internal antenna drivers

thereby, turning off the RF field. Transmitter power-down mode is entered by setting either the TxControlReg register's Tx1RFEn bit or Tx2RFEn bit to logic 0

15 Oscillator circuitry

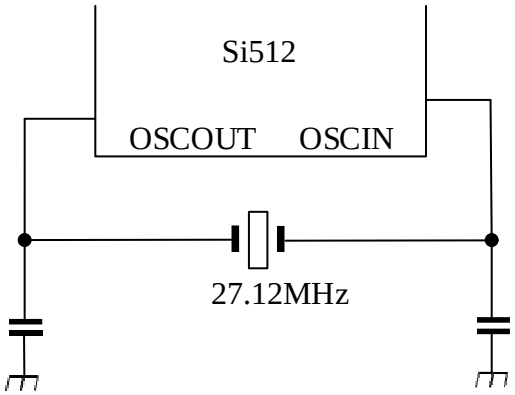


Figure 15.1 Quartz crystal connection

The clock applied to the Si512 provides a time basis for the synchronous system's encoder and decoder. The stability of the clock frequency, therefore, is an important factor for correct operation. To obtain optimum performance, clock jitter must be reduced as much as possible. This is best achieved using the internal oscillator buffer with the recommended circuitry.

If an external clock source is used, the clock signal must be applied to pin OSCIN. In this case, special care must be taken with the clock duty cycle and clock jitter and the clock quality must be verified.

16 Reset and oscillator start-up time

16.1 Reset timing requirements

The reset signal is filtered by a hysteresis circuit and a spike filter before it enters the digital circuit. The spike filter rejects signals shorter than 10 ns. In order to perform a reset, the signal must be LOW for at least 100 ns.

16.2 Oscillator start-up time

If the Si512 has been set to a Power-down mode or is powered by a VDD supply, the start-up time for the Si512 depends on the oscillator used and is shown in Figure 16.1

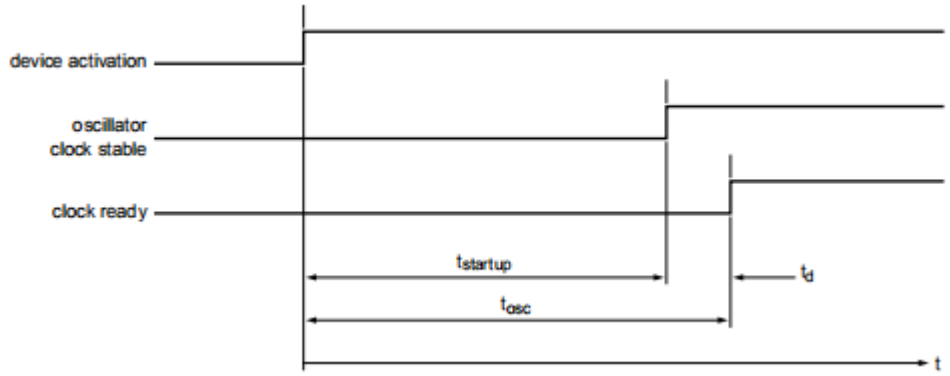


Figure 16.1 Oscillator start-up time

The time ($t_{startup}$) is the start-up time of the crystal oscillator circuit. the time (t_d) is the internal delay time of the Si512 when the clock signal is stable before the Si512 can be addressed.

The delay time is calculated by:

$$t_d = \frac{1024}{27\ \mu\ s} = 37.74\ \mu\ s$$

The time (t_{OSC}) is the sum of t_d and $t_{startup}$.

17 Command set

The Si512 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code to the CommandReg register. Arguments and/or data necessary to process a command are exchanged via the FIFO buffer.

17.1 General description

- Each command that needs a data bit stream (or data byte stream) as an input immediately processes any data in the FIFO buffer. An exception to this rule is the Transceive command. Using this command, transmission is started with the BitFramingReg register's StartSend bit.
- Each command that needs a certain number of arguments, starts processing only when it has received the correct number of arguments from the FIFO buffer.
- The FIFO buffer is not automatically cleared when commands start. This makes it possible to write command arguments and/or the data bytes to the FIFO buffer and then start the command.
- Each command can be interrupted by the host writing a new command code to the CommandReg register, for example, the Idle command.

17.2 Command overview

Table 17-1 Command overview

Command	Command code	Description
Idle	0000	no action, cancels current command execution
Configure	0001	Configures the Si512 for FeliCa and NFCIP-1 communication
Generate RandomID	0010	generates a 10-byte random ID number
CalcCRC	0011	activates the CRC coprocessor or performs a self test
Transmit	0100	transmits data from the FIFO buffer
MStart	0101	Trigger 3K RC automatic correction
ADC_EXCUTE	0110	Automatically obtain Poll reference values
NoCmdChange	0111	no command change, can be used to modify the CommandReg register bits without affecting the command, for example, the PowerDown bit
Receive	1000	activates the receiver circuits
Transceive	1100	transmits data from FIFO buffer to antenna and automatically activates the receiver after transmission
AutoColl	1101	Handles FeliCa polling (Card Operation mode only)
SoftReset	1111	resets the Si512

17.3 Command descriptions

17.3.1 Idle

Places the Si512 in Idle mode. The Idle command also terminates itself.

17.3.2 Config

To use the FeliCa Polling and NFCID3 the data used for these transactions has to be stored internally. All the following data have to be written to the FIFO in this order:

1) SENS_RES (2 bytes); in order byte 0, byte 1
2) NFCID1 (3 Bytes); in order byte 0, byte 1, byte 2; the first NFCID1 byte is

fixed to 08h and the check byte is calculated automatically.

3) SEL_RES (1 Byte)
4) polling response (2 bytes (shall be 10h, FEh) + 6 bytes NFCID2 + 8 bytes Pad + 2 bytes system code)
5) NFCID3 (1 byte)

In total 25 bytes are transferred into an internal buffer.

The complete NFCID3 is 10 bytes long and consists of the 3 NFCID1 bytes, the 6 NFCID2 bytes and the one NFCID3 byte which are listed above. To read out this configuration the command Config with an empty FIFO-buffer has to be started. In this case the 25 bytes are transferred from the internal buffer to the FIFO.

The Si512 has to be configured after each power up, before using the automatic Anticollision/Polling function (AutoColl command). During a hard power down (reset pin) this configuration remains unchanged. This command terminates automatically when finished and the active command is idle.

17.3.3 Generate RandomID

This command generates a 10-byte random number which is initially stored in the internal buffer. This then overwrites the 10 bytes in the internal 25-byte buffer. This command automatically terminates when finished and the Si512 returns to Idle mode.

17.3.4 CalcCRC

The FIFO buffer content is transferred to the CRC coprocessor and the CRC calculation is started. The calculation result is stored in the CRCResultReg register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped when the FIFO buffer is empty during the data stream. The next byte written to the FIFO buffer is added to the calculation.

The CRC preset value is controlled by the ModeReg register's CRCPreset[1:0] bits. The value is loaded in to the CRC coprocessor when the command starts.

This command must be terminated by writing a command to the CommandReg register, such as, the Idle command.

If the AutoTestReg register's SelfTest[3:0] bits are set correctly, the Si512 enters

Self Test mode. Starting the CalcCRC command initiates a digital self test. The result of the self test is written to the FIFO buffer.

17.3.5 Transmit

The FIFO buffer content is immediately transmitted after starting this command. Before transmitting the FIFO buffer content, all relevant registers must be set for data transmission.

This command automatically terminates when the FIFO buffer is empty. It can be terminated by another command written to the CommandReg register.

17.3.6 MStart

Calibrate 3K RC automatically ,when Max is set to 0，only rough calibration.When Max is set to 1,first rough calibration and followed by precision calibration.

17.3.7 ADC_EXCUTE

Automatically start ADC for RF measurement.

17.3.8 NoCmdChange

This command does not influence any running command in the CommandReg register. It can be used to manipulate any bit except the CommandReg register Command[3:0] bits, for example, the RcvOff bit or the PowerDown bit.

17.3.9 Receive

The Si512 activates the receiver path and waits for a data stream to be received. The correct settings must be chosen before starting this command.

This command automatically terminates when the data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected frame type and speed.

NOTE: If the RxModeReg register's RxMultiple bit is set to logic 1, the Receive command will not automatically terminate. It must be terminated by starting another command in the CommandReg register.

17.3.10 Transceive

This command continuously repeats the transmission of data from the FIFO buffer and the reception of data from the RF field.

Each transmit process must be started by setting the BitFramingReg register's StartSend bit to logic 1. This command must be cleared by writing any command to the CommandReg register.

NOTE: If the RxModeReg register's RxMultiple bit is set to logic 1, the Transceive command never leaves the receive state because this state cannot be cancelled automatically.

17.3.11 AutoColl

This command automatically handles the FeliCa polling in the Card Operation mode. The bit Initiator in the register ControlReg has to be set to logic 0 for correct operation. During this command also the mode detector is active if not deactivated by setting the bit ModeDetOff in the ModeReg register. After the mode detector detects a mode, all the mode dependent registers are set according to the received data. In case of no external RF field the command resets the internal state machine and returns to the initial state but it will not be terminated. When the command terminates the transceive command gets active.

During protocol processing the IRQ bits are not supported. Only the last received framewill serve the IRQ's. The treatment of the TxCRCEn and RxCRCEn bits is different to the protocol. During ISO/IEC 14443A activation the enable bits are defined by the command AutoColl. The changes cannot be observed at the register TXModeReg and RXModeReg. After the Transceive command is active, the value of the register bit is relevant.

The FIFO will also receive the two CRC check bytes of the last command even if they already checked and correct, if the state machine (Anticollision and Select routine)

has to not been executed and 106kbit is detected.

During Felica activation the register bit is always relevant and is not overruled by the command settings. This command can be cleared by software by writing any other command to the CommandReg register, e.g. the Idle command. Writing the same content again to the CommandReg register resets the state machine.

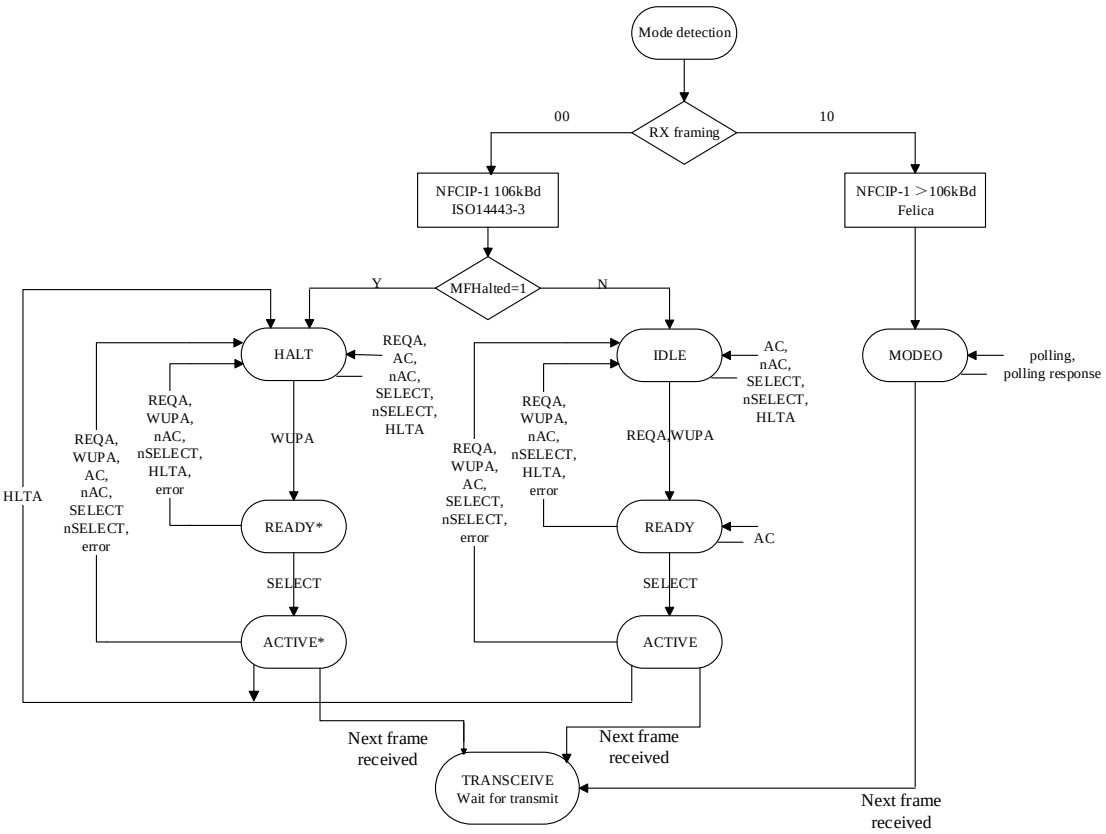


Figure 17.1 AutoColl Command

NFCIP-1 106kbps Passive Communication mode:

The FIFO contains the ATR_REQ frame including the start byte F0h. The bit TargetActivated in the Status2Reg register is set to logic 1.

NFCIP-2 212/424kbps Passive Communication mode:

The FeliCa polling command is finished and the command has automatically changed to Transceive. The FIFO contains the ATR_REQ. The bit TargetActivated in the Status2Reg register is set to logic 1.

NFCIP-1 106/212/424kbps Active Communication mode:

This command is changing the automatically to the command Transceive. The FIFO contains the ATR REQ.The bit TargetActivated in the Status2Reg register is set

to logic 0. For 106 kbps only, the first byte in the FIFO indicates the start byte F0h and the CRC is added to the FIFO.

Felica (Card Operation mode)：

The FeliCa polling command is finished and the command has automatically changed to transceive. The FIFO contains the first command followed after the Poling by the FeliCa protocol. The bit TargetActivated in the Status2Reg register is set to logic 1.

17.3.12 SoftReset

This command performs a reset of the device. The configuration data of the internal buffer remains unchanged. All registers are set to the reset values. This command automatically terminates when finished.

NOTE: The SerialSpeedReg register is reset and therefore the serial data rate is set to 9.6 kBd.

18 Application design-in information

The figure below shows a typical circuit diagram, using a complementary antenna connection to the Si512.

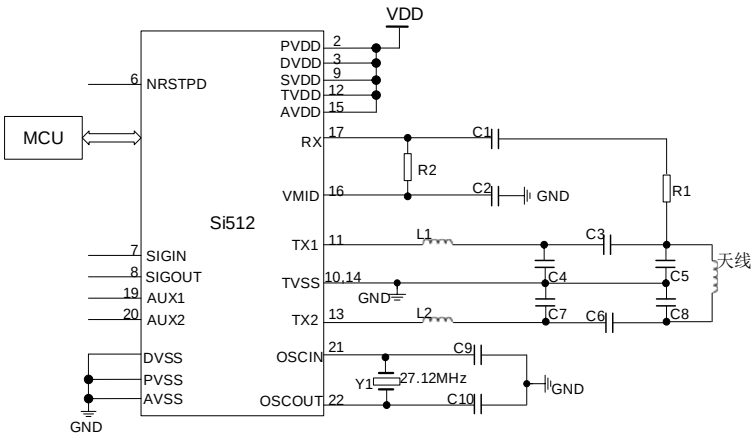


Figure 18.1 Typical circuit diagram

19 Recommended operating conditions

The limit parameters and recommended working environment are shown in the table below：

Table19-1 Limit parameter

Parameter	Symbol	Min	Max	Unit
Supply voltage	VDD	2.3	4	V
Temperature	Tamb	-40	+110	℃

Table19-2 Recommend working environment

Parameter	Symbol	Conditions	Min	Typical	Max	Unit
Analog supply voltage	VDDA	AVDD=VDD(PVDD)=VDD(TVDD); VSSA=VSSD=VSS(PVSS)=VSS(TVSS)=0V	2.3	3.3	3.6	V
TVDD supply voltage	VDD(TVDD)		2.3	3.3	3.6	V
PVDD supply voltage	VDD(PVDD)		2.3	3.3	3.6	V
SVDD supply voltage	VDD(SVDD)	VSSA=VSSD=VSS(PVSS)=VSS(TVSS)=0V	2.3	3.3	3.6	V
Temperature	Tamb	QFN32	-40	-	+110	℃

20 Package information

Package specifications：

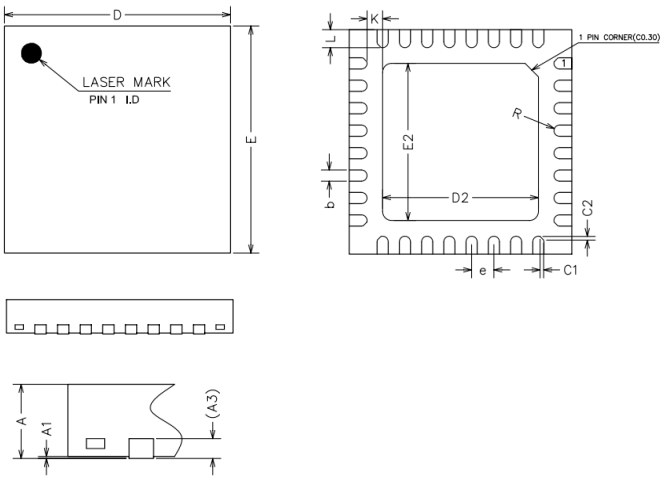


Figure 20.1 Si512 package outline package version

Parameter （unit：mm）：

Table 20-1 typical specifications

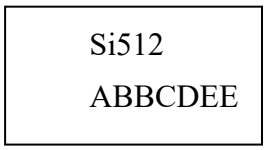
Symbol	Min	Typical	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.20REF		
b	0.23	0.25	0.28
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.35	3.50	3.65
E2	3.35	3.50	3.65
e	0.48	0.50	0.53
K	0.20	-	-
L	0.35	0.40	0.45
R	0.09	-	-
c1	-	0.08	-
c2	-	0.08	-

21 Revision history

Version	Modified date	Modified content
V1.0	2023/11/13	First draft

22 Order Information

Package marking



Si512: chip code

A: package date code, 5 represents year 2020

BB: week of sending out processing, 42 represents in the year A the 42th week

C: package factory code, A、HT、NJ or WA, can also abbreviated as A、H、N or W

D: test factory code, A、Z or H

EE: production batch code

Table22-1 order information

Order code	package	container	minimum
Si512-Sample	5×5mm 32-pin QFN	Box/Tube	5
Si512	5×5mm 32-pin QFN	Tape and reel	4K

23 Technical Support and Contact information

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