SA571 COMPANDOR

1. General Description

1.1 Description

The SA571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier./

The SA571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

1.2 Features

- Complete Compressor and Expandor in one IChip
- Temperature Compensated
- Greater than 110 dB Dynamic Range
- Operates Down to 6.0 VDC
- System Levels Adjustable with External Components
- Distortion may be Trimmed Out
- Dynamic Noise Reduction Systems
- Voltage Controlled Amplifier

1.3 Device Information

PART NUMBER	PACKAGE
SA571	DIP
	SOP - W
	TSSOP

2. Connection Diagrams and Pin Description

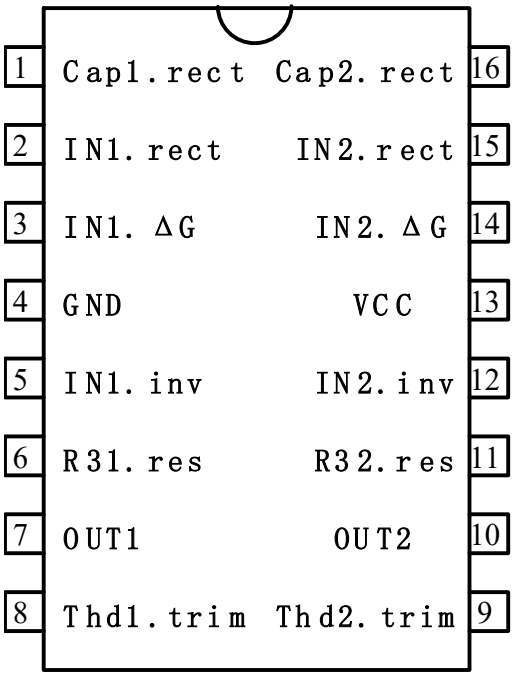


Figure 2.1 Top View

3. System Diagram

3.1 Logic Diagram

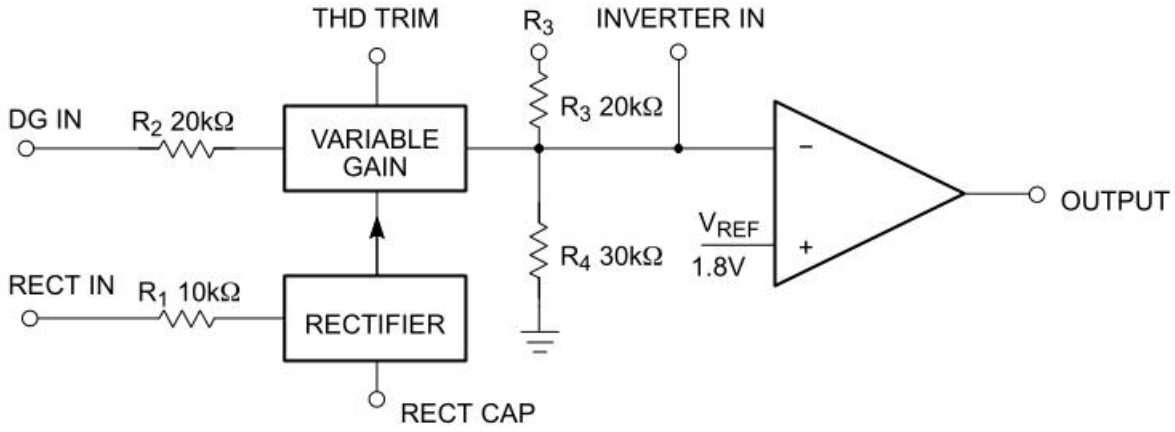


Figure 3.1：SA571 Logic Diagram

4. Specifications

4.1 Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit
V_{CC}	Supply Voltage	--	18	V
T_J	Operating Junction Temperature	-55	150	℃
T_A	Operating Ambient Temperature	-40	85	℃

Absolute maximum ratings are those values beyond which the device could be permanently damaged,These are stress ratings only,which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions.

4.2 Electrical Characteristics

4.2.1 DC Specifications

(Vcc=15V，Ta＝25°C， unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	VCC	--	6	--	18	V
Supply Current	ICC	No Signal	--	4.2	4.8	mA
Output Current Capability	IOUT	--	±20	--	--	mA
Output Slew Rate	SR	--	--	±.5	--	V/μs
Gain Cell Distortion (Note 2)		Untrimmed Trimmed	--	0.5 0.1	2.0	%
Resistor Tolerance		--	--	±5	±15	%
Internal Reference Voltage		--	1.65	1.8	1.95	V
Output DC Shift (Note 3)		Untrimmed	--	±90	±150	mV
Expandor Output Noise		No Signal, 15 Hz−20 kHz (Note 1)	--	20	60	μV
Unity Gain Level (Note 5)		1.0kHz	-1.5	0	+1.5	dBm
Gain Change (Notes 2 and 4)		--	--	±0.1	--	dB
Reference Drift (Note 4)		--	--	+2, -25	+20,-50	mV
Resistor Drift (Note 4)		-40℃ to +85℃	--	+10, -12	--	%
Tracking Error (Measured Relative to Value at Unity Gain) Equals [VO − VO (unity gain)] dB − V2dBm		Rectifier Input, VCC = +6.0 V V2 = +6.0 dBm, V1 = 0 dB V2 = −30 dBm, V1 = 0 dB	--	 +0.2 +0.2	 -1,+1.5	dB
Channel Separation		--	--	60	--	dB

Note1: Input to V1 and V2 grounded.

Note2: Measured at 0 dBm, 1.0 kHz.

Note3: Expandor AC input change from no signal to 0 dBm.

Note4: Relative to value at TA = 25°C.

Note5: 0 dBm = 775 mV_{RMS}.

5. Circuit Description

The SA571 compandor building blocks, as shown in the block diagram, are a full−wave rectifier, a variable gain cell,an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full−wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at VREF. The rectified current is averaged on an external filter capacitor tied to the CRECT terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively−coupled voltage inputs as shown in the following equation. Note that for capacitively−coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1 μA.

$$G \propto \frac{|V_{IN} - V_{REF}|\,avg}{R_1}$$

or

$$G \propto \frac{|V_{IN}|\,avg}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a trade−off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\, e^{\frac{-t}{\tau}} + G_{final}$$

$$\tau = 10k\Omega \times C_{RECT}$$

The variable gain cell is a current−in, current−out device with the ratio IOUT/IIN controlled by the rectifier. IIN is the current which flows from the ΔG input to an internal summing node biased at VREF. The following equation applies for capacitively−coupled inputs. The output current, IOUT, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non−inverting input tied to VREF, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R3, is brought out from the summing node and allows compressor or expander gain to be determined only by internal components.

The output stage is capable of ± 20 mA output current.This allows a +13 dBm (3.5 VRMS) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13 dBm with a 600 Ω output impedance.

A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input−output transfer curve for basic compressor or expander circuits.

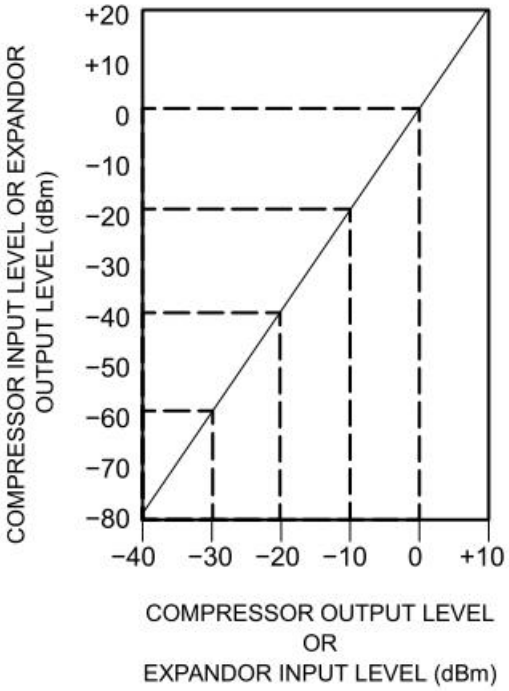


Figure 5.1：Basic Input−Output Transfer Curve

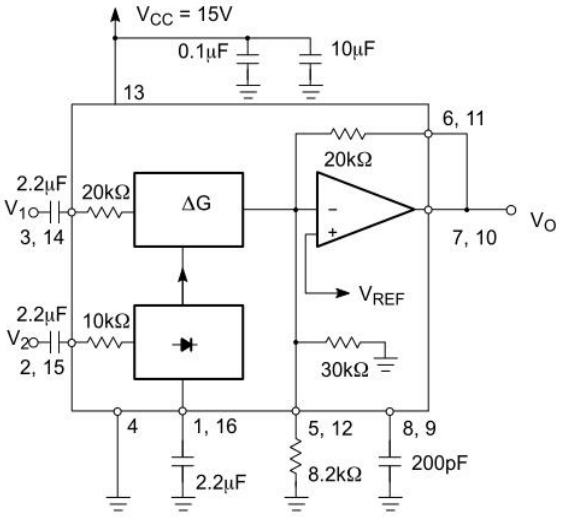


Figure 5.2：Typical Test Circuit

6. INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non−critical applications, an integrated circuit operational transconductance amplifier can be used, but when high−performance is required, one has to resort to complex discrete circuitry with many expensive, well−matched components. This paper describes an inexpensive integrated circuit, the SA571 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<0.1%), high signal−to−noise ratio (90 dB), and wide dynamic range (110 dB).

6.1 Circuit Background

The SA571 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal−to−noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 4.3 graphically shows what a compandor can do for the signal−to−noise ratio of a restricted dynamic range channel. The input level range of +20 to −80 dB is shown undergoing a 2−to−1 compression where a 2.0 dB input level change is compressed into a 1.0 dB output level change by the compressor. The original 100 dB of dynamic range is thus compressed to a 50 dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45 dB.

The significant circuits in a compressor or expander are the rectifier and the gain control element. The phone system requires a simple full−wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple Operational Transconductance Multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

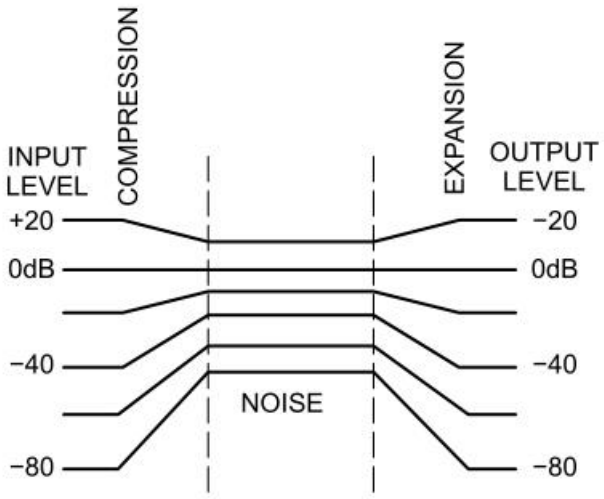


Figure 6.1：Restricted Dynamic Range Channel

6.2 Basic Hook−up and Operation

Figure 6.2 shows the block diagram of one half of the chip,(there are two identical channels on the IC). The full−wave averaging rectifier provides a gain control current, IG, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8 V reference denoted VREF. The non−inverting input of the op amp is tied to VREF, and the summing nodes of the rectifier and ΔG cell(located at the right of R1 and R2) have the same potential. The THD trim pin is also at the VREF potential.

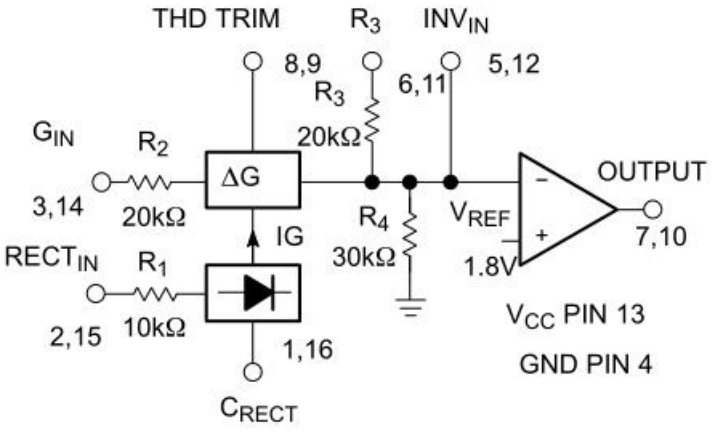
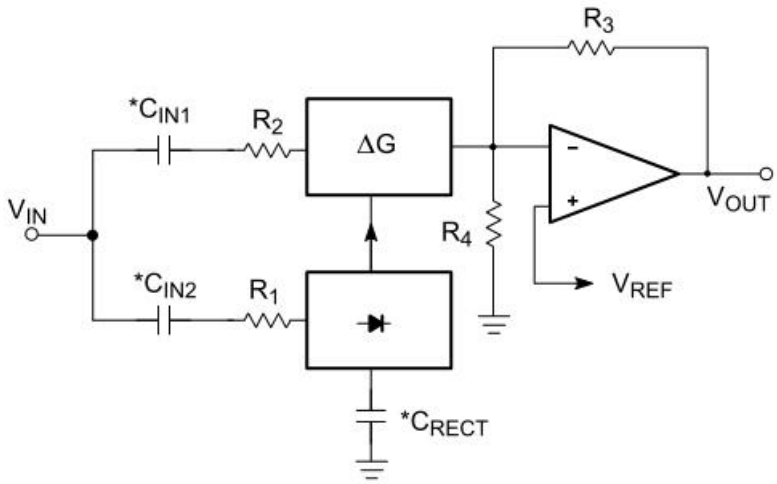


Figure 6.2：Chip Block Diagram (1 of 2 Channels)

Figure 6.3 shows how the circuit is hooked up to realize an expandor. The input signal, VIN, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6.0 dB, the gain control current will drop by a factor of 2, and so the gain will drop 6.0 dB. The output level at VOUT will thus drop 12 dB, giving us the desired 2−to−1 expansion.



NOTE: $GAIN = \left(\frac{2\,R_3\,V_{IN}\,(avg)}{R_1\,R_2\,I_B}\right)^2$

$I_B = 140\mu A$

*EXTERNAL COMPONENTS

Figure 6.3： Basic Expander

Figure 6.4 shows the hook−up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two RDC and CDC. The values of RDC will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\,DC = \left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) V_{REF}$$

$$V_{OUT}\,DC = \left(1 + \frac{R_{DCTOT}}{30k\Omega}\right) 1.8V$$

The output of the expander will bias up to:

$$V_{OUT}\,DC = \left(1 + \frac{R_3}{R_4}\right) V_{REF}$$

$$V_{OUT}\,DC = \left(1 + \frac{20k\Omega}{30k\Omega}\right) 1.8V = 3.0V$$

The output will bias to 3.0 V when the internal resistors are used. External resistors may be placed in series with R3, (which will affect the gain), or in parallel with R4 to raise the DC bias to any desired value.

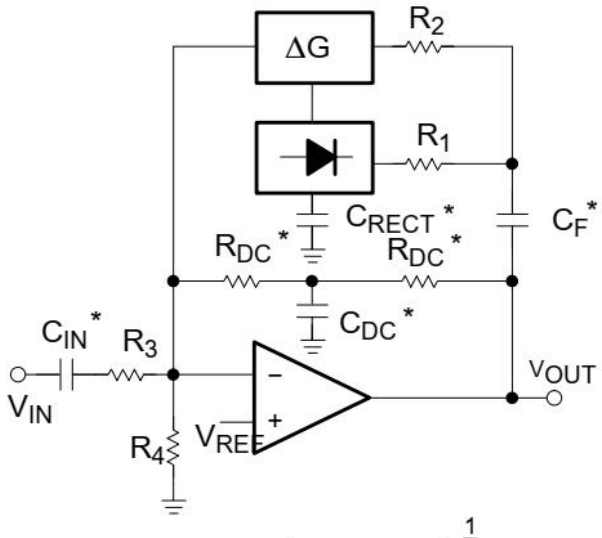


Figure 6.4： Basic Expander

6.3 Circuit Details - Rectifier

Figure 6.5 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, VIN/R1, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become IG, the gain control current.

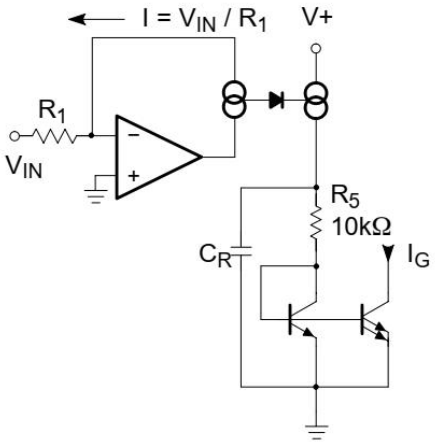
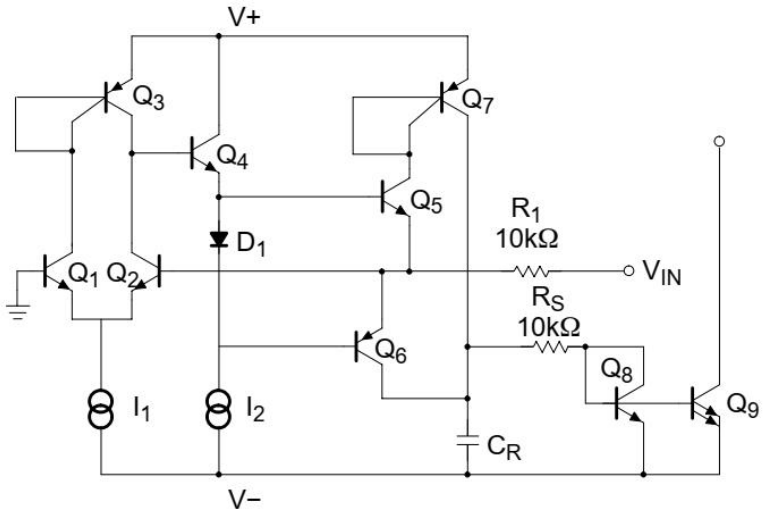


Figure 6.5： Rectifier Concept

Figure 6.6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q1), which is shown grounded, is actually tied to the internal 1.8 V, VREF. The inverting input is tied to the op amp output, (the emitters of Q5 and Q6), and the input summing resistor R1. The single diode between the bases of Q5 and Q6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q5 and Q6. Q6 will conduct when the input swings positive and Q5 conducts when the input swings negative. The collector currents will be in error by the α of Q5 or Q6 on negative or positive signal swings, respectively. ICs such as this have typical NPN β's of 200 and PNP β's of 40. The α's

of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13 dB gain error.



NOTE: $I_G = 2\frac{V_{IN}\,avg}{R\,1}$

Figure 6.6： Simplified Rectifier Schematic

At very low input signal levels the bias current of Q2, (typically 50 nA), will become significant as it must be supplied by Q5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the VIN input pin and the base of Q2, an error current of VOS/R1 will be generated. A mere 1.0 mV of offset will cause an input current of 100 nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled capacitively. At high input levels the β of the PNP Q6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250 uA. If necessary, an external resistor may be placed in series with R1 to limit the current to this value. Figure 6.7 shows the rectifier accuracy vs. input level at a frequency of 1.0 kHz.

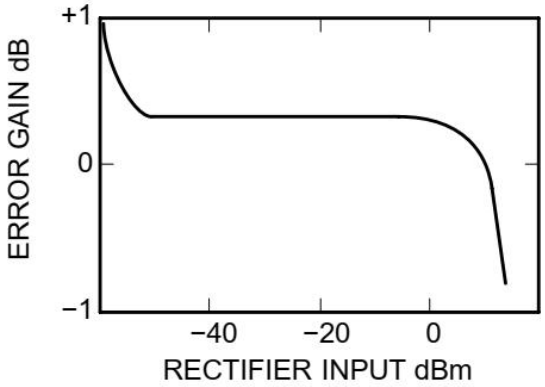


Figure 6.7： Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q5 or Q6 conducting. The rectifier frequency response for input levels of 0 dBm, -20 dBm, and -40 dBm is shown in Figure 6.8. The response at all three levels is flat to well above the audio range.

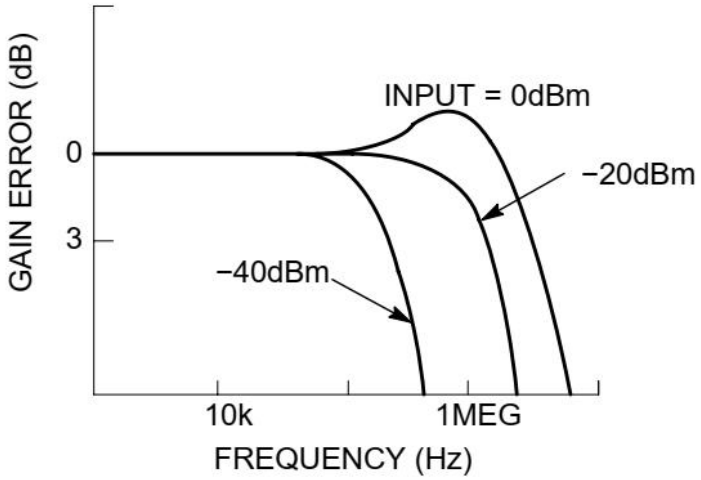


Figure 6.8： Rectifier Frequency Response vs. Input Level

6.4 Variable Gain Cell

Figure 6.9 is a diagram of the variable gain cell. This is a linearized two-quadrant transconductance multiplier. Q1, Q2 and the op amp provide a predistorted drive signal for the gain control pair, Q3 and Q4. The gain is controlled by IG and a current mirror provides the output current.

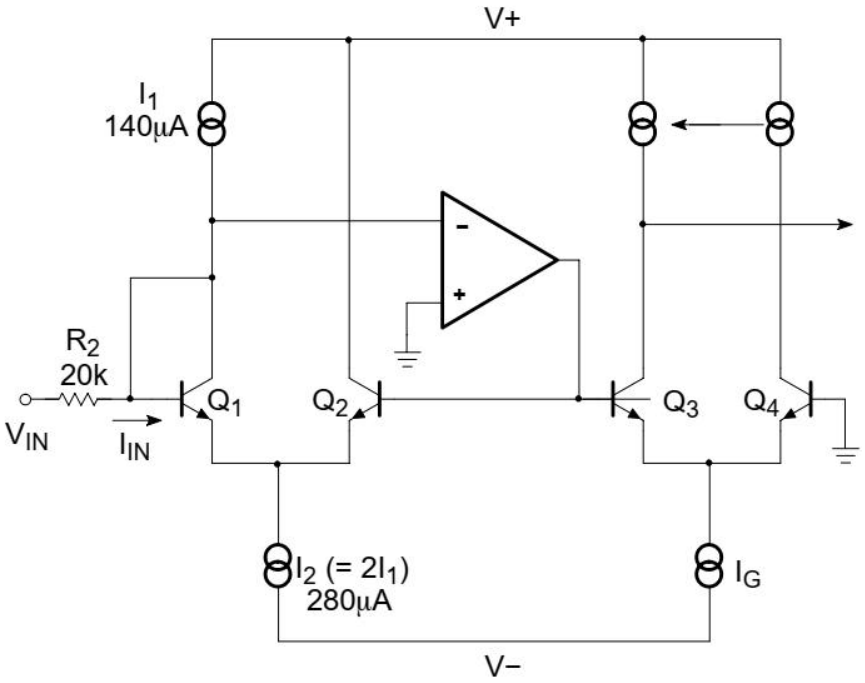


Figure 6.9：Simplified ΔG Cell Schematic

The op amp maintains the base and collector of Q1 at ground potential (VREF) by controlling the base of Q2. The input current IIN (= VIN/R2) is thus forced to flow through Q1 along with the current I1, so IC1 = I1 + IIN. Since I2 has been set at twice the value of I1, the current through Q2 is:

$$I_2 - (I_1 + I_{IN}) = I_1 - I_{IN} = I_{C2}.$$

The op amp has thus forced a linear current swing between Q1 and Q2 by providing the proper drive to the base of Q2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q1 and Q2, under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q3 and Q4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships IG = IC3 + IC4 and IOUT = IC4 - IC3 will yield the multiplier transfer function,

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN}}{R_2} \frac{I_G}{I_1}$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 6.10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8 dBm level. At a nominal operating level of 0 dBm, a 1.0 mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 6.11 shows the simple trim network required.

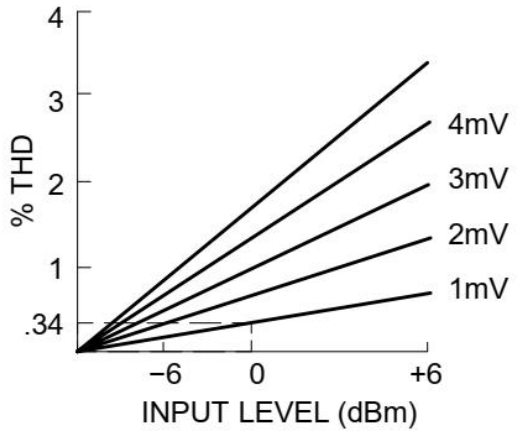


Figure 6.10：ΔG Cell Distortion vs. Offset Voltage

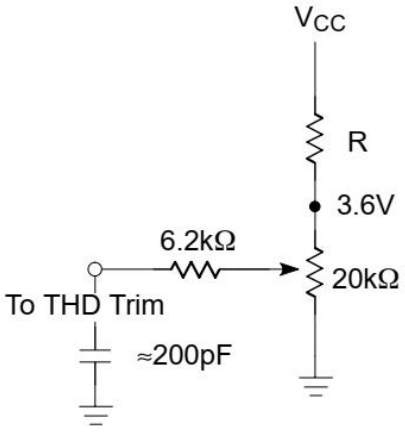


Figure 6.11：THD Trim Network

Figure 6.12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20 kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20 dB of gain reduction. At high gains, the signal to noise ratio is 90 dB, and the total dynamic range from maximum signal to minimum noise is 110 dB.

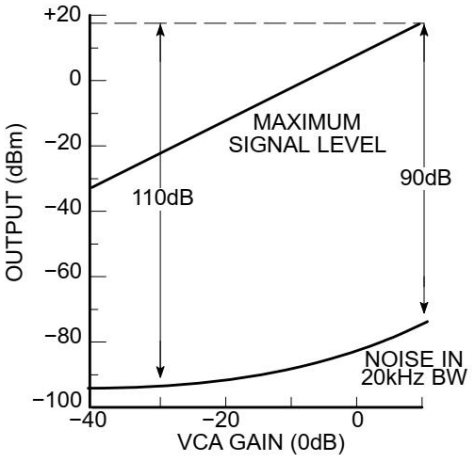


Figure 6.12：Dynamic Range

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I1 and I2. When no input signal is present, changing IG will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I1. Figure 6.13 shows such a trim network.

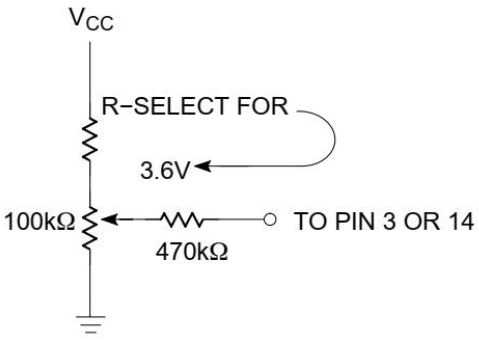


Figure 6.13：Control Signal Feedthrough

6.5 Operation Amplifier

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1.0 MHz bandwidth. Figure 6.14 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10 pF may be used. The output stage, although capable of output currents in excess of 20 mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

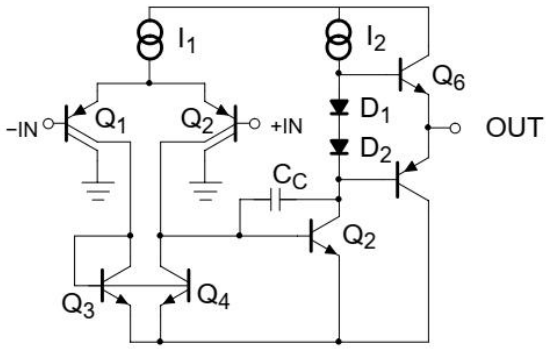


Figure 6.14：Operational Amplifier

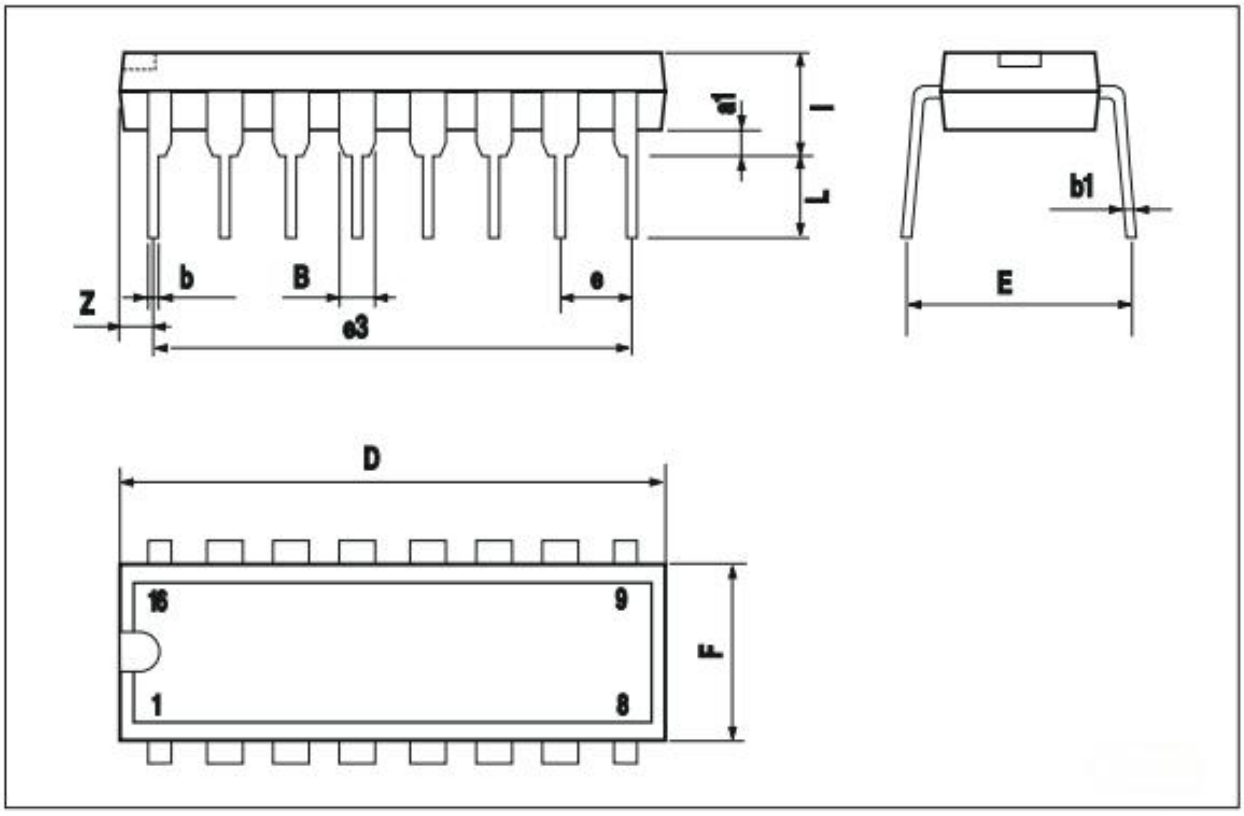
7. Ordering Information

Orderable Device	Package Type	Pins	Packing	Package Qty
SA571ND16ATBE	DIP	16	Tube	25
SA571WS16ARBQ	SOP - W	16	Tape & Reel	2000
SA571TS16ARDQ	TSSOP	16	Tape & Reel	4000

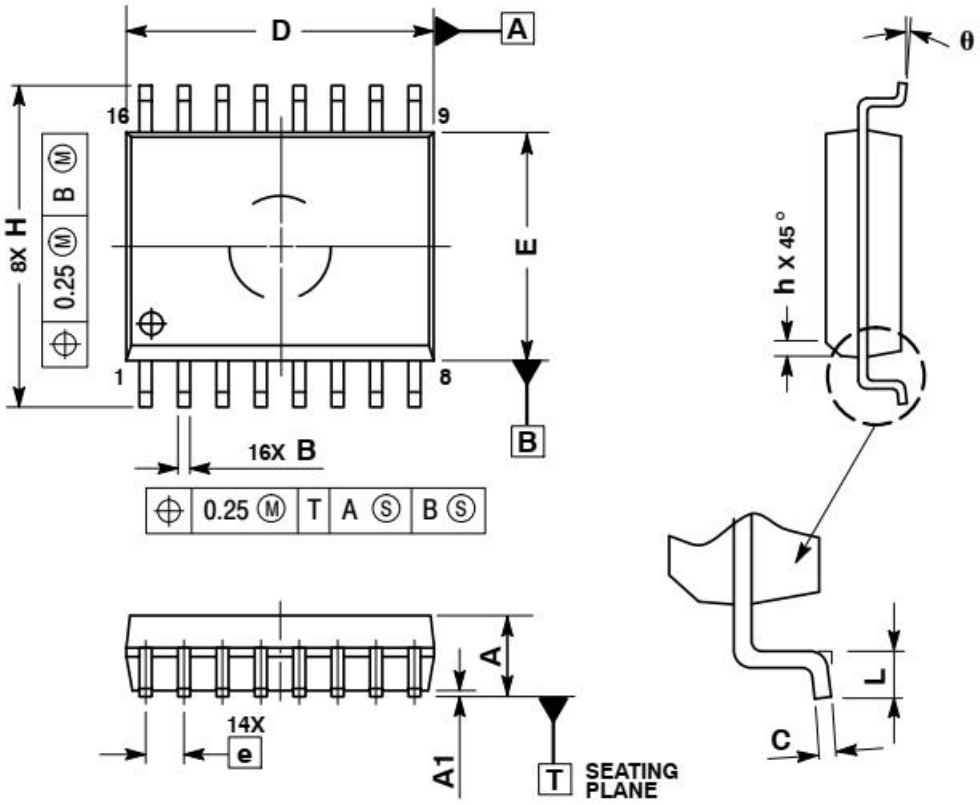
8. Package Information

8.1 DIP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



8.2 SOP16 - W



DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0 °	7 °

8.3 TSSOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030