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NC7SZ74 TinyLogic[®] UHS D-Type, Flip-Flop with Preset and Clear

Features

- Ultra-High Speed: t_{PD} 2.6ns (Typical) into 50pF at 5V V_{CC}
- High Output Drive: ±24mA at 3V V_{CC}
- Broad V_{cc} Operating Range: 1.65V to 5.5V
- Power Down High-Impedance Inputs/Outputs
- Over-Voltage Tolerance Inputs Facilitate 5V to 3V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak[™] Package

Ordering Information

Space-Saving US8 Surface Mount Package

Description

The NC7SZ74 is a single, D-type, CMOS flip-flop with preset and clear from Fairchild's ultra high-speed series of TinyLogic[®]. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive, while maintaining low static power dissipation over a very broad V_{CC} operating range of 1.65V to 5.5V V_{CC}. The inputs and outputs are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V, independent of V_{CC} operating voltage.

The signal level applied to the D input is transferred to the Q output during the positive-going transition of the CLK pulse.

Part Number	Top Mark	Package	Packing Method
NC7SZ74K8X	SZ74	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide-	3000 Units on Tape & Reel
NC7SZ74L8X	N9	8-Lead MicroPak, 1.6 mm Wide	5000 Units on Tape & Reel



Function Table

	Inp	outs		Ou	tput	Function
/CLR	/PR	D	СК	Q	/Q	Function
L	Н	Х	Х	L	Н	Clear
Н	L	Х	Х	Н	L	Preset
L	L	Х	Х	Н	Н	
Н	Н	L	\uparrow	L	Н	
Н	Н	Н	\uparrow	Н	L	
Н	Н	Х	\downarrow	Q _n	/Q _n	No Change
H = HIGH Log	gic Level	Qn = No chan	ige in data	X = Immaterial	\downarrow = Falling Edge	
L = LOW Log	ic Level	Z = High Impe	edance	↑ = Rising Edge		

NC7SZ74 — TinyLogic[®] UHS D-Type Flip-Flop with Preset and Clear

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Pa	rameter	Min.	Max.	Unit
V _{CC}	Supply Voltage		-0.5	7.0	V
V _{IN}	DC Input Voltage		-0.5	7.0	V
V _{OUT}	DC Output Voltage		-0.5	7.0	V
I _{IK}	DC Input Diode Current	V _{IN} < 0V		-50	mA
loк	DC Output Diode Current	V _{OUT} < 0V		-50	mA
I _{OUT}	DC Output Source/Sink Curre	ent		±50	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current			±50	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
TJ	Junction Temperature Under	Bias		+150	°C
TL	Junction Lead Temperature (Soldering, 10 Seconds)		+260	°C
PD	Power Dissipation at +85°C			250	mW
FOD	Human Body Model, JEDEC:	JESD22-A114		5000	N
ESD	Charge Device Model: JEDEC	C:JESD22-C101		2000	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
M	Supply Voltage Operating		1.65	5.50	V
V _{CC}	Supply Voltage Data Retention		1.50	5.50	V
V _{IN}	Input Voltage		0	5.5	V
V		Active State	0	V _{CC}	V
V _{OUT}	Output Voltage	3-State	0	5.5	
		V_{CC} =1.8V, 2.5V ± 0.2V	0	20	
t _r , t _f	Input Rise and Fall Times	$V_{CC}=3.3V \pm 0.3V$	0	10	ns/V
		V _{CC} =5.0V ± 0.5V	0	5	
T _A	Operating Temperature		-40	+85	°C
0	Thermal Desistance	US8		250	°C/W
θ_{JA}	Thermal Resistance	MicroPak™-8		280	0/00

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

•	Symbol Parameter	N/		T,	₄=+25°	°C	T _A =-40	to +85°C	
Symbol	Parameter	Vcc	Conditions	Min.	Тур.	Max.	Min.	Max.	Units
	HIGH Level Control	1.65 to 1.95		0.75V _{cc}			0.75V _{CC}		
V _{IH}	Input Voltage	2.30 to 5.50		0.70V _{CC}			$0.70V_{CC}$		V
	LOW Level Control	1.65 to 1.95				$0.25V_{CC}$		$0.25V_{CC}$	N
V _{IL}	Input Voltage	2.30 to 5.50				$0.30V_{CC}$		0.30V _{cc}	V
		1.65		1.55	1.65		1.55		
		2.30	V _{IN} =V _{IH} ,	2.20	2.30		2.20		
	3.00	3.00	I _{он} =-100µА	2.90	3.00		2.90		
		4.50		4.40	4.50		4.40		
V _{OH}	HIGH Level Output	1.65	I _{OH} =-4mA	1.29	1.52		1.29		V
	Voltage	2.30	I _{OH} =-8mA	1.90	2.15		1.90		
		3.00	I _{OH} =-16mA	2.40	2.80		2.40		
	3.00	I _{OH} =-24mA	2.30	2.68		2.30			
		4.50	I _{OH} =-32mA	3.80	4.20		3.80		
1		4.50				0.10		0.10	
		2.30	V _{IN} =V _{IH} ,			0.10		0.10	
		3.00	I _{oL} =100μA			0.10		0.10	
		4.50				0.10		0.10	
V _{OL}	LOW Level Control Output Voltage	1.65	I _{OL} =4mA		0.80	0.24		0.24	V
	Output Voltage	2.30	I _{oL} =8mA		0.10	0.30		0.30	
		3.00	I _{oL} =16mA		0.15	0.40		0.40	
		3.00	I _{OL} =24mA		0.22	0.55		0.55	
	4.50	I _{OL} =32mA		0.22	0.55		0.55		
I _{IN}	Input Leakage Current	0 to 5.5	$0 \leq V_{\text{IN}} \leq 5.5 V$			±0.1		±1.0	μA
I _{OFF}	Power Off Leakage Current	0	V _{IN} or V _{OUT} =5.5V			1		10	μA
I _{cc}	Quiescent Supply Current	1.65 to 5.50	V _{IN} =5.5V, GND			1		10	μA

.				Т	_A =+25°	С	T _A =-40	to +85°C		
Symbol	Parameter	Vcc	Conditions	Min.	Тур.	Max.	Min.	Max.	Units	Figure
		1.80 ± 0.15		75			75			
		2.50 ± 0.20	C _L =15pF	150			150			
	Maximum Clock	3.30 ± 0.30	$R_D = 1M\Omega$ S ₁ =Open	200			200			Figure 4
f_{MAX}	Frequency	5.00 ± 0.50		250			250		1	Figure 8
		3.30 ± 0.50	C _L =50pF	175			175			
	5.00 ± 0.50	$R_D = 500\Omega$, S ₁ =Open	200			200				
		1.80 ± 0.15		2.5	6.5	12.5	2.5	13.0		
		2.50 ± 0.20	C _L =15pF,	1.5	3.8	7.5	1.5	8.0	ĺ	
	t _{PHL} Propagation Delay CK to Q, /Q	3.30 ± 0.30	R _D =1MΩ S₁=Open	1.0	2.8	6.5	1.0	7.0		Figure 4
t_{PLH}, t_{PHL}		5.00 ± 0.50		0.8	2.2	4.5	0.8	5.0	ns	Figure 6
		3.30 ± 0.30	C _L =50pF	1.0	3.4	7.0	1.0	7.5		1.90.00
		5.00 ± 0.50	R _D =500Ω, S₁=Open	1.0	2.6	5.0	1.0	5.5		
		1.80 ± 0.15		2.5	6.5	14.0	2.5	14.5		
	Descention Dates	2.50 ± 0.20	C _L =15pF,	1.5	3.8	9.0	1.5	9.5		
		3.30 ± 0.30	R _L =1MΩ S₁=Open	1.0	2.8	6.5	1.0	7.0		Eiguro
t _{PLH} , t _{PHL} Propagation Dela /CLR, /PR to Q, /	/CLR, /PR to Q, /Q	5.00 ± 0.50		0.8	2.2	5.0	0.8	5.5	ns	Figure 4 Figure 6
	· , · · · · , ·	3.30 ± 0.30	C _L =50pF,	1.0	3.4	7.0	1.0	7.5		i iguro c
		5.00± 0.50	$R_D = 500\Omega \Im$ S ₁ =Open	1.0	2.6	5.0	1.0	5.5		
	1.80 ± 0.15		6.5			6.5				
		2.50 ± 0.20	C _L =15pF,	3.5			3.5			Figure 4
		3.30 ± 0.30	R _L =1MΩ S₁=Open	2.0			2.0			
ts	Setup Time CK to D	5.00 ± 0.50		1.5			1.5		ns	Figure 4 Figure 7
		3.30 ± 0.30	C _L =50pF,	2.0			2.0			Ű
		5.00± 0.50	R _D =500Ω∍ S₁=Open	1.5			1.5			
		1.80 ± 0.15		0.5			0.5			
		2.50 ± 0.20	C _L =15pF,	0.5			0.5			
		3.30 ± 0.30	$R_L=1M\Omega$ S ₁ =Open	0.5			0.5			Figure 4
t _H	Hold Time, CK to D	5.00 ± 0.50		0.5			0.5		ns	Figure 4 Figure 7
		3.30 ± 0.30	C _L =50pF,	0.5			0.5			ga. e .
		5.00± 0.50	R _D =500Ω∋ S₁=Open	0.5			0.5			
		1.80 ± 0.15		6.0			6.0			
		2.50 ± 0.20	C _L =15pF,	4.0			4.0			
		3.30 ± 0.30	R _L =1MΩ S₁=Open	3.0			3.0			
tw	Pulse Width, CK, /PR, /CLR	5.00 ± 0.50		2.0			2.0		ns	Figure 4 Figure 8
		3.30 ± 0.30	C _L =50pF,	3.0			3.0			i igui e c
		5.00± 0.50	R _D =500Ω∍ S₁=Open	2.0			2.0			
		1.80 ± 0.15	S, Spon	8.0			8.0			
		2.50 ± 0.20	C _L =15pF,	4.5			4.5			
		3.30 ± 0.30	$R_L=1M\Omega$	3.0			3.0			-
t _{REC}	Recover Time /CLR, /PR to CK	5.00 ± 0.50	S₁=Open	3.0			3.0		ns	Figure 4 Figure 7
		3.30 ± 0.30	C _L =50pF,	3.0			3.0			. iguic /
		5.00 ± 0.50	R _D =500Ω∍ S₁=Open	3.0	1	1	3.0	1	ł	

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C. una la cal	Deverseter	V	Conditions	т	_=+25°	C	T _A =-40	to +85°C	l lusite	F :	
Symbol	Parameter	¥ CC	Vcc	Conditions	Min.	Тур.	Min.	Тур.	Min.	Units	Figure
CIN	Input Capacitance	0			3				pF		
C _{OUT}	Output Capacitance	0			4				pF		
0	Power Dissipation	3.30			10						
CPD	O and a the set of (2)								pF		
Note: 2. C _{PD} is curre	Capacitance ⁽²⁾ s defined as the value ont consumption (I _{CCD} ating current by the e) at no outp	ut loading and o	perating	at 50%		/cle. C _{PD} i				
Note: 2. C _{PD} is curre	s defined as the value	e of the inte) at no outp	ut loading and o	perating	nce whi at 50%						
Note: 2. C _{PD} is curre	s defined as the value	e of the inte) at no outp	ut loading and o	perating	nce whi at 50%		/cle. C _{PD} i				

Note:

3. C_L includes load and stray capacitance. Input PRR=1.0MHz t_w=500ns.



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D Input

- 4. CP input=AC Waveforms t_r=t_f=2.5ns.
- 5. CP input PRR=10MHz; Duty Cycle=50%.
- 6. D input PRR=5MHz; Duty Cycle=50%.
 - Figure 5. ICCD Test Circuit

-

Q Output







Physical Dimensions



A



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.
- E. FILE DRAWING NAME : MKT-MAB08Arev4





Figure 9. 8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: <u>http://www.fairchildsemi.com/products/analog/pdf/sc70-5_tr.pdf</u>.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
K8X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data, supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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