Ci522

13.56MHz reader/writer for contactless communication

1 Introduction

This document describes the functionality and electrical characteristics of the contactless reader/writer Ci522.

2 General description

The Ci522 is a highly integrated reader/writer for contactless communication at 13.56 MHz. The Ci522 reader supports ISO/IEC 14443 A.

The Ci522's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443 A cards and transponders without additional active circuitry. The receiver module provides a robust and efficient implementation for demodulating and decoding signals from ISO/IEC 14443 A compatible cards and transponders. The digital module manages the complete ISO/IEC 14443 A framing and error detection (parity and CRC) functionality.

The Ci522 supports contactless communication.

SPI (Serial Peripheral Interface) host interfaces are provided.

Three packages are provided: QFN16、QFN20 and ESOP16.

Contents

3 Features and benefits

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers for connecting an antenna with the minimum number of external components
- Supports ISO/IEC 14443 A
- Typical operating distance in Read/Write mode up to 50 mm depending on the antenna size and tuning
- Supports ISO/IEC 14443 A with higher transmission rates communication, up to 848 kBd
- Supported SPI up to 10 Mbit/s
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power
- Power-down by software
- Programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- 2.3 V to 4.0 V power supply
- CRC coprocessor

4 Quick reference data

Table 4-1 Absolute Maximum Ratings

Conditions	Min	Max	Unit
Supply voltage			
VDD	2.3	4.0	V
Temperature			
Operating temperature	-40	+85	℃

Table 4-2 Quick Reference Data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
AVDD	Analog supply voltage	AVDD = VDD (PVDD) = VDD (TVDD); VSS = 0 V	(1)	2.3	3.3	4.0	V
VDD (PVDD)	PVDD supply voltage			2.3	3.3	4.0	V
VDD (TVDD)	TVDD supply voltage			2.3	3.3	4.0	V
Ipd	power-down current	AVDD=VDD（PVDD）=VDD(TVDD)= 3.3V					
		hard power-down; pin NRSTPD set LOW	(2)	-	0.9	2.5	uA
		soft power-down	(2)	-	1.5	1.5	uA
IPVDD	PVDD supply current	Pin VDD1 ； PVDD = 3.3 V		-	0.9	1.5	mA
IDDA	analog supply	Pin VDD4 ； VDDA = 3.3 V，CommandReg		-	2.9	4	mA

	current	register's RcvOff bit = 0					
		Pin VDD4；receiver switched off；VDDA = 3.3 V，CommandReg register's RcvOff bit = 1		-	0.8	1	mA
IDD (TVDD)	TVDD supply current	Pin VDD3；TVDD = 3.3 V	(3)	-	25	30	mA

1. *VDDA, VDD(PVDD) and VDD(TVDD) must always be the same voltage.*
2. *Ipd is the total current for all supplies.*
3. *During typical circuit operation, the overall current is below 30 mA.*

Table 4-3 Recommended Value

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AVDD	Analog supply voltage	AVDD=VDD（PVDD）=VDD(TVDD); VSS=0V	2.3	3.3	4.0	V
VDD(PVDD)	PVDD supply voltage		2.3	3.3	4.0	V
VDD(TVDD)	TVDD supply voltage		2.3	3.3	4.0	V
	Storage temperature	QFN32L	-55	-	+125	℃
	Operating temperature	QFN32L	-40	-	+85	℃

Note:Stresses beyond those Absolute Maximum Ratings may cause permanent damage to the device.

Table 4-4 Version information

Chip type	Description
Ci522	-

5 Block diagram

The analog interface manages the modulation and demodulation of the analog signals. The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host. The FIFO buffer ensures fast and convenient data transfers to/from the host and the contactless UART.

SPI is implemented to meet different users' requirements.

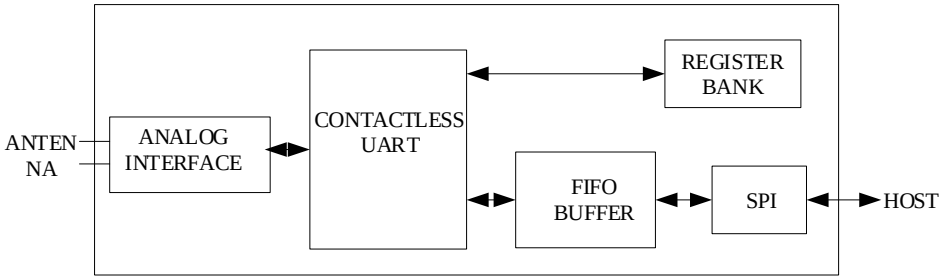
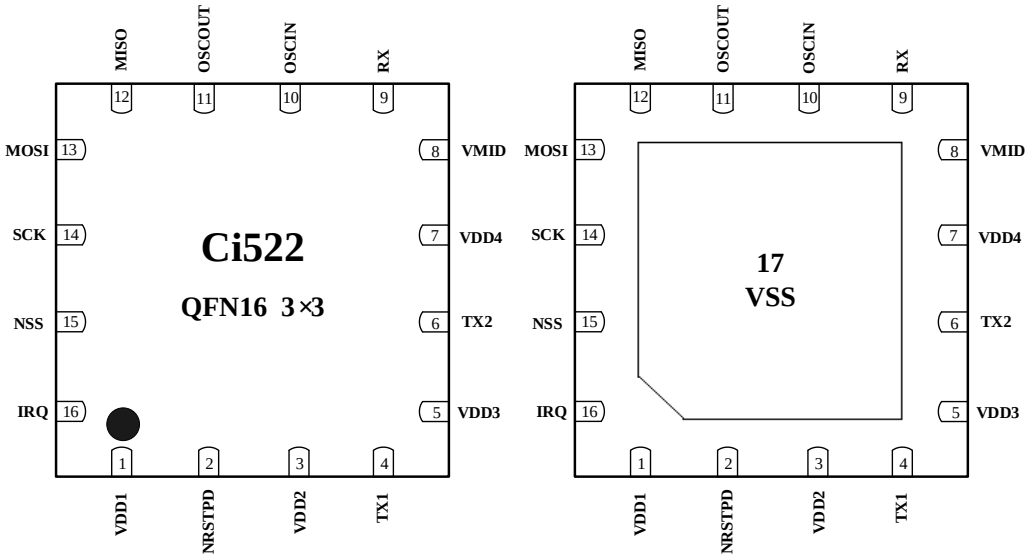


Figure 5-1 Simplified block diagram

6 Pinning information

6.1 QFN16 Package



(a)Top (b)Bottom

Figure 6-1 Pinning configuration (QFN16)

Table 6-1 Pin description

Pin	Symbol	Type[1]	Description
1	VDD1	P	Pad power supply
2	NRSTPD	I	Reset and power-down input: reset: enabled by a positive edge power-down: enabled when LOW; internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world
3	VDD2	P	Floating
4	TX1	O	Transmitter 1 delivers the modulated 13.56 MHz energy carrier
5	VDD3	P	Transmitter power supply: supplies the output stage of transmitters 1 and 2
6	TX2	O	Transmitter 2 delivers the modulated 13.56 MHz energy carrier

7	VDD4	P	Analog power supply
8	VMID	P	Internal reference voltage
9	RX	I	RF signal input
10	OSCIN	I	Crystal oscillator inverting amplifier input; also the input for an externally generated clock (fclk = 27.12 MHz)
11	OSCOUT	O	Crystal oscillator inverting amplifier output
12	MISO	O	SPI master in, slave out
13	MOSI	I	SPI master out, slave in
14	SCK	I	SPI serial clock input
15	NSS	I	SPI signal input
16	IRQ	O	Interrupt request output: indicates an interrupt event
17	VSS	G	Ground, connection of heatsink pad on package underside

Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground

6.2 ESOP16 Package

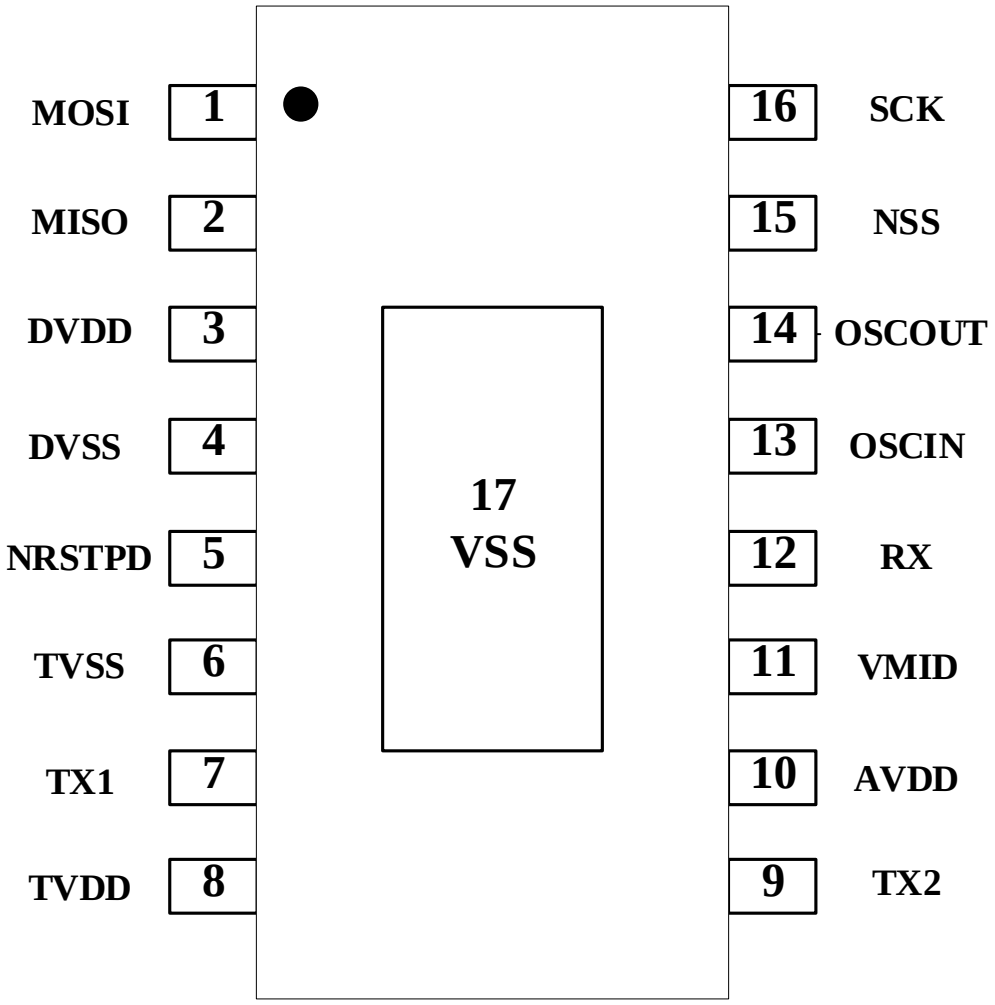


Figure 6-2 Pinning configuration (ESOP16)

Note：Pin 17 is VSS, it is the connection of heatsink pad on package underside.

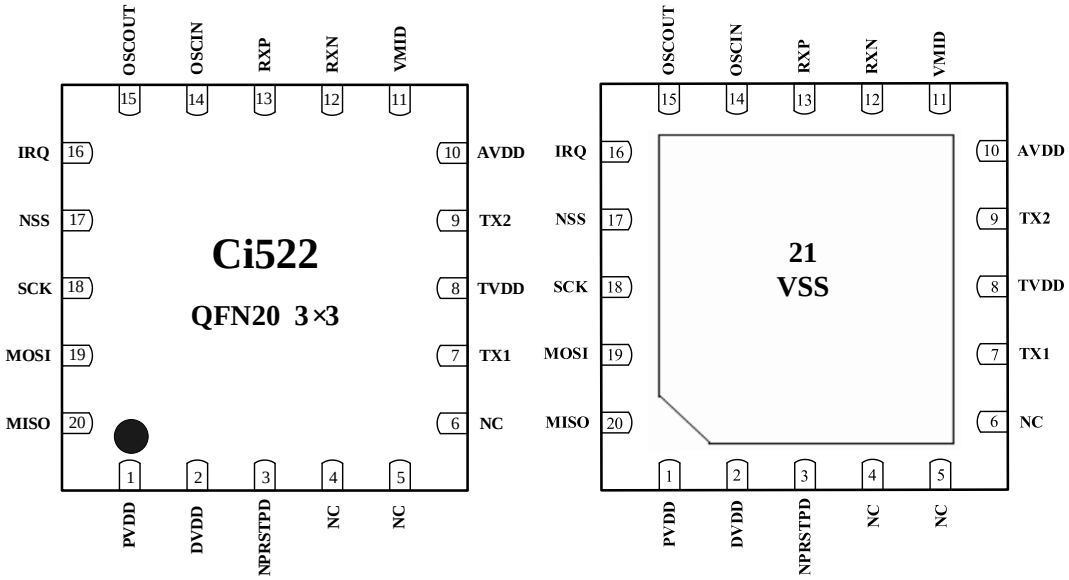
Table 6-2 Pin description

Pin	Symbol	Type[1]	Description
1	MOSI	I	SPI master out, slave in
2	MISO	O	SPI master in, slave out
3	DVDD	P	Digital power supply
4	DVSS	G	Digital ground
5	NRSTPD	I	Reset and power-down input: reset: enabled by a positive edge power-down: enabled when low; internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside

6	TVSS	G	Transmitter output stage 2 ground
7	TX1	O	Transmitter 1 delivers the modulated 13.56 MHz energy carrier
8	TVDD	P	Transmitter power supply: Supplies the output stage of transmitters 1 and 2
9	TX2	O	Transmitter 2 delivers the modulated 13.56 MHz energy carrier
10	AVDD	P	Analog power supply
11	VMID	P	Internal reference voltage
12	RX	I	Rf signal input
13	OSCIN	I	Crystal oscillator inverting amplifier input; also the input for an externally generated clock (fclk = 27.12 mhz)
14	OSCOUT	O	Crystal oscillator inverting amplifier output
15	NSS	I	SPI signal input
16	SCK	I	SPI serial clock input
17	VSS	G	Ground, connection of heatsink pad on package underside

Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground

6.3 QFN20 Package



(a)Top (b)Bottom

Figure 6-3 Pinning configuration (QFN20)

Table 6-3 Pin description

Pin	Symbol	Type[1]	Description
1	PVDD	P	Pad power supply
2	DVDD	P	Digital power supply
3	NRSTPD	I	Reset and power-down input: reset: enabled by a positive edge power-down: enabled when low; internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world
4	NC	—	—
5	NC	—	—
6	NC	—	—
7	TX1	O	Transmitter 1 delivers the modulated 13.56 MHz energy carrier
8	TVDD	P	Transmitter power supply: supplies the output stage of transmitters 1 and 2
9	TX2	O	Transmitter 2 delivers the modulated 13.56 MHz energy carrier
10	AVDD	P	Analog power supply
11	VMID	P	Internal reference voltage
12	RXN	I	RF signal input
13	RXP	I	RF signal input
14	OSCIN	I	Crystal oscillator inverting amplifier input; also the input for an externally generated clock (fclk = 27.12 MHz)
15	OSCOUT	O	Crystal oscillator inverting amplifier output
16	IRQ	O	Interrupt request output: indicates an interrupt event
17	NSS	I	SPI signal input
18	SCK	I	SPI serial clock input
19	MOSI	I	SPI master out, slave in

20	MISO	O	SPI master in, slave out
21	VSS	G	Ground，connection of heatsink pad on package underside

Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground

7 Functional description

The Ci522 transmission module supports ISO/IEC 14443 A and ISO/IEC 14443 A/B Read/Write mode at various transmission rates and modulation protocols.

Table 7 -1 Communication overview for ISO/IEC 14443 A reader/writer

Communication direction	Signal type	transmission rates			
		106kBd	212kBd	424kBd	848kBd
Reader to card (Ci522 sends data to a card)	reader side modulation	100% ASK	100% ASK	100% ASK	100% ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit length	128(13.56us)	64(13.56us)	32(13.56us)	16(13.56us)
Card to reader (card sends data to the Ci522)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56MHz/16	13.56MHz/16	13.56MHz/16	13.56MHz/16
	bit encoding	Manchester encoding	BPSK	BPSK	BPSK

The Ci522's contactless UART and dedicated external host must manage the ISO/IEC 14443 A protocol. Figure 7-1 shows the data coding and framing according to ISO/IEC 14443 A.

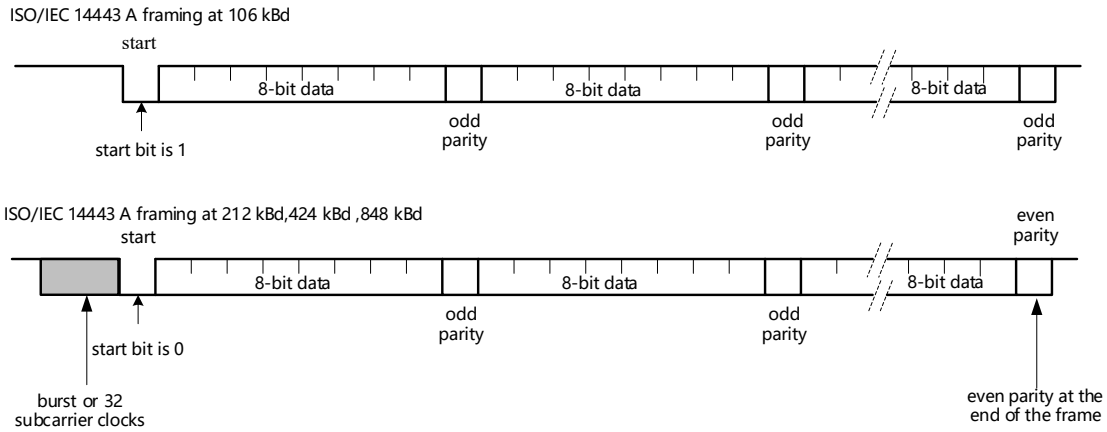


Figure 7-1 Data coding and framing according to ISO/IEC 14443 A

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally based on the transmission rates. Automatic parity generation can be switched off using the MfRxReg register's ParityDisable bit.

7.1 Digital interfaces

7.1.1 Serial Peripheral Interface

A Serial Peripheral Interface (SPI compatible) is supported and enables high-speed communication with the host. The interface can manage data speeds up to 10 Mbit/s. When communicating with a host, the Ci522 acts as a slave, receiving data from the external host for register settings, sending and receiving data relevant for RF interface communication. An interface compatible with SPI enables high-speed serial communication between the Ci522 and a microcontroller. The implemented interface is in accordance with the SPI standard.

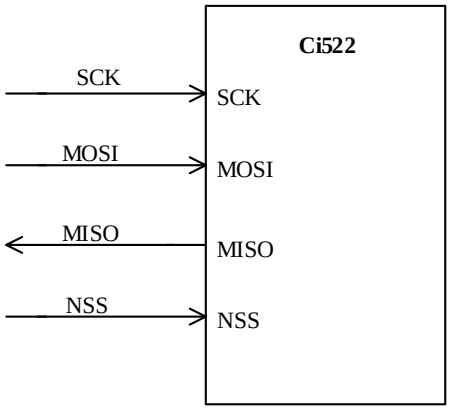


Figure 7-2 SPI connection to host

The Ci522 acts as a slave during SPI communication and is timed using the SPI clock signal (SCK) generated by the master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the Ci522 to the master. Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge. Data is sent by the Ci522 on the falling clock edge and is stable during the rising clock edge.

7.1.2 SPI read data

Reading data using SPI requires the byte order shown in Table 7-3 to be used. It is possible to read out up to n-data bytes.The read timing is shown in Figure 7-3.

Table 7-2 MOSI and MISO byte order

Line	Byte0	Byte1	Byte2	To	Byte n	Byte n+1
MOSI	address 0	address 1	address 2	…	address n	00
MISO	X	data 0	data 1	…	data n-1	data n

NOTE: The MSB must be sent first.

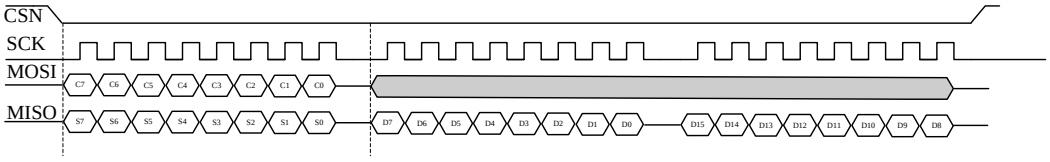


Figure 7-3 SPI read timing

7.1.3 SPI write data

To write data to the Ci522 using SPI requires the byte order shown in Table 7-4. It is possible to write up to n-data bytes by only sending one address byte. The first send byte defines both the mode and the address byte.The write timing is shown in Figure 7-4.

Table 7-3 MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n+1
MOSI	address 0	data 0	data 1	…	data n-1	data n
MISO	X	X	X	…	X	X

NOTE: The MSB must be sent first.

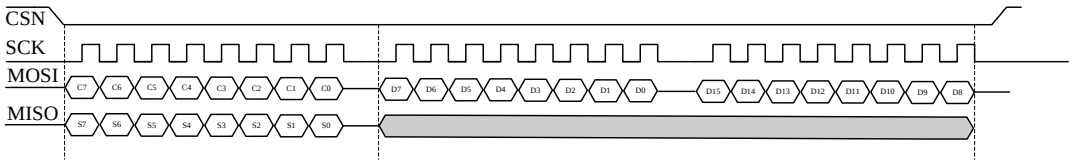


Figure 7-4 SPI write timing

7.1.4 SPI typical timing

SPI typical timing is shown in Figure 7-5 and SPI typical timing parameter is shown in Table 7-5.

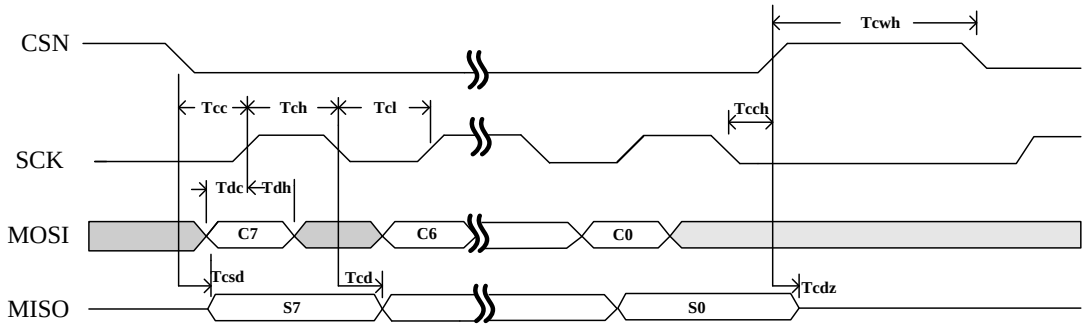


Figure 7-5 SPI typical timing

Table 7-4 SPI typical timing parameter

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns

Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		42	ns
Tcd	SCK to Data Valid		58	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	10	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		42	ns

7.1.5 SPI Read and Write address byte

The read address byte must meet the following criteria:the Most Significant Bit (MSB) of the first byte sets the mode. To read data from the Ci522, the MSB is set to logic 1; bits [6:1] define the address; the Least Significant Bit (LSB) should be set to logic 0.

Table 7-5 SPI read and write address

7(MSB)	6：1	0(LSB)
1：read/0：write	address	0

7.2 FIFO buffer

An 64x8 bit FIFO buffer is used in the Ci522. It buffers the input and output data stream between the host and the Ci522’s internal state machine. This makes it possible to manage data streams up to 64 bytes long without the need to take timing constraints into account.

The FIFO buffer input and output data bus is connected to the FIFODataReg register. Writing to this register stores one byte in the FIFO buffer and increments the

internal FIFO buffer write pointer. Reading from this register shows the FIFO buffer contents stored in the FIFO buffer read pointer and decrements the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the FIFOLevelReg register.

The Ci522 can generate two interrupts signal to know the condition of the FIFO buffer in time: HiAlertIRq 和 LoAlertIRq.

If the maximum number of WaterLevel[5:0] bits (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the HiAlert bit is set to logic 1. If it enables interrupt,the HiAlertIRq will be generated.

$$HiAlert = (64 - FIFOLength) \leq WaterLevel$$

If the number of WaterLevel[5:0] bits (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the LoAlert bit is set to logic 1.If it enables interrupt,the LoAlertIRq will be generated.

$$LoAlert = FIFOLength \leq WaterLevel$$

7.3 Interrupt request system

The Ci522 indicates certain events by setting the Status1Reg register's IRq bit and, if activated, by pin IRQ. The signal on pin IRQ can be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

Table 7-6 Interrupt sources

Interrupt flag	Interrupt source	Trigger action
TimerIRq	timer unit	the timer counts from 1 to 0
TxIRq	transmitter	a transmitted data stream ends
CRCIRq	CRC coprocessor	all data from the FIFO buffer has been processed
RxIRq	receiver	a received data stream ends
IdleIRq	ComIrqReg register	command execution finishes

HiAlertIRq	FIFO buffer	the FIFO buffer is almost full
LoAlertIRq	FIFO buffer	the FIFO buffer is almost empty
ErrIRq	contactless UART	an error is detected

7.4 Power reduction modes

7.4.1 Hard power-down

Hard power-down mode is enabled when pin NRSTPD is LOW. After exiting hard power-down mode, all registers will be reset.

7.4.2 Soft power-down

Soft power-down mode is entered immediately after the CommandReg register's PowerDown bit is set to logic 1. After exiting soft power-down mode, all registers will keep their values.

7.4.3 Transmitter Power-down

The Transmitter Power-down mode switches off the internal antenna drivers and the RF field. Transmitter Power-down mode is entered by setting either the TxControlReg register's Tx1RFEn bit or Tx2RFEn bit to logic 0.

8 Ci522 command set

8.1 General description

The Ci522 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code to the CommandReg register.

8.2 General behavior

• Each command that needs a data bit stream (or data byte stream) as an input immediately processes any data in the FIFO buffer. An exception to this rule is the Transceive command. Using this command, transmission is started with the BitFramingReg register's StartSend bit.

• Each command that needs a certain number of arguments, starts processing only when it has received the correct number of arguments from the FIFO buffer.

• The FIFO buffer is not automatically cleared when commands start. This makes it possible to write command arguments and/or the data bytes to the FIFO buffer and then start the command.

• Each command can be interrupted by the host writing a new command code to the CommandReg register, for example, the Idle command.

8.3 Ci522 command overview

Table 8-1 Command overview

Command	Command code	Action
Idle	0000	no action, cancels current command execution
Mem	0001	stores 25 bytes into the internal buffer
Generate RandomID	0010	generates a 10-byte random ID number
CalcCRC	0011	activates the CRC coprocessor or performs a self-test
Transmit	0100	transmits data from the FIFO buffer
NoCmdChange	0111	no command change, can be used to modify the CommandReg register bits without affecting the command, for example, the PowerDown bit
Receive	1000	activates the receiver circuits
Transceive	1100	transmits data from FIFO buffer to antenna and automatically activates the receiver after transmission
SoftReset	1111	resets Ci522

9 Ci522 register overview

Table 9-1 Ci522 register overview

Address (Hex)	Mnemonic	Bit	Type	Reset Value	Description
00h	reserved			00h	reserved for future use
01h	CommandReg			20h	starts and stops command execution
	reserved	7:6	R/W		write 0 by default
	RcvOff	5	R/W		1: analog part of the receiver is switched off
	PowerDown	4	D		1: Soft Power-down mode entered 0: Ci522 starts the wake up procedure during which this bit is read as a logic 1; it is read as a logic 0 when the Ci522 is ready NOTE: The PowerDown bit cannot be set when the SoftReset command is activated
	Command[3:0]	3:0	D		activates a command based on the Command value; reading this register shows which command is executed
02h	ComIEnReg			80h	enable and disable interrupt request control bits
	IRqInv	7	R/W		1：signal on pin IRQ is inverted with respect to the Status1Reg register’s IRq bit 0：signal on pin IRQ is equal to the IRq bit; in combination with the DivIEnReg register’s IRqPushPull bit, the default value of logic 1 ensures that the output level on pin IRQ is 3-state

	TxIEn	6	R/W		1: allows the transmitter interrupt request (TxIRq bit) to be propagated to pin IRQ
	RxIEn	5	R/W		1：allows the receiver interrupt request (RxIRq bit) to be propagated to pin IRQ
	IdleEn	4	R/W		1：allows the idle interrupt request (IdleIRq bit) to be propagated to pin IRQ
	HiAlertIEn	3	R/W		1：allows the high alert interrupt request (HiAlertIRq bit) to be propagated to pin IRQ
	LoAlertIEn	2	R/W		1：allows the low alert interrupt request (LoAlertIRq bit) to be propagated to pin IRQ
	ErrIEn	1	R/W		1：allows the error interrupt request (ErrIRq bit) to be propagated to pin IRQ
	TimerIEn	0	R/W		1：allows the timer interrupt request (TimerIRq bit) to be propagated to pin IRQ
03h	DivIEnReg			00h	enable and disable interrupt request control bits
	IRQPushPull	7	R/W		1：pin IRQ is a standard CMOS output pin 0：pin IRQ is an open-drain output pin
	reserved	6:3	R/W		write 0 by default
	CRCIEn	2	R/W		1: allows the CRC interrupt request, indicated by the DivIrqReg register's CRCIRq bit, to be propagated to pin IRQ
	reserved	1:0	-		reserved for future use
04h	ComIrqReg			14h	interrupt request bits
	Set1	7	W		1: indicates that the marked bits in the ComIrqReg register are set

					0: indicates that the marked bits in the ComIrqReg register are cleared
	TxIRq	6	D		1: set immediately after the last bit of the transmitted data was sent out
	RxIRq	5	D		1: receiver has detected the end of a valid data stream if the RxModeReg register's RxNoErr bit is set to logic 1, the RxIRq bit is only set to logic 1 when data bytes are available in the FIFO
	IdleIRq	4	D		1: if a command terminates, for example, when the CommandReg changes its value from any command to the Idle command; if an unknown command is started, the CommandReg register Command[3:0] value changes to the idle state and the IdleIRq bit is set; if the microcontroller starting the Idle command does not set the IdleIRq bit
	HiAlertIRq	3	D		1：the Status1Reg register's HiAlert bit is set the HiAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
	LoAlertIRq	2	D		1: Status1Reg register's LoAlert bit is set the LoAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
	ErrIRq	1	D		1: any error bit in the ErrorReg register is set

	TimerIRq	0	D		1: the timer decrements the timer value in register TCounterValReg to zero
05h	DivIrqReg			x0h	interrupt request bits
	Set2	7	W		1：indicates that the marked bits in the DivIrqReg register are set 0：indicates that the marked bits in the DivIrqReg register are cleared
	reserved	6:3	D		reserved for future use
	CRCIRq	2	D		1：the CalcCRC command is active and all data is processed
	reserved	1:0	-		reserved for future use
06h	ErrorReg			00h	error bits showing the error status of the last command executed
	WrErr	7	R		1：data is written into the FIFO buffer by the host if data is written into the FIFO buffer by the host during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface
	TempErr	6	R		1: internal temperature sensor detects overheating, in which case the antenna drivers are automatically switched off
	reserved	5	-		reserved for future use
	BufferOvfl	4	R		1：the host or a Ci522's internal state machine (e.g. receiver) tries to write data to the FIFO buffer even though it is already full
	CollErr	3	R		1：a bit-collision is detected cleared automatically at receiver start-up

					phase only valid during the bitwise anticollision at 106 kBd always set to logic 0 during communication protocols at 212 kBd, 424 kBd and 848 kBd
	CRCErr	2	R		1:the RxModeReg register's RxCRCEn bit is set and the CRC calculation fails automatically cleared to logic 0 during receiver start-up phase
	ParityErr	1	R		1：parity check failed automatically cleared during receiver start-up phase only valid for ISO/IEC 14443 A communication at 106 kBd
	ProtocolErr	0	R		1：SOF is incorrect automatically cleared during receiver start-up phase bit is only valid for 106 kBd
07h	Status1Reg			21h	communication status bits
	reserved	7	-		reserved for future use
	CRCOk	6	R		1：the CRC result is zero the CRCOk bit is undefined for data transmission and reception: use the ErrorReg register's CRCErr bit indicates the status of the CRC coprocessor, during calculation the value changes to logic 0, when the calculation is done correctly the value changes to logic 1
	CRCReady	5	R		1：the CRC calculation has finished; only valid for the CRC coprocessor calculation using the CalcCRC command

	IRq	4	R		indicates if any interrupt source requests attention with respect to the setting of the interrupt enable bits: see the ComIEnReg and DivIEnReg registers
	TRunning	3	R		1：MFRC523’s timer unit is running, i.e. the timer will decrement the TCounterValReg register with the next timer clock NOTE: in gated mode, the TRunning bit is set to logic 1 when the timer is enabled by TModeReg register’s TGated[1:0] bits; this bit is not influenced by the gated signal
	reserved	2	-		reserved for future use
	HiAlert	1	R		1：the alert level for the number of bytes in the FIFO buffer (FIFO Length[6:0]) is: HiAlert = (64-FIFOLength)≤WaterLevel Example: FIFO Length = 60, WaterLevel = 4 -> HiAlert = 1 FIFO Length = 59, WaterLevel = 4 -> HiAlert = 0
	LoAlert	0	R		1：the alert level for number of bytes in the FIFO buffer (FIFO Length[6:0]) is: LoAlert = FIFOLength≤WaterLevel Example： FIFO Length = 4, WaterLevel = 4 -> LoAlert = 1 FIFO Length = 5, WaterLevel = 4 ->

					LoAlert = 0
08h	Status2Reg			00h	receiver and transmitter status bits
	TempSensClear	7	R/W		1：clears the temperature error if the temperature is below the alarm limit of 125 ℃
	reserved	6:3	-		reserved
	ModemState [2:0]	2:0	R		shows the state of the transmitter and receiver state machines: 000：idle 001：wait for the BitFramingReg register's StartSend bit 010：TxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1. The minimum time for TxWait is defined by the TxWaitReg register 011：transmitting 100：RxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1. The minimum time for RxWait is defined by the RxWaitReg register 101：wait for data 110：receiving
09h	FIFODataReg			xxh	input and output of 64 byte FIFO buffer
	FIFOData[7:0]	7:0	D		data input and output port for the internal 64-byte FIFO buffer. FIFO buffer acts as parallel in/parallel out converter for all

					serial data stream inputs and outputs
0Ah	FIFOLevelReg			00h	number of bytes stored in the FIFO buffer
	FlushBuffer	7	W		1：immediately clears the internal FIFO buffer's read and write pointer and ErrorReg register's BufferOvfl bit. Reading this bit always returns 0
	FIFOLevel[6:0]	6:0	R		indicates the number of bytes stored in the FIFO buffer. Writing to the FIFODataReg register increments and reading decrements the FIFOLevel value
0Bh	WaterLevelReg			08h	level for FIFO underflow and overflow warning
	reserved	7:6	-		reserved for future use
	WaterLevel[5:0]	6:0	R/W		defines a warning level to indicate a FIFO buffer overflow or underflow: Status1Reg register's HiAlert bit is set to logic 1 if the remaining number of bytes in the FIFO buffer space is equal to, or less than the defined number of WaterLevel[5:0] bits Status1Reg register's LoAlert bit is set to logic 1 if equal to, or less than the WaterLevel[5:0] bits in the FIFO buffer
0Ch	ControlReg			10h	miscellaneous control registers
	TStopNow	7	W		1：timer stops immediately Reading this bit always returns it to 0
	TStartNow	6	W		1：timer starts immediately. Reading this bit always returns it to 0

	reserved	5:3	-		reserved for future use
	RxLastBits[2:0]	2:0	R		indicates the number of valid bits in the last received byte. If this value is zero, the whole byte is valid
0Dh	BitFramingReg			00h	adjustments for bit-oriented frames
	StartSend	7	W		1：starts the transmission of data only valid in combination with the Transceive command
	RxAlign[2:0]	6:4	R/W		used for reception of bit-oriented frames: defines the bit position for the first bit received to be stored in the FIFO buffer example: 0：LSB of the received bit is stored at bit position 0, the second received bit is stored at bit position 1 1：LSB of the received bit is stored at bit position 1, the second received bit is stored at bit position 2 7：LSB of the received bit is stored at bit position 7, the second received bit is stored in the next byte that follows at bit position 0 these bits are only to be used for bitwise anticollision at 106 kBd, for all other modes they are set to 0
	reserved	3	-		reserved for future use
	TxLastBits[2:0]	2:0	R/W		used for transmission of bit oriented frames: defines the number of bits of the

					last byte that will be transmitted. 000b indicates that all bits of the last byte will be transmitted
0Eh	CollReg			xxh	bit position of the first bit-collision detected on the RF interface
	ValuesAfterColl	7	R/W		0：all received bits will be cleared after a collision only used during bitwise anticollision at 106 kBd, otherwise it is set to logic 1
	reserved	6	-		reserved for future use
	CollPosNotValid	5	R		1：no collision detected or the position of the collision is out of the range of CollPos[4:0]
	CollPos[4:0]	4:0	R		shows the bit position of the first detected collision in a received frame only data bits are interpreted example: 00h：indicates a bit-collision in the 32nd bit 01h：indicates a bit-collision in the 1st bit 08h：indicates a bit-collision in the 8th bit these bits will only be interpreted if the CollPosNotValid bit is set to logic 0
0Fh	reserved				reserved for future use
10h	reserved			00h	reserved for future use
11h	ModeReg			3Fh	defines general modes for transmitting and receiving
	MSBFirst	7	R/W		1：CRC coprocessor calculates the CRC with MSB first. In the CRCResultReg register the values for the

					CRCResultMSB[7:0] bits and the CRCResultLSB[7:0] bits are bit reversed NOTE: during RF communication this bit is ignored
	reserved	6	-		reserved for future use
	TXWaitRF	5	R/W		1：transmitter can only be started if an RF field is generated
	reserved	4:2	R/W		reserved for future use
	CRCPreset	1:0	R/W		defines the preset value for the CRC coprocessor for the CalcCRC command NOTE: during any communication, the preset values are selected automatically according to the definition of bits in the RxModeReg and TxModeReg registers 00：0000h 01：6363h 10：A671h 11：FFFFh
12h	TxModeReg			00h	defines transmission data rate and framing
	TxCRCEn	7	R/W		1：enables CRC generation during data transmission NOTE: it can only be set to logic 0 at 106 kBd
	TxSpeed[2:0]	6:4	D		defines the bit rate during data transmission. Ci522 handles transmission rates up to 848 kBd 000:106kBd 001:212kBd

					010:424kBd 011:848kBd 100-111：reserved
	InvMod	3	R/W		1：modulation of transmitted data is inverted
	reserved	2:0	R/W		reserved
13h	RxModeReg			00h	defines transmission data rate and framing
	RxCRCEn	7	R/W		1：enables CRC generation during data transmission NOTE: it can only be set to logic 0 at 106 kBd
	RxSpeed[2:0]	6:4	D		defines the bit rate during data transmission. Ci522 handles transmission rates up to 848 kBd 000:106kBd 001:212kBd 010:424kBd 011:848kBd 100-111：reserved
	RxNoErr	3	R/W		1：modulation of transmitted data is inverted
	RxMultiple	2	R/W		reserved
	reserved	1:0	R/W		defines transmission data rate and framing
14h	TxControlReg			80h	controls the antenna driver pins TX1 and TX2
	InvTx2RFOn	7	R/W		1：output signal on pin TX2 inverted when driver TX2 is enabled
	InvTx1RFOn	6	R/W		1：output signal on pin TX1 inverted when

					driver TX1 is enabled
	InvTx2RFOff	5	R/W		1：output signal on pin TX2 inverted when driver TX2 is disabled
	InvTx1RFOff	4	R/W		1：output signal on pin TX1 inverted when driver TX1 is disabled
	Tx2CW	3	R/W		1：output signal on pin TX2 continuously delivers the unmodulated 13.56 MHz energy carrier 0：Tx2CW bit is enabled to modulate the 13.56 MHz energy carrier
	reserved	2	-		reserved for future use
	Tx2RFEn	1	R/W		1：output signal on pin TX2 delivers the 13.56 MHz energy carrier modulated by the transmission data
	Tx1RFEn	0	R/W		1：output signal on pin TX1 delivers the 13.56 MHz energy carrier modulated by the transmission data
15h	TxASKReg			00h	controls the setting of the transmission modulation
	reserved	7	-		reserved for future use
	Force100ASK	6	R/W		1：forces 100 % ASK modulation independently of the ModGsPReg register setting
	reserved	5:0	-		reserved for future use
16h	TxSelReg			10h	selects the internal sources for the antenna driver
	reserved	7:6	-		reserved for future use
	DriverSel[1:0]	5:4	R/W		selects the input of drivers TX1 and TX2

					00：3-state; in soft power-down the drivers are only in 3-state mode if the DriverSel[1:0] value is set to 3-state mode 01：modulation signal (envelope) from the internal encoder, Miller pulse encoded 10：reserved 11：HIGH; the HIGH level depends on the setting of bits InvTx1RFOn/InvTx1RFOff and InvTx2RFOn/InvTx2RFOff
	reserved	3:0	R/W		reserved
17h	RxSelReg			84h	selects internal receiver settings
	UARTSel[1:0]	7:6	R/W		selects the input of the contactless UART 00：constant LOW 01: Manchester with subcarrier from pin MFIN 10: modulated signal from the internal analog module, default 11: reserved
	RxWait[5:0]	5:0	R/W		after data transmission the activation of the receiver is delayed for RxWait bit-clocks, during this ‘frame guard time’ any signal on pin RX is ignored this parameter is ignored by the Receive command all other commands, such as Transceive use this parameterthe counter starts immediately after the external RF field is switched on

18h	RxThresholdReg				selects thresholds for the bit decoder
	MinLevel[3:0]	7:4	R/W		defines the minimum signal strength at the decoder input that will be accepted. If the signal strength is below this level it is not evaluated
	reserved	7:4	-		reserved for future use
	CollLevel[2:0]	3:0	R/W		defines the minimum signal strength at the decoder input that must be reached by the weaker half-bit of the Manchester encoded signal to generate a bit-collision relative to the amplitude of the stronger half-bit
19h	DemodReg				defines demodulator settings
	AddIQ[1:0]	7:6	R/W		defines the use of I-channel and Q-channel during reception NOTE: the FixIQ bit must be set to logic 0 to enable the following settings: 00：selects the stronger channel 01：selects the stronger channel and freezes the selected channel during communication 10：reserved 11：reserved
	FixIQ	5	R/W		1：if the bits of AddIQ are set to X0, the reception is fixed to I-channel if the bits of AddIQ are set to X1, the reception is fixed to Q-channel
	TPrescalEven	4	R/W		set the frequency mode
	TauRcv[1:0]	3:2	R/W		changes the time-constant of the internal PLL during data reception

	TauSync[1:0]	1:0	R/W		changes the time constant of the internal PLL during burst
1Ah	reserved			00h	reserved for future use
1Bh	reserved			00h	reserved for future use
1Ch	MfTxReg			62h	controls communication transmit parameters
	reserved	7:2	-		reserved
	TxWait	1:0	R/W		defines the additional response time.
1Dh	MfRxReg			00h	controls communication receive parameters
	reserved	7:5	-		reserved for future use
	ParityDisable	4	R/W		1: generation of the parity bit for transmission and the parity check for receiving is switched off. The received parity bit is handled like a data bit
	reserved	3:0	-		reserved for future use
1Eh	reserved			00h	reserved for future use
1Fh	reserved			EBh	reserved for future use
20h	reserved			00h	reserved for future use
21h	CRCResultReg (higher bits)			FFh	shows the MSB and LSB values of the CRC calculation
	CRCResultMSB [7:0]	7:0	R		shows the value of the CRCResultReg register's most significant byte. Only valid if Status1Reg register's CRCReady bit is set to logic 1
22h	CRCResultReg (lower bits)			FFh	shows the MSB and LSB values of the CRC calculation

	CRCResultLSB [7:0]	7:0	R/W		shows the value of the least significant byte of the CRCResultReg register. Only valid if Status1Reg register's CRCReady bit is set to logic 1
23h	reserved			88h	reserved for future use
24h	ModeWidthReg			26h	controls the ModWidth setting
	ModWidth[7:0]	7:0	R/W		defines the width of the Miller modulation as multiples of the carrier frequency (ModWidth + 1 / fclk). The maximum value is half the bit period
25h	reserved			87h	reserved for future use
26h	RFCfgReg			48h	configures the receiver gain
	reserved	7	-		reserved for future use
	RxGain[2:0]	6:4	R/W		defines the receiver's signal voltage gain factor: 000：18dB 001：23dB 010：18dB 011：23dB 100：33dB 101：38dB 110：43dB 111：48dB
	reserved	3:0	-		reserved for future use
27h	GsNReg			88h	selects the conductance of the antenna driver pins TX1 and TX2 for modulation
28h	CWGsPReg			20h	defines the conductance of the p-driver output when not active

29h	ModGsPReg			20h	defines the conductance of the p-driver output during modulation
2Ah	TModeReg			00h	defines settings for the internal timer
	TAuto	7	R/W		1：the timer starts automatically at the end of the transmission in all communication modes at all speeds or when InvTxnRFOn bits are set to logic 1 and the RF field is switched on 0：indicates that the timer is not influenced by the protocol
	reserved	6:5			reserved for future use
	TAutoRestart	4	R/W		1：timer automatically restarts its count-down from the 16-bit timer reload value instead of counting down to zero 0：timer decrements to 0 and the ComIrqReg register's TimerIRq bit is set to logic 1
	TPrescaler_Hi [3:0]	3:0	R/W		defines the higher 4 bits of the TPrescaler value
2Bh	TPrescalerReg			00h	defines the lower 8 bits of the TPrescaler value
	TPrescaler_Lo [7:0]	7:0	R/W		defines the lower 8 bits of the TPrescaler value
2Ch	TReloadReg (higher bits)			00h	defines the 16-bit timer reload value
2Dh	TReloadReg (lower bits)			00h	defines the 16-bit timer reload value

2Eh	TCounterValReg (higher bits)			xxh	timer value higher 8 bits
2Fh	TCounterValReg (lower bits)			xxh	timer value lower 8 bits
30h~ 36h	RFT			00h	
37h	Version		R	92h	shows the software version

NOTE：R/W：Read/Write；D：Dynamic；R：Only Read；W：Only Write；

10 Application information

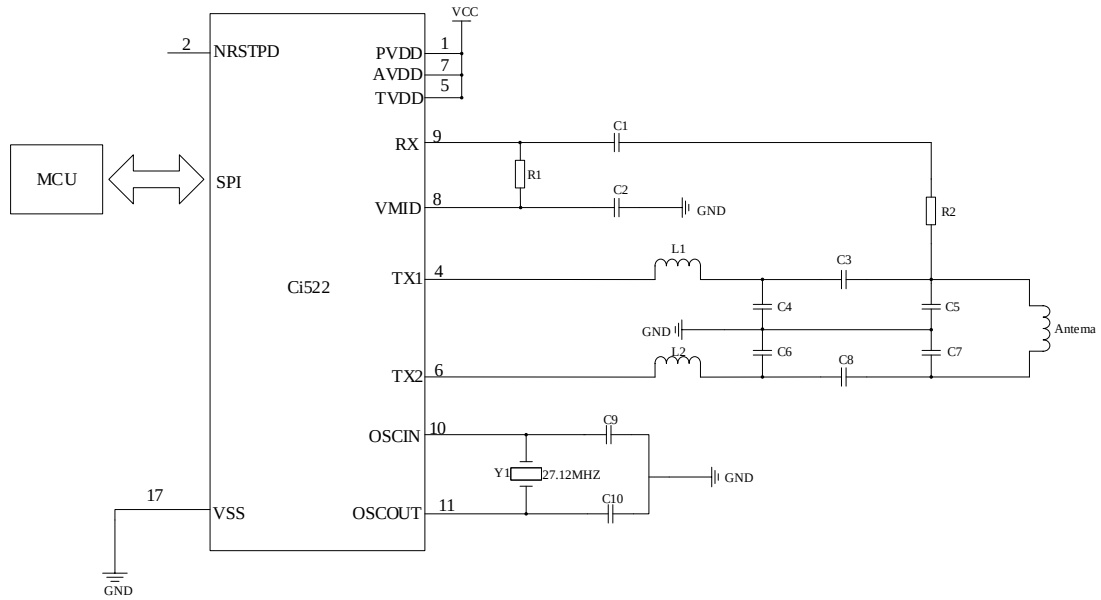


Figure 10-1 Typical application diagram 1

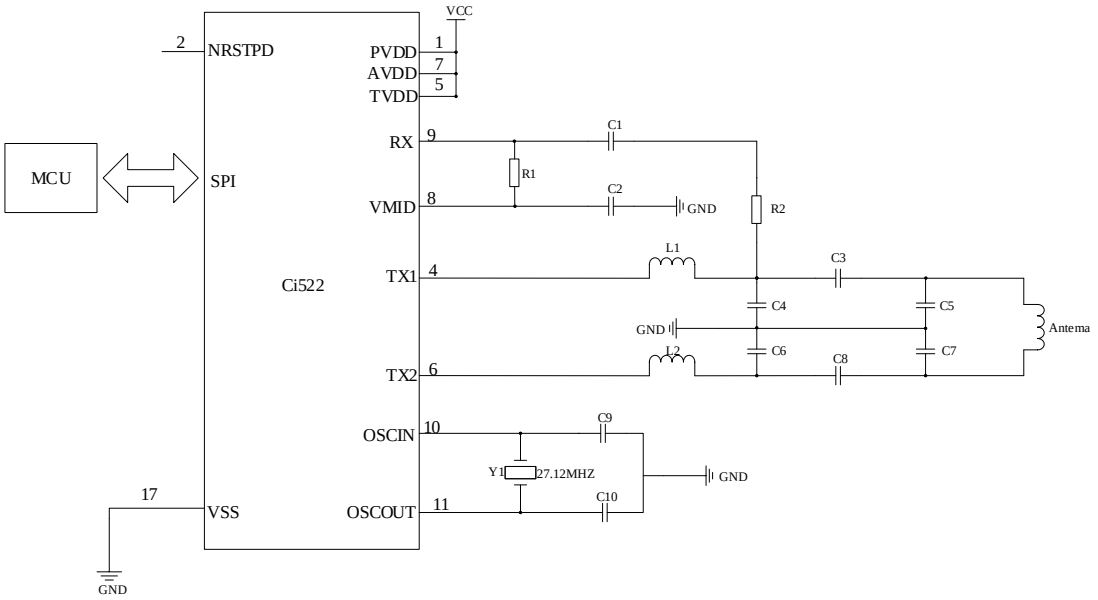


Figure 10-2 Typical application diagram 2

NOTE: When working with button batteries, it is recommended to add a 100μF large capacitor to the power supply;

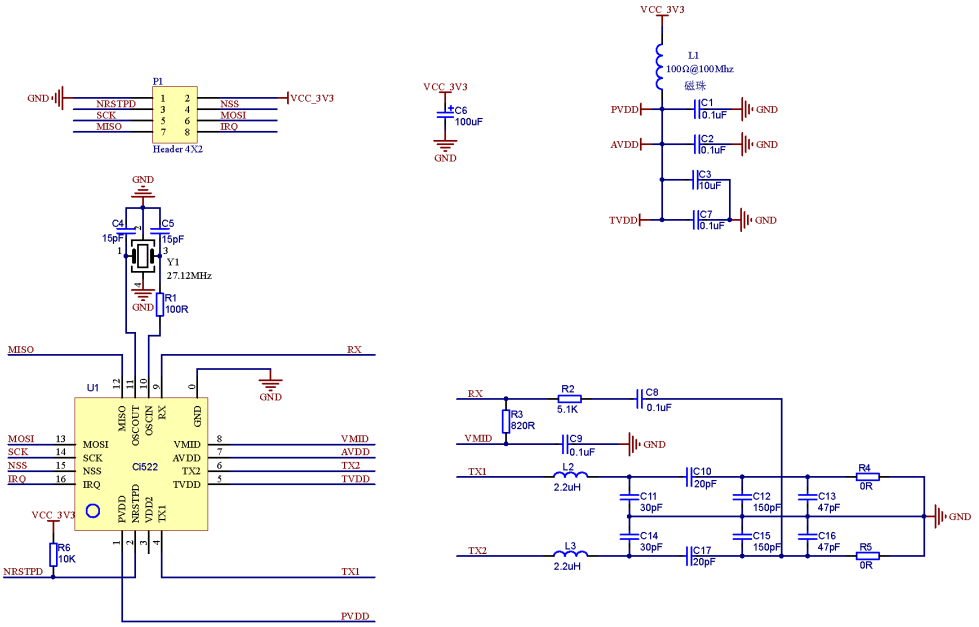


Figure 10-3 Typical application schematic diagram (QFN-16 package)

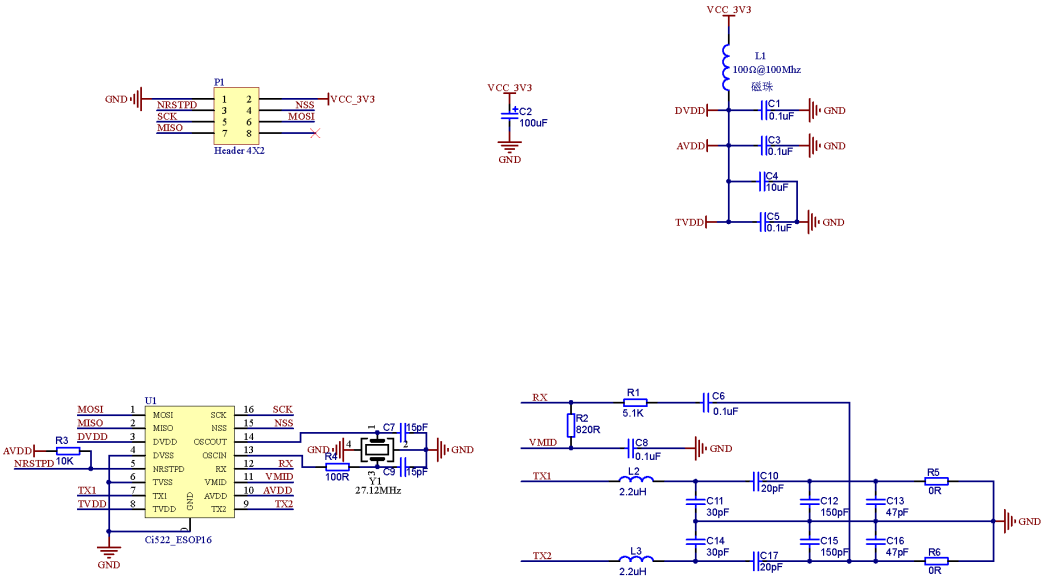


Figure 10-4 Typical application schematic diagram (ESOP-16 package)

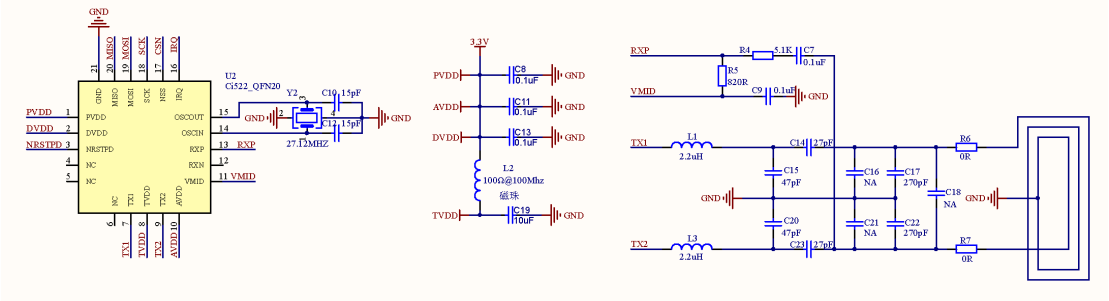


Figure 10-5 Typical application schematic diagram (QFN-20 package)

11 Package outline

11.1 QFN16 Package

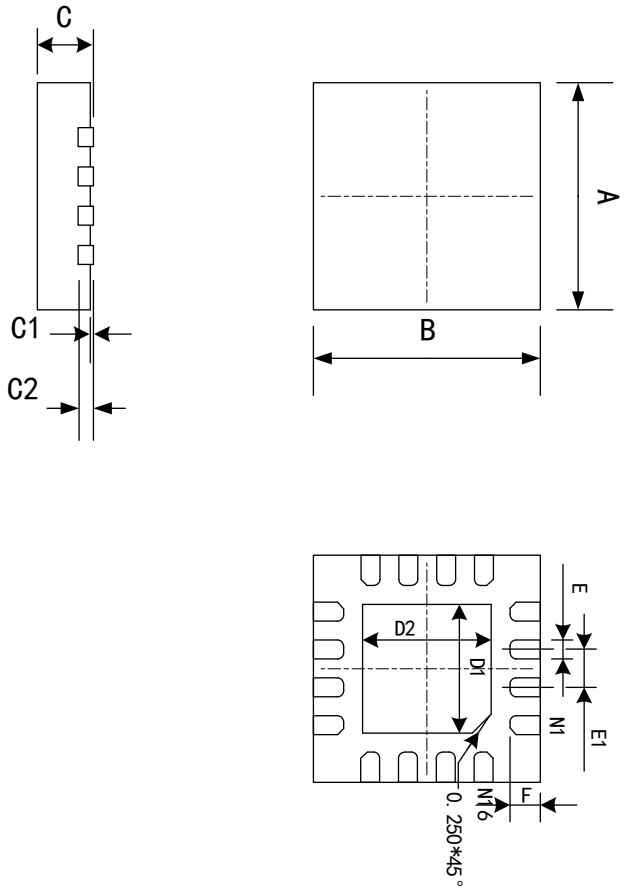


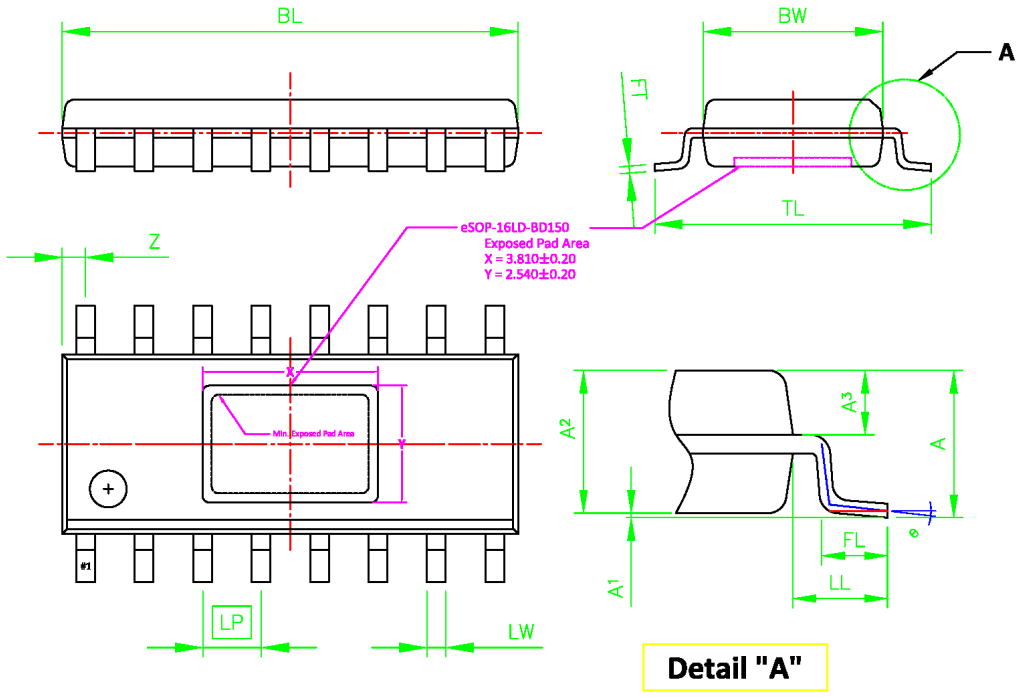
Figure 11-1 Package QFN16

Table 11-1 Package size

尺寸 / 标注	最小	最大	尺寸 / 标注	最小	最大
A	3.0±0.1		D1	1.70TYP	
B	3.0±0.1		D2	1.70TYP	
C	0.70	0.80	E	0.250TYP	
C1	0~0.050		E1	0.500TYP	
C2	0.203TYP		F	0.400TYP	

Unit：mm

11.2 ESOP16 Package



Dimensions

Unit	BL	BW	FT	TL	LP	LW	A	A1	A2	A3	LL	FL	θ	Z
mm	10.00 (9.90) 9.80	4.00 (3.90) 3.80	0.211 (0.203) 0.195	6.10 (6.00) 5.90	1.295 (1.270) 1.245	0.425 (0.400) 0.375	1.75 1.60	0.25 0.05	1.55 1.35	0.623 BSC	1.05 BSC	0.80 0.50	8 0	(0.50)

Notes:

1. All Dimensions are in Millimeters.

2. Dimensions Do Not include Burrs, Mold Flash, and Tie-bar Extrusions.

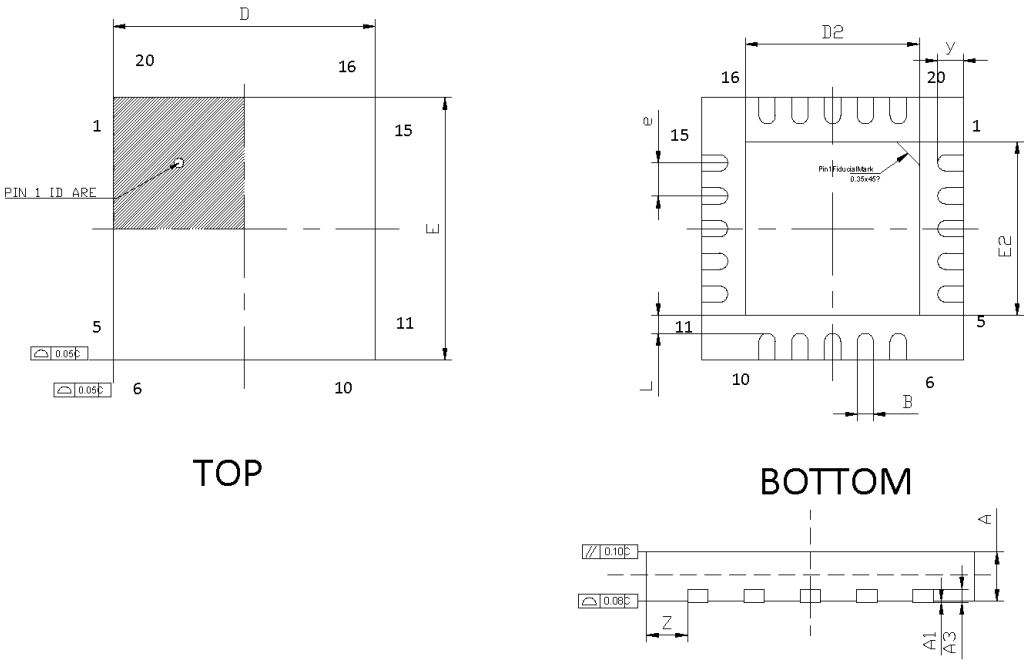
3. Diemnsions(LW) Do Not include Plating Thickness.

4. JEDEC References : MS-012

5. Mold Flash should Not be over 0.200mm per each side on the Exposed Pad.

Figure 11-2 Package ESOP16

11.3 QFN20 Package



Dimensions

Unit	D	E	D2	E2	A	A1	A3	B	e	K	L	y	Z
mm	3.025 (3.00) 2.975	3.025 (3.00) 2.975	1.65 (1.6) 1.55	1.65 (1.6) 1.55	0.80 (0.75) 0.70	0.05 (0.02) 0.00	0.203 REF	0.30 (0.25) 0.20	0.40 BSC	-	0.33 (0.28) 0.23	0.40 REF	0.655 REF

Notes

1.AllDimensionsareinMillimeters.
2.DimensionsDoNotincludeBurrs,MoldFlash,andTie-barExtrusions.

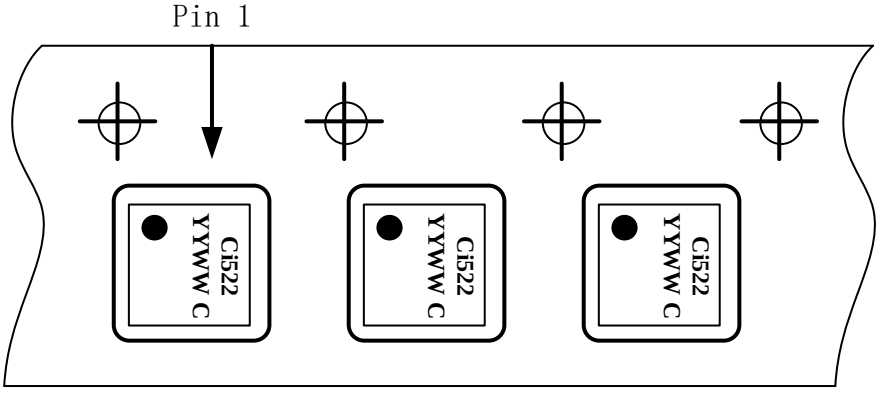


Figure 11-3 Package (QFN20)

12 Version information

Version	Modified date	Modified content
V1.0	2023/11/13	First draft
V1.1	2023/12/19	Modify Figure 7-2 SPI connection to host

13 Order Information

Package marking

Ci522 ABBCDEE

Ci522: chip code

A: package date code, 5 represents year 2020

BB: week of sending out processing, 42 represents in the year A the 42th week

C: package factory code, A、HT、NJ or WA, can also abbreviated as A、H、N or W

D: test factory code, A、Z or H

EE: production batch code

Table 15-1 Ci522 order example

order code	package	container	minimum
Ci522-Sample		Box/Tube	5
Ci522	3×3mm 16-pin QFN	Tape and reel	5K
Ci522	9.9×6.0mm 16-pin ESOP	Tape and reel	4K
Ci522	3×3mm 20-pin QFN	Tape and reel	5K

14 Technical Support and Contact Information

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