

80V Input, 4A Current Limit, Asynchronous Step-down Converter

Features

- 9V to 80V input voltage range
- 4A current limit
- 2A continuous load current
- 93% Peak Efficiency
- 400 μ A operating quiescent current
- 100V 400-m Ω high-side MOSFET
- Peak Current mode control
- 150/300KHz switching frequency
- Internal compensation for ease of use
- Up to 92% duty cycle
- 0.8V voltage reference
- 9 μ A shutdown current
- 150ms Hiccup mod short circuit protection Function
- Thermal shutdown Function
- Available in an ESOP8 package

Applications

- Appliances, power and garden tools
- High-cell-count battery packs (E-Bike, E-Scooter)
- Motor drives, drones, telecom
- Industrial Automation Control Vehicle Accessories
- Motor Control Vehicle Accessories

Description

The MST8820AXKP is a high voltage, Asynchronous step-down converter operates over a wide range input voltage 9V to 80V. The MST8820AXKP integrates a 100-V 400-m Ω high-side MOSFET.

The MST8820AXKP delivers 2A continuous load current with up to 93% efficiency. The MST8820AXKP operates with fixed frequency peak current control with built-in compensation eliminates the need for external components.

Cycle-by-cycle current limit in high-side MOSFET protects the converter in an overload condition. Hiccup mode protection is triggered if the over-current condition has persisted for longer than the present time.

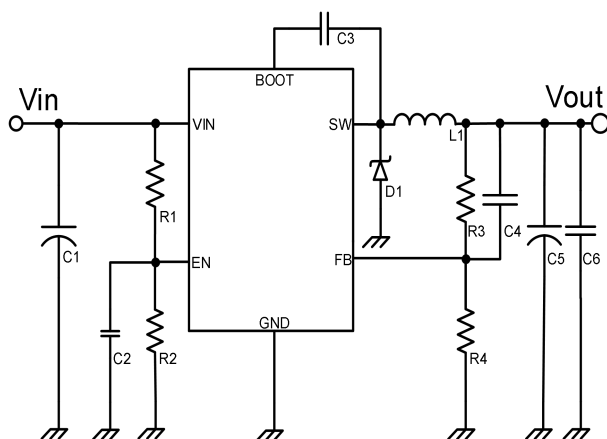
The MST8820AXKP exhibits protection features that protect the load from faults like under voltage, over-current and over-temperature.

The MST8820AXKP is available in an ESOP-8 package.

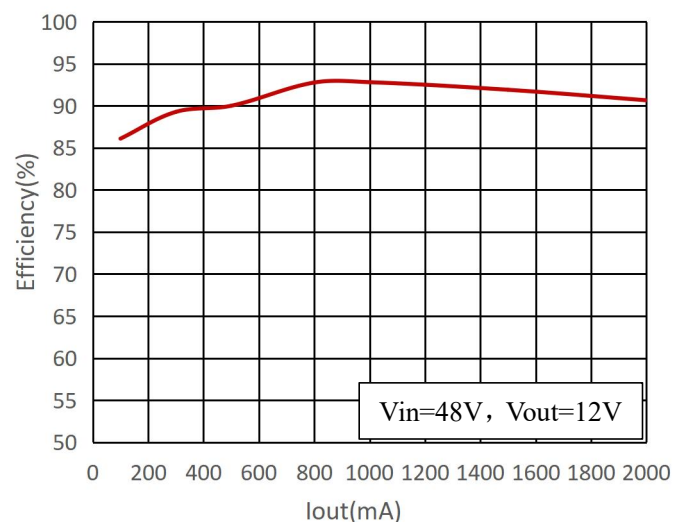
Device Information

PART NUMBER	PACKAGE	BODY SIZE(NOM)
MST8820AXKP	ESOP8	4.9mm*6.0mm

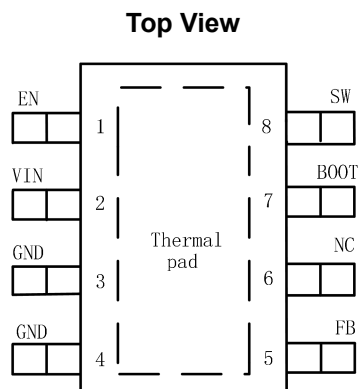
Typical Application



Efficiency



Pin Configuration and Functions



NO.	Name	Description
1	EN	Enable input. Pull EN below the specified threshold to shut down the MST8820AXKP. Pull EN above the specified threshold to enable the MST8820AXKP.
2	VIN	Input supply. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
3 , 4	GND	Ground. GND should be placed as close to the output capacitor as possible to avoid the high-current switch paths. Connect the exposed pad to GND plane for optimal thermal performance.
5	FB	Feedback. Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.
6	NC	No Connection
7	BOOT	Bootstrap. Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when SW voltage is low.
8	SW	Switch node. SW is the output from the high-side switch. A low forward voltage schottky rectifier to ground is required. The rectifier must be placed close to SW to reduce switching spikes.
9	Thermal Pad	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

Absolute Maximum Ratings

	Description	Min	Max	Unit
Input voltage	VIN to GND	-0.3	105	V
	EN to GND	-0.3	105	V
	FB to GND	-0.3	7	V
Output voltage	BOOT to GND	-0.3	105.5	V
	BOOT to SW	-0.3	5.5	V
	SW to GND	-0.3	105	V
T _{stg}	Storage Junction Temperature	-40	150	°C
T _{solder}	Lead Temperature (Soldering 10 sec.)	-40	150	°C

Note:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD Ratings

Item	Description	Range	Unit
V _{ESD}	Human Body Model(HBM)	2	KV
	Charged Device Model(CDM)	200	V

Note:

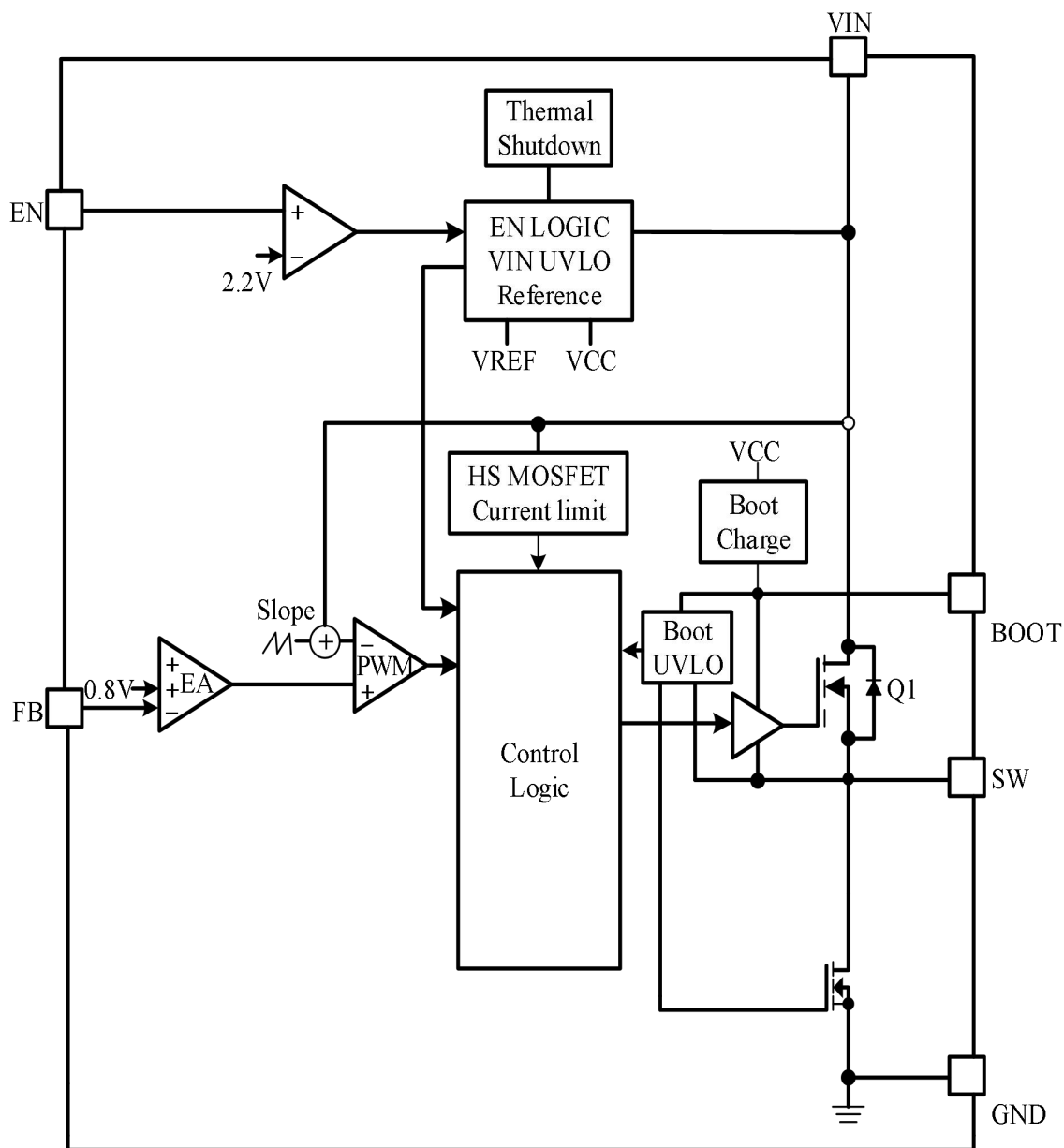
JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 200-V CDM allows safe manufacturing with a standard ESD control process.

Electrical Characteristics

(At $T_A=25^{\circ}\text{C}$, $V_{IN}=48\text{V}$, $V_{OUT}=5\text{V}$, Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VCC SUPPLY VOLTAGE						
V_{IN}	Operating Input Voltage		9	-	80	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising	-	8	-	V
$V_{UVLO(HY)}$	Input UVLO Hysteresis		-	0.3	-	V
I_{SHDN}	Shutdown Current from VIN pin	$V_{EN}=0\text{V}$, no load	-	9	-	μA
I_Q	Quiescent Current from VIN pin	$V_{FB}=1\text{V}$	-	500	-	μA
ENABLE						
V_{EN}	Enable threshold voltage		-	2.2	-	V
V_{EN_UVLO}	Enable threshold voltage Hysteresis		-	0.2	-	V
V_{EN_MAX}			80	-	-	V
FEEDBACK						
V_{FB}	FB Reference Threshold		-	0.8	-	V
$V_{FB\text{ (short)}}$	Feedback short voltage		-	0.35	-	V
V_{FB2}	Feedback short voltage Hysteresis		-	0.1	-	V
OSCILLATOR						
F_{OSC}	Switching frequency(A1)	$I_{OUT}=2\text{A}$	-	150	-	KHz
	Switching frequency(A3)	$I_{OUT}=2\text{A}$	-	300	-	KHz
D_{MAX}	Maximum Duty Cycle	$V_{IN}=12\text{V}$	-	92	-	%
CURRENT LIMIT						
I_{PEAK}	Current Limit Threshold		-	4	-	A
HIGH-SIDE MOSFET						
$R_{DS(on)}$	On-resistance	$V_{IN}=18\text{V}$	-	400	-	$\text{m}\Omega$
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown Temp		-	150	-	$^{\circ}\text{C}$
T_{SH}	Thermal shutdown Temp Hysteresis		-	30	-	$^{\circ}\text{C}$

Functional Block Diagram



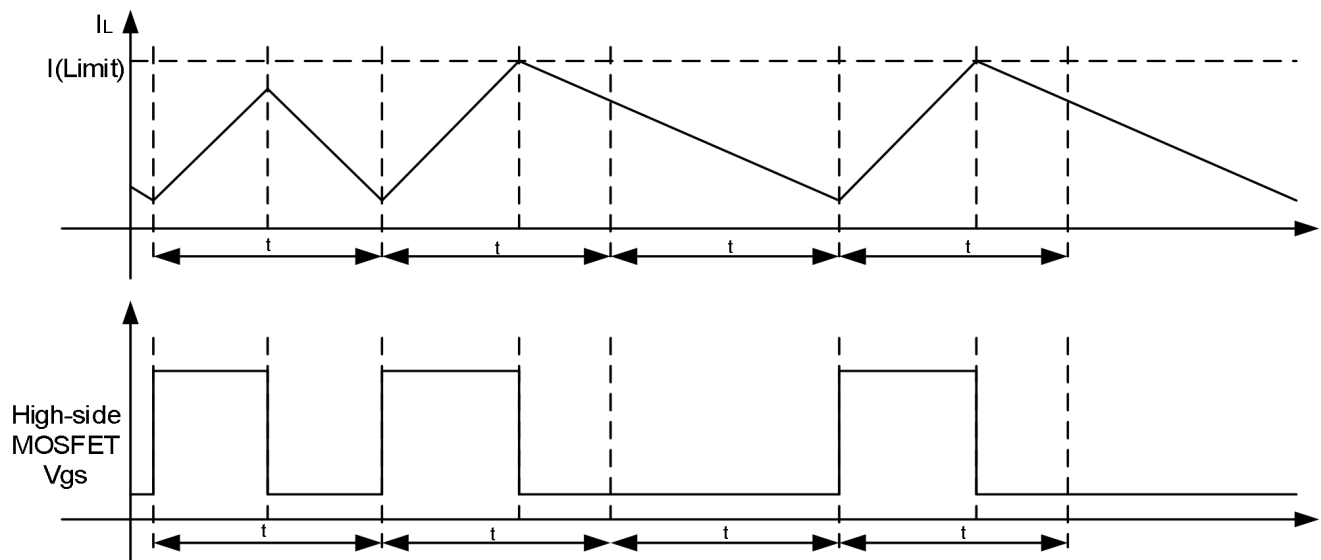
Functional Block Diagram

Overview

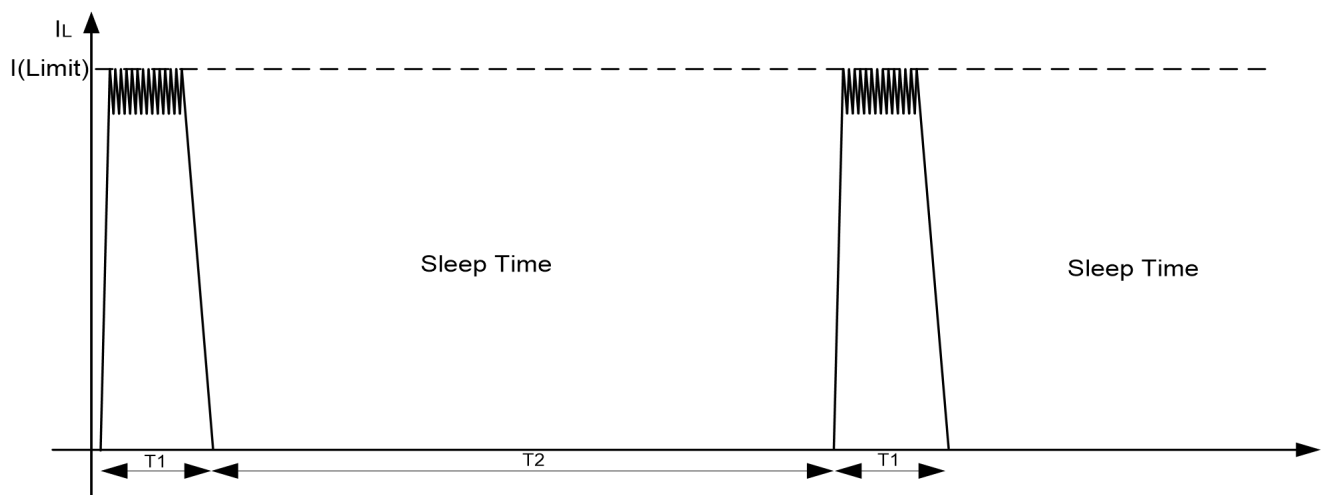
The MST8820AXKP is a 9V-80V input, 2A output, buck converter with integrated 400mΩ $R_{ds(on)}$ high-side power MOSFET. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external loop compensation design. The MST8820AXKP features an internal 200μs soft-start time to avoid large inrush current and output voltage overshoot during startup. The MST8820AXKP full protection features include the input under-voltage lockout, over current protection with cycle-by-cycle current limiting, output hard short protection and thermal shutdown protection.

Applications Information

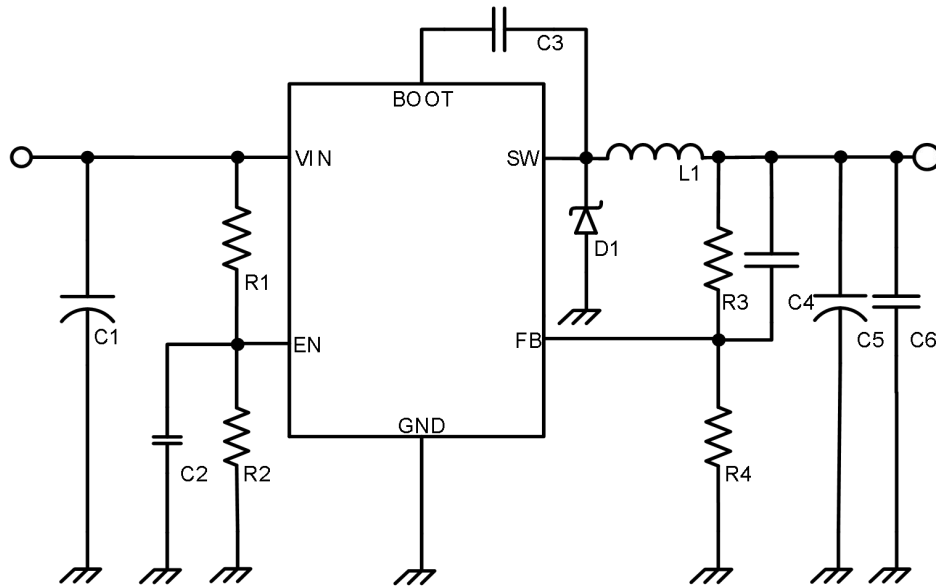
Over-current Protection: The MST8820AXKP implements current-mode control which uses the internal COMP voltage to control the turn on and the turnoff of the high-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared. When the peak switch current intersects the current reference the high-side switch turns off.



Hiccup mode: If an output overload condition occurs for more than the hiccup wait time, which is programmed for 512 switching cycles (T_1), the device shuts down and restarts after the hiccup time of 16384 cycles (T_2). The hiccup mode helps to reduce the device power dissipation under severe over-current conditions.



Typical Application



MST8820AXKP Design Example, 12V Output with Programmable UVLO

ID	Parameters	Type	Part Number	Vendor
U1		ESOP-8	MST8820AXKP	MST
C1	47uF	Capacitor,47uF,100V,20%,插件	ECE2EM470K21OTPO	Yunxing
C2	10uF	Capacitor,10uF,10V,20%,0603	CL10A106MP8NNNC	SAMSUNG
C3	0.1uF	Capacitor,0.1uF,50V,10%,0603	CL10B104KB8NNNC	SAMSUNG
C4	470pF	Capacitor,470pF,50V,10%,0603	CC0603KRX7R9BB471	YAGEO
C5	100uF	Capacitor,100uF,25V,20%,插件	RC025M101LO8*12TH-2A1Et	BERYL
C6	10uF	Capacitor,10uF,25V,10%,0805	CL21A106KAYNNNE	SAMSUNG
R1	100K	Resistor,100K,1%,0603	RC0603FR-07100KL	YAGEO
R2	10K	Resistor,10K,1%,0603	RT0603BRD0710KL	YAGEO
R3	43K	Resistor,43K,1%,0603	RC0603FR-0743KL	YAGEO
R4	3K	Resistor,3K,1%,0603	RC0603FR-073KL	YAGEO
D1	3A	Diode,3A,100V	SS310FL	GOODWORK
L1	68uH	Inductance,68uH,3A	MWSA1004S-680MT	SUNLORD

Design Parameters	Example Value
Input Voltage	48V
Output Voltage	12V
Maximum Output Current	2A
Switching Frequency	150/300KHz
Start Input Voltage (rising VIN)	24V
Stop Input Voltage (falling VIN)	22V

Output Voltage

The output voltage is set by an external resistor divider

R3 and R4 in typical application schematic.

Recommended R4 resistance is 3KΩ. Use equation

1 to calculate R3, $V_{REF}=0.8V$.

$$R_3 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) * R_4 \quad (1)$$

Under Voltage Lock-Out

An external voltage divider network of R1 from the input to EN pin and R2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold, $V_{EN}=2.2V$.

$$R_1 = \left(\frac{V_{UVLO}}{V_{EN}} - 1 \right) * R_2 \quad (2)$$

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor ILPP can be calculated as in Equation 3.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{sw}} \quad (3)$$

I_{LPP} is the inductor peak-to-peak current

L is the inductance of inductor

f_{sw} is the switching frequency

V_{OUT} is the output voltage

V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 4 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{sw} * LIR * I_{OUT(max)}} * \left(1 - \frac{V_{OUT}}{V_{IN(max)}} \right) \quad (4)$$

L_{MIN} is the minimum inductance required

f_{sw} is the switching frequency

V_{OUT} is the output voltage

$V_{IN(max)}$ is the maximum input voltage

$I_{OUT(max)}$ is the maximum DC load current

LIR is coefficient of ILPP to IOUT

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current. And RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 5 and equation 6.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (5)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (6)$$

I_{LPEAK} is the inductor peak current

I_{OUT} is the DC load current

I_{LPP} is the inductor peak-to-peak current

I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 4A. The most conservative approach is to choose an inductor with a saturation current rating greater than 4A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Diode Selection

requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(max)}$. The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator. Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 100-V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the MST8820AXKP. For the example design, the SS310 Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the SS310FL is 0.65 volts at 3 A. The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. The ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 14 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 1uF) with small package size (0805) to filter high frequency switching noise. Place the small size capacitor close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (7)$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 17 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

For this example, four 4.7 μ F, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1 μ F for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1F ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance. The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 18 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}^2 * L * C_{OUT} * V_{IN}} \quad (10)$$

ΔV_{OUT} is the output voltage ripple

f_{SW} is the switching frequency

L is the inductance of inductor

C_{OUT} is the output capacitance

V_{OUT} is the output voltage

V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, four 47F ceramic output capacitors work for most applications.

Typical Characteristics (At $T_A=25^{\circ}\text{C}$, $V_{IN}=48\text{V}$, $V_{OUT}=12\text{V}$, Unless Otherwise Noted)

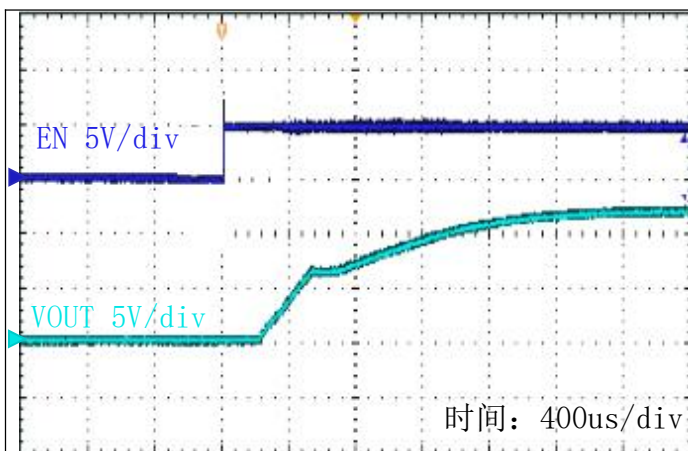


Figure1 EN Start up

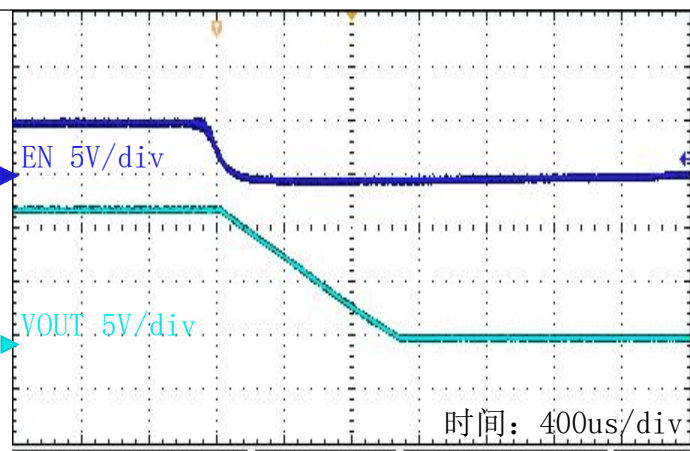


Figure2 EN Turn off

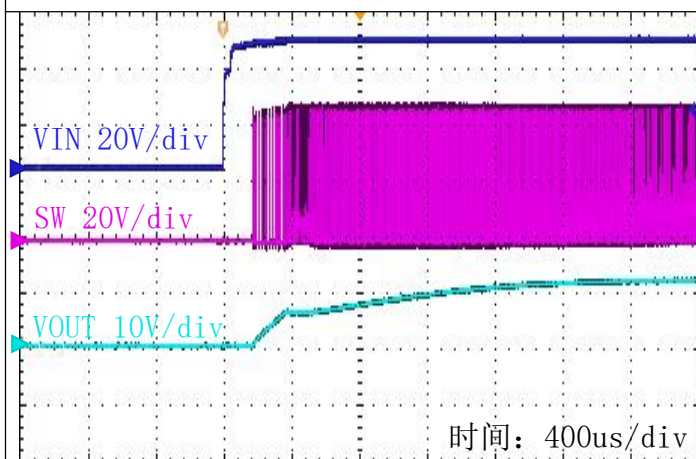


Figure3 Start up

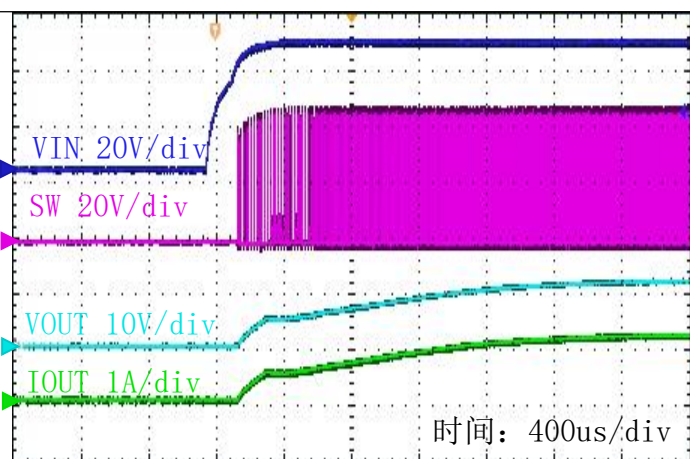
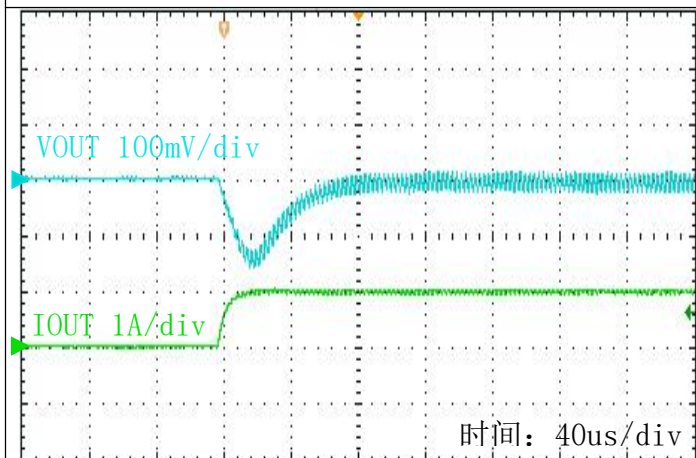
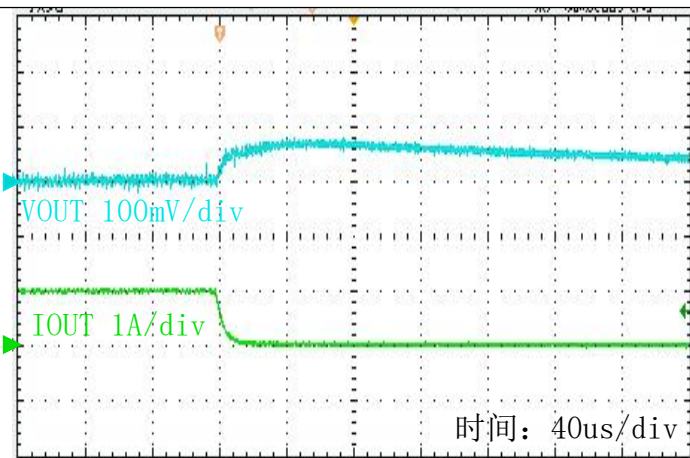


Figure4 Start up



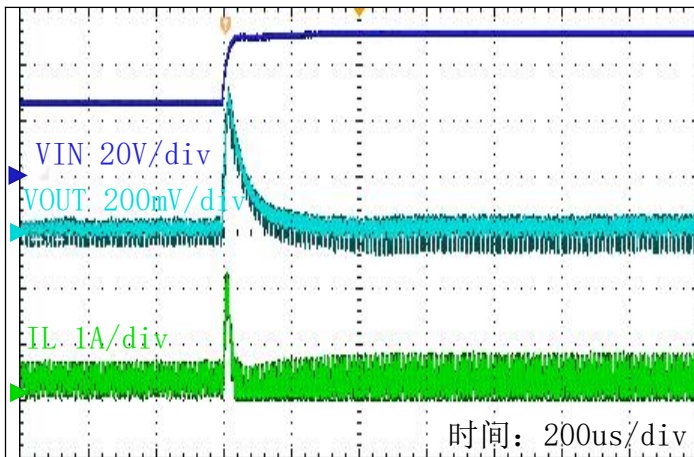
$I_{out}=10\text{mA} \sim 1\text{A}$

Figure5 Load Transient



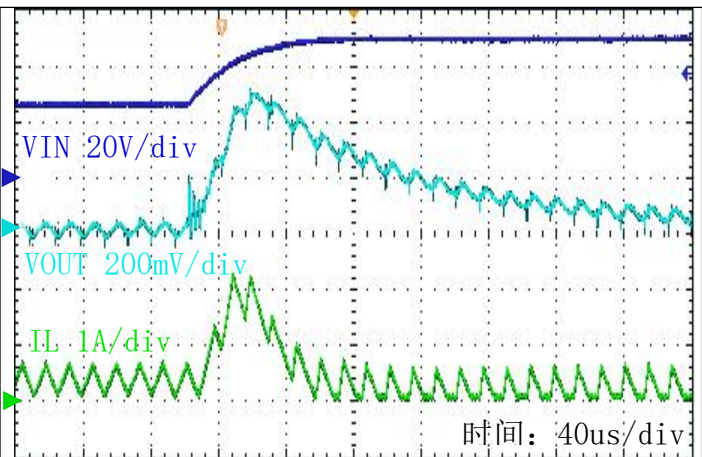
$I_{out}=1\text{A} \sim 10\text{mA}$

Figure6 Load Transient



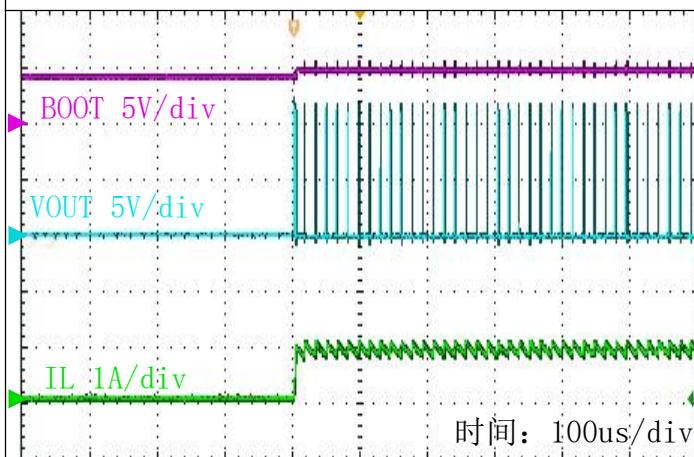
Iout=300mA Vin=24V~48V

Figure7 Line Transient



Iout=300mA Vin=24V~48V

Figure8 Line Transient



Vin=24V Iout=0A

Figure9 Continuous Short Circuit

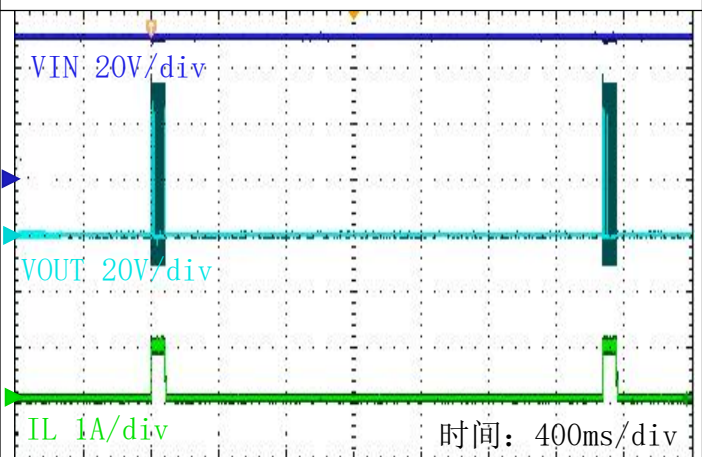
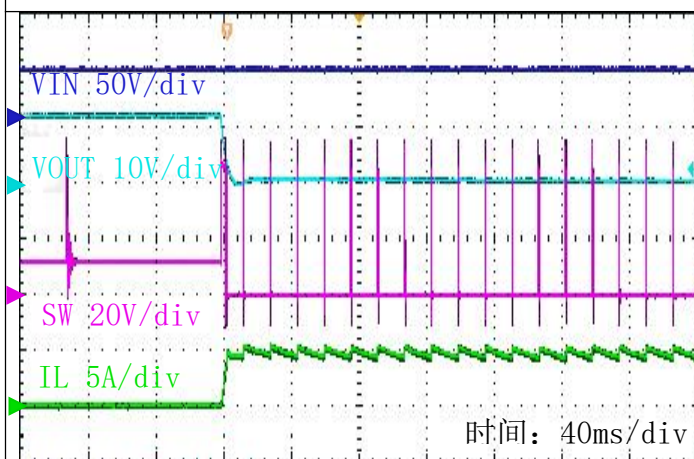
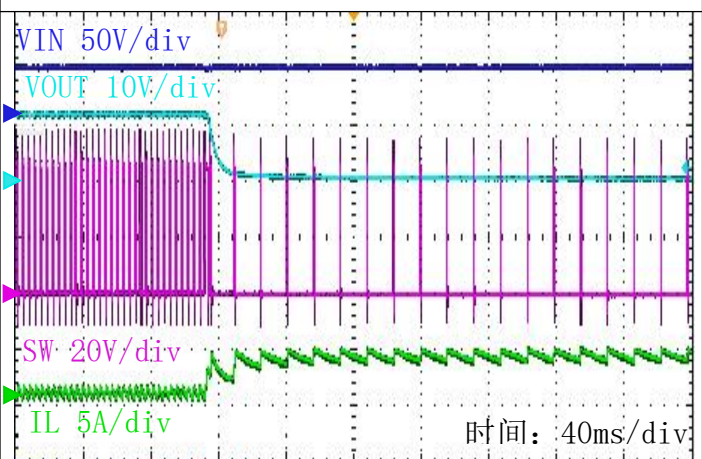


Figure10 Continuous Short Circuit



Iout=0A

Figure11 Power On Short Circuit



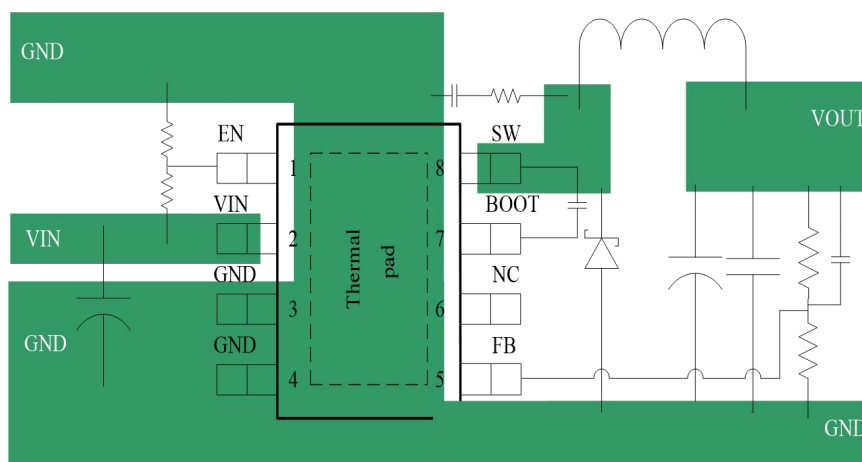
Iout=1A

Figure12 Power On Short Circuit

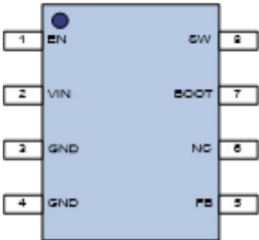
Layout

Proper PCB layout is a critical for MST8820AXKP's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

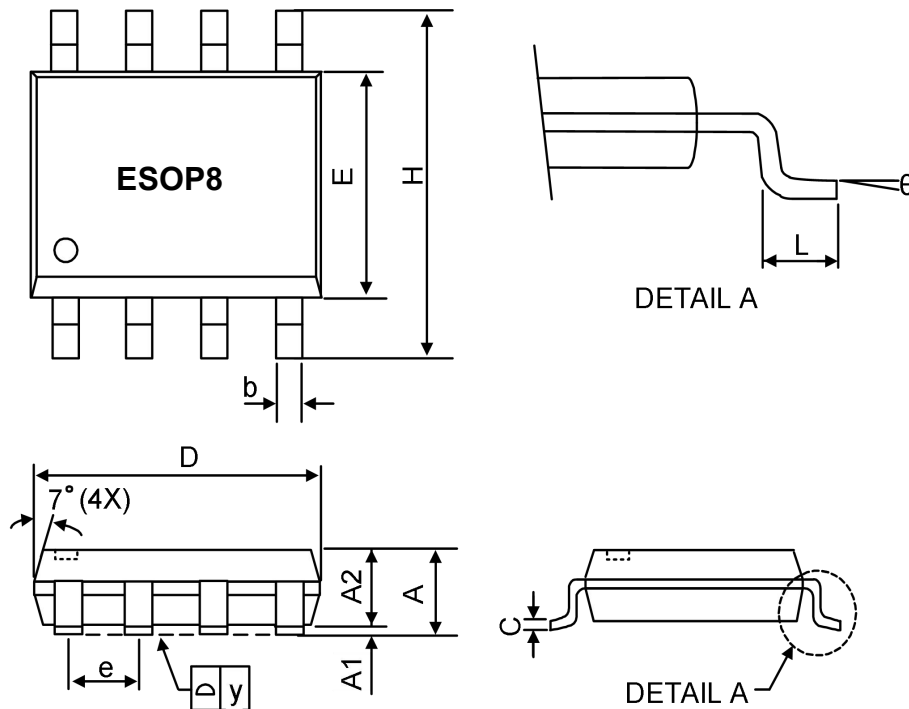
1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impedance and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. Freewheeling diode should be place as close to SW pin and the ground as possible to reduce parasitic effect.
4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impedance of grounding.
5. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
6. Output inductor and freewheeling diode should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive cap active coupling.
7. Route BOOT capacitor trace on the other layer than top layer to provide wide path for topside ground.



Ordering And Marking Information

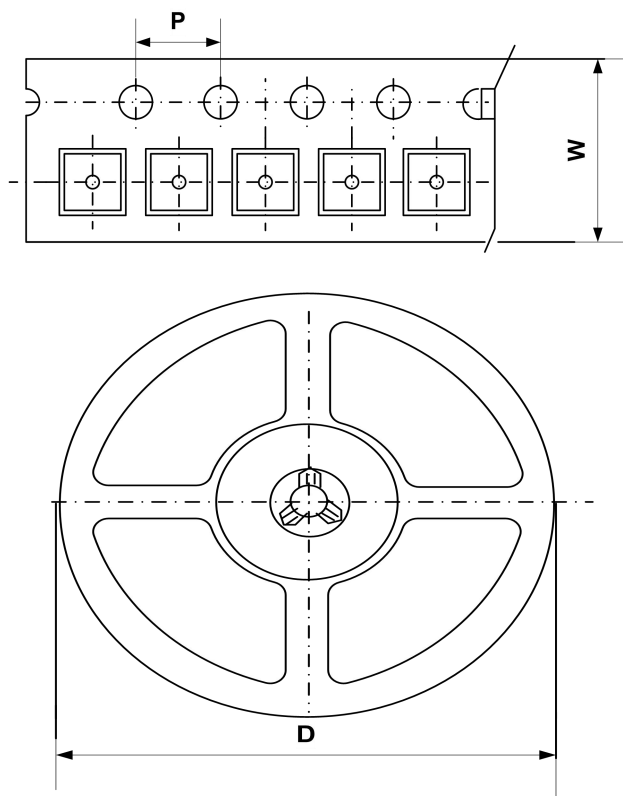
Part Number	Package Outline	
MST8820AXKP - Package Definition - Frequency identification - Product Name - Company Name		ESOP8 4000pcs/Reel
		8820AX 348 X - A1:150KHz A3:300KHz - X:Packaging Factory 348: Year2023,Week 48 - Product Name

Package Outline



Symbol	Millimetre			Inch		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.75	-	-	0.069
A1	0.1	-	0.25	0.04	-	0.1
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
θ	0°	-	8°	0°	-	8°

Packing Information



Type	W(mm)	P(mm)	D(mm)	Qty (pcs)
ESOP8	12.0±0.1 mm	8.0±0.1 mm	330±1 mm	4000pcs



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1-0	2022-9-20		Xingxiaolin	Xingxiaolin	Xingxiaolin
1-1	2023-2-7		Xingxiaolin	Xingxiaolin	Xingxiaolin
1-2	2024-5-6		Lvhan	Lvhan	Lvhan



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