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HLW8032 User manual

REV 1.5

Address: F4, Building 6, Zhongchu Building, Baguasi Road, Futian District, Shenzhen
Postcode: 518028
Website:www.hiliwi.com
Tel.:0755-29650970
Fax:0755-86968790

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Single-phase metering IC

HLW8032

Product application

- Intelligent household appliances
- Metering socket
- Smart WIFI socket
- Charging pile for electromobile
- PDU equipment
- LED lighting
- Street lamp control

Features

- ✓ Able to measure effective value of active power, apparent power, current and voltage
- ✓ Output of active electric energy pulse from PF pin
- ✓ Measuring error of active power reaches 0.2% with dynamic range of 1000:1
- ✓ Measuring error of effective current reaches 0.5% with dynamic range of 1000:1
- ✓ Measuring error of effective voltage reaches 0.5% within dynamic range of 1000:1
- ✓ Built-in frequency oscillator
- ✓ Built-in voltage reference source
- ✓ Built-in power supply monitoring circuit
- ✓ UART communication
- ✓ SOP8 packaging

General Description

HLW8032 is a high-precision electric energy metering IC which is manufactured using CMOS process and is mainly applied to single-phase application. It is able to measure line voltage and current and calculate active power, apparent power and power factor.

The interior of the device integrates two ∑-Δ ADCs and one high-precision inner core of electric energy metering. Able to communicate data via UART port, HLW8032 adopts 5V power supply and built-in 3.579M crystal oscillator, and uses SOP packaging with 8Pin.

Featured with high precision, low power consumption, high reliability, strong adaptability to environment, etc., HLW8032 is applicable to electric energy metering for power consumers with single-phase two-wire system.

Functional block diagram

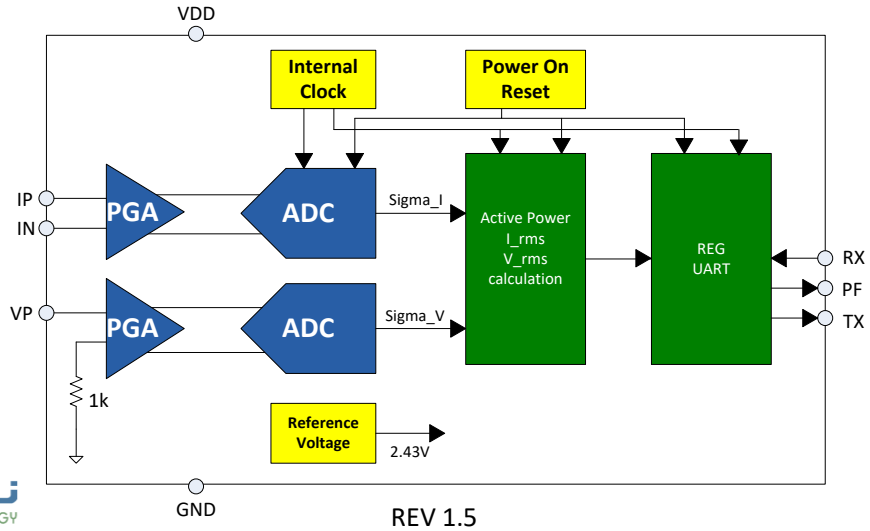

Fig. 1 Functional block diagram of chip

Contents

Revision history

Time	Revision record	Version
2015-9-26	Initial version	REV 1.0
2016-7-18	Modified contents	REV 1.1
2016-9-20	Modified State REG register	REV 1.2
2017-3-11	Modified statistic method for electrical quantity	REV 1.3
2018-3-5	Supplemented description of data format	REV 1.4
2018-3-20	Supplemented description for State REG	REV 1.5

Pin configuration and functional description

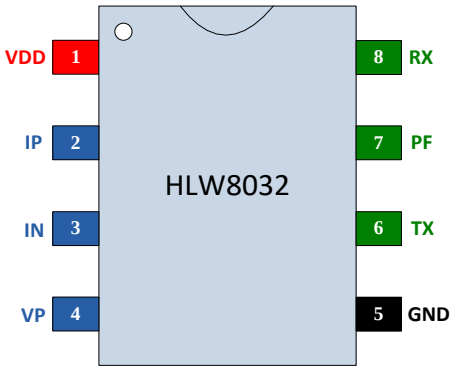

Fig.2 chip pin Diagram

Table 1 Functional description of pins

Pin SN	Pin name	Input/output	Description
1	VDD	Chip power supply	Chip power supply
2	IP	Analog input	Positive input terminal for differential signal of current, the maximal effective value of differential input voltage is ±30.9mV
3	IN	Analog input	Negative input terminal for differential signal of current, the maximal effective value of differential input voltage is±30.9mV
4	VP	Analog input	Positive input terminal of voltage signal, the maximum effective value of input voltage is ±495mV
5	GND	Chip ground	Grounding of chip
6	TX	Digital output	UART data output port
7	PF	Output	Outputting active high frequency rectangular wave pulse, duty ratio is 50%
8	RX	Digital input	UART data input port (reserved port which does not needed to used by user)

Technical specification

Recommended working conditions

Parameter	Sign	Minima	Typical value	Maxima	Unit
Positive power	VDD	4.5	5.0	5.5	V
Temperature range	T_A	-40	-	+85	℃

Analog characteristics

Unless otherwise specified, VDD= 5.0V,GND= 0V, on-chip reference voltage, on-chip oscillator, T_{MIN} to T_{MAX} = -40℃ to 85℃

Parameter	符号	Minima	Typical value	Maxima	Unit
Precision					
Active power Full gain range Input range 0.1% ~ 100%	P_{Active}	-	±0.2	-	%
Current effective value Full gain range Input range 0.2% ~ 100%	I_{RMS}	-	±0.5	-	%
Voltage effective value Full gain range Input range 0.2% ~ 100%	V_{RMS}	-	±0.5	-	%
Analog input (all channels)					
Common mode signal		-1	-	1	V
Analog input					
Crosstalk interference in voltage channel in the case of full range (50, 60Hz)		-	-100	-	dB
Input capacitance	IC	-	6.4	-	pF
Equivalent input impedance Current channel Voltage channel	EII		500 6	-	kΩ MΩ

Equivalent input noise Current channel Voltage channel	N_I	- -	- -	2 20	μVrms μVrms
Power supply					
Current consumption IA+ID			4	-	mA
Power consumption (VDD = 5 V)	PC	-	25		mW
Low voltage threshold for power failure detection	PMLO	-	4	-	V
High voltage threshold for power failure detection	PMHI	-	4.3	-	V

Built-in reference voltage

Parameter	Sign	Minima	Typical value	Maxima	Unit
Reference voltage	VREF	+2.3	+2.43	+2.55	V
Temperature drift	TC_{VREF}	-	25	-	ppm/℃

Numerical properties

Unless otherwise specified, VDD = 5.0V, GND = 0V, on-chip reference voltage, on-chip oscillator, TMIN to TMAX = - 40℃ to 85℃

Parameter	Sign	Minima	Typical value	Maxima	Unit
Master clock					
Master clock frequency	MCLK	3.04	3.579	4.12	MHz
Duty ratio of master clock		30	50	70	%
Filter					
Input sampling rate(DCLK = MCLK/K)		-	MCLK/4	-	Hz
Output code rate of digital filter	OWR	-	MCLK/ 128	-	Hz
Turnover (- 3dB) frequency of high pass filter		-	0.543	-	Hz
Input/output					

High level input voltage VDD = 5V	V_{IH}	0.8VDD	-	-	V
Low level input voltage VDD = 5V	V_{IL}	-	-	0.8	V
High level output voltage Iout = +5 mA	V_{OH}	VDD-0.5	-	-	V
Low level output voltage Iout = - 5 mA	V_{OL}	-	-	0.5	V
Input leakage current	I_{in}	-	±10	-	μA
Capacitance of digital output pin	C_{OUT}	-	5	-	pF

Absolute mxximum ratings

Parameter	Sign	Minima	Typical value	Maxima	Unit
Digital power supply	VDD	-0.3	-	+6.0	V
Analog power supply	VDD	-0.3	-	+6.0	V
VDD to GND		-0.3	-	+6.0	V
V1P, V1N, V2P		-2		+2	V
Analog input voltage	V_{INA}	-0.3	-	VDD+0.3	V
Digital input voltage	V_{IND}	-0.3	-	VDD+0.3	V
Digital output voltage	V_{OUTD}	-0.3	-	VDD+0.3	V
Temperature of work environment	T_A	-40	-	85	°C
Storage temperature	T_{stg}	-65	-	150	°C

UART communication interface

HLW8032 has a simple UART interface and adopts asynchronous serial communication mode, which allows data communication via two one-way pins. The UART interface can realize isolated communication by only a low-cost photoelectric coupler. The UART interface operates at fixed frequency of 4800 bps and its interval for transmitting data is 50mS, which is suitable for design of low velocity.

UART of HLW8032 uses two pins. The TX pin is used to transmit data from HLW8032, and data is transmitted in the least significant bit (LSB) with priority. The RX pin is used to receive the data from microcontroller.

UART data format

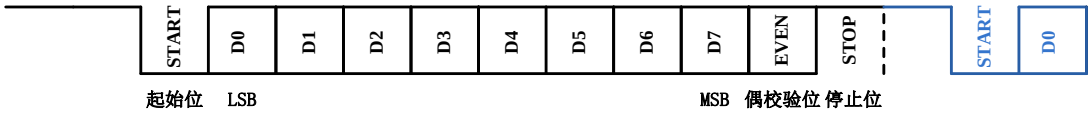

Fig.3 UART frame data

Data format of HLW8032:

Baud rate:4800bps

Start bit+data bit (8bit) + even bit + stop bit

Every complete transmission of data by HLW8032 is 24bytes. The transmission of a group of data starts from register 1 (State REG) and ends at register 11 (CheckSum REG), involving altogether 11 registers and data of 24 bytes. See register list for details.

Register description

Register list

SN	Data type	Data length(Byte)	Description
1	State register (State REG)	1	Indication of data state
2	Check register (Check REG)	1	Default
3	Voltage parameter register (Voltage parameter REG)	3	Default
4	Voltage register (Voltage REG)	3	
5	Current parameter register (Current Parameter REG)	3	Default
6	Current register (Current REG)	3	
7	Power parameter register (Power parameter REG)	3	Default
8	Power register (Power REG)	3	
9	Data updata register (Data Updata REG)	1	Indication of power, voltage, current state
10	PF register (PF REG)	2	PF pulse numbers, used in conjunction with state register, not saved after power-fail
11	CheckSum register (CheckSum REG)	1	Data check sum, used to verify whether data package is complete in communication

Every complete transmission of data by HLW8032 is 24bytes. The transmission of a group of data starts from register 1 (State REG) and ends at register 11 (CheckSum REG), involving altogether 11 registers and data of 24 bytes.

State REG

	8bit	Function	Description
State REG	Bit7	Reserve	1,Default
	Bit6	Reserve	1,Default
	Bit5	Reserve	1,Default
	Bit4	Reserve	1,Default
	Bit3	Status bit of Voltage REG	0: Normal 1: Voltage REG overflows
	Bit2	Status bit of current register	0: Normal 1: Current REG overflows
	Bit1	Status bit of Power REG	0: Normal 1: Power REG overflows
	Bit0	Status bit for Voltage Parameter REG, Current Parameter REG and Power Parameter REG	0: Normal 1: Voltage Parameter REG, Current Parameter REG and Power Parameter REG is not usable

1. When State REG = 0xaa, the chip's function of error correction fails, now the Voltage Parameter REG, Current Parameter REG and Power Parameter REG are not usable;
2. When State REG = 0x55, the chip's function of error correction is normal, now the Voltage Parameter REG, Current Parameter REG and Power Parameter REG are usable, and the Voltage REG, Current REG and Power REG do not overflow;
3. When State REG = 0xfx (x is arbitrary number between 0-f), the chip's function of error correction is normal, now the Voltage Parameter REG, Current Parameter REG and Power Parameter REG are usable. When the corresponding bit of State REG is 1, this represents corresponding register overflows, and overflowing means the current, voltage or power are very small and approach 0;

Check REG

Check REG	Hexadecimal	Description
8bit	0x5A	Default

Voltage Parameter REG

U Parameter REG	High Byte	Middle Byte	Low Byte
24bit	8bit	8bit	8bit

Transmission order of data: High 8bit - > middle 8bit - > low 8bit

This register is of default

Voltage REG

Voltage REG	High Byte	Middle Byte	Low Byte
24bit	8bit	8bit	8bit

Transmission order of data: High 8bit - > middle 8bit - > low 8bit

Current Parameter REG

Current Parameter REG	High Byte	Middle Byte	Low Byte
24bit	8bit	8bit	8bit

Transmission order of data: High 8bit - > middle 8bit - > low 8bit

This register is of default

Current REG

Current REG	High Byte	Middle Byte	Low Byte
24bit	8bit	8bit	8bit

Transmission order of data: High 8bit - > middle 8bit - > low 8bit

Power Parameter REG

Power Parameter REG	High Byte	Middle Byte	Low Byte
24bit	8bit	8bit	8bit

Transmission order of data: High 8bit -- > middle 8bit-- > low 8bit

This register is of default.

Power REG

Power REG	High Byte	Middle Byte	Low Byte
24bit	8bit	8bit	8bit

Transmission order of data: High 8bit - > middle 8bit - > low 8bit

Data updata register

	8bit	Function	Description
Data Updata REG	Bit7	Carry flag bit of PF register	When PF REG overflows, bit7 is negated once
	Bit6	Status flag bit of Voltage REG	0:Updating of Voltage REG data is not finished 1:Updating of Voltage REG data has been finished
	Bit5	Status flag bit of Current REG	0:Updating of Current REG data is not finished 1:Updating of Current REG data has been finished

	Bit4	Status flag bit of Power REG	0:Updating of Power REG data is not finished 1:Updating of Power REG data has been finished
	Bit3	Reserve	
	Bit2	Reserve	
	Bit1	Reserve	
	Bit0	Reserve	

1. Bit6 = 1 represents data state of Voltage REG has been updated;
2. Bit5 = 1 represents data state of Current REG has been updated;
3. Bit4 = 1 represents data state of Power REG has been updated;

3、When bit4 = 1,

PF REG

PF REG		High Byte	Low Byte
16bit		8bit	8bit

Transmission order of data: High 8bit -- > low 8bit

PF REG is used to accumulate impulse signal. When the 16-bit register's data overflows, the bit7 of Data Updata REG would be negated once, and PF REG is zeroed.

CheckSum REG

CheckSum REG	Hexadecimal	Description
8bit	0xXX	CHECKSUM Low 8bit for the sum data for register otherwise than State REG, Check REG and CheckSum REG

When the data of CheckSum REG is not equal to low 8bit for the sum data for register otherwise than State REG, Check REG and CheckSum REG, the data for this time is discarded

Operating principle and typical application

Typical application circuit

As shown in Fig.4, two small capacitors should be connected in parallel at power end of

HLW8032 to filter the high frequency and low frequency noise from grid.

The the electric current signal sampled by manganin resistor is connected to HLW8032, while the voltage signal is input to HLW8032 after passing resistance network. PF and TX are directly connected to input end of CPU. The current effective value, voltage effective value and active power are calculated via formula.

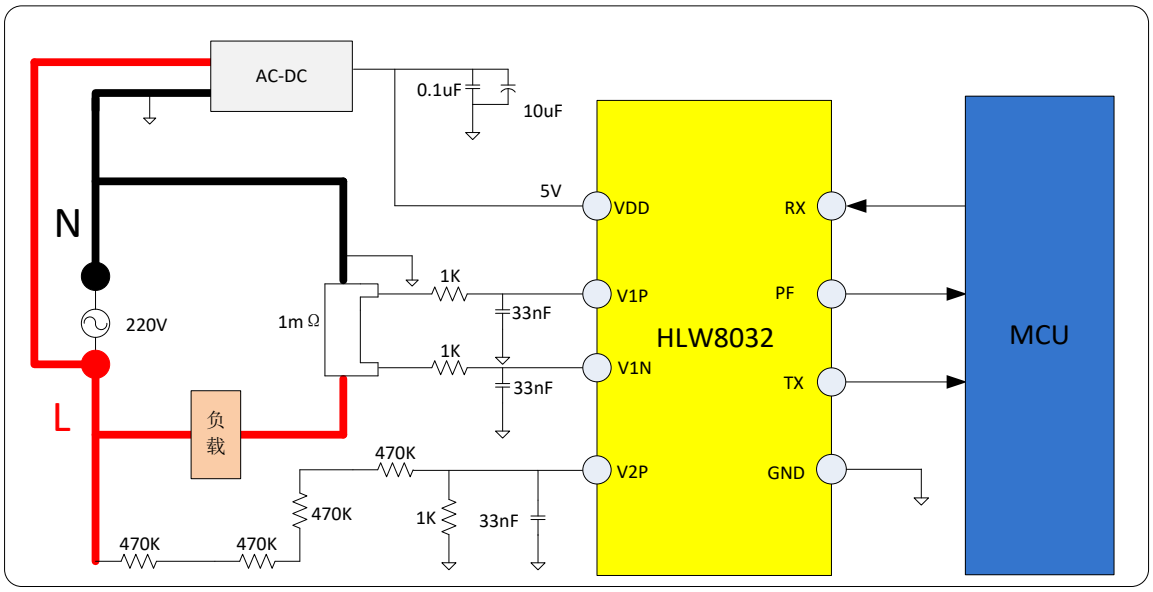

Fig.4 Typical application circuit of HLW8032

Calculation of voltage current effective value

$$\text{Effective voltage} = \frac{\text{Voltage Parameter REG}}{\text{Voltage REG}} \times \text{Voltage coefficient}$$

Voltage coefficient: voltage division coefficient of resistance for voltage channel. Take Fig.3 for example: the sampled voltage signal passes four 470K resistors and 1k resistors for voltage division , then Voltage coefficient $= \frac{470K \times 4}{1K \times 1000} = \frac{1880K}{1000K} = 1.88$;

Calculation of current effective value

$$\text{Effective current} = \frac{\text{Current Parameter REG}}{\text{Current REG}} \times \text{Current coefficient}$$

Current coefficient: resistance coefficient of current channel. Take Fig.3 for example: the sampled resistance is R = 0.001Ω,

then Current coefficient $= \frac{1}{\text{R}\times 1000} = \frac{1}{0.001\times 1000} = 1$;

Calculation of active power

$$\textbf{Active power} = \frac{\text{Power Parameter REG}}{\text{Power REG}} \times \text{Voltage coefficient} \times \text{Current coefficient}$$

Calculation of apparent power

$$\textbf{Apparent power} = \text{Effective voltage} \times \text{Effective current}$$

Calculation of power factor

$$\textbf{Power factor} = \frac{\text{Active power}}{\textbf{Apparent power}}$$

Electrical quantity calculation

Statistics table 5 of impulse signal count involves registers related to impulse signal, including Data Updata REG and PF REG. Register related to impulse signal	Data Updata REG bit7	PF REG	
	High Byte	Middle Byte	Low Byte
17bit	1bit	8bit	8bit

1、Statistics of pulse count

PF REG represents pulse number of PF. When PF REG overflows, the bit7 of Data Updata REG would be negated, and PF REG is zeroed at the same time. So, impulse signal count:

$$PF_{cnt} = k * 65536 + n$$

k is the negation times for bit7 of Data Updata REG

n is register value of PF REG

Corresponding pulse count of 2 and 1 kwh

Pulse count of 1kwh

$$= \frac{1}{\text{Power parameter REG}} \times \frac{1}{\text{Voltage coefficient} \times \text{Current coefficient}} \times 10^9 \times 3600$$

When the count of PF_{cnt} is equal to the pulse count of 1kwh, this means 1 kwh has been tallied accumulatively;

Current electrical quantity (KW.h)=$\frac{PF_{cnt}}{pulse}$ count for 1kwh

Packaging of HLW8032

HLW8032 adopts SOP8 packaging mode. The concrete packaging information is as shown in figure below:

Size / Label	Min （mm）	Max （mm）	Size / Label	Min （mm）	Max （mm）
A	4.95	5.15	C3	0.05	0.20
A1	0.37	0.47	C4	0.20TYP	
A2	1.27TYP		D	1.05TYP	
A3	0.41TYP		D1	0.40	0.60
B	5.80	6.20	R1	0.07TYP	
B1	3.80	4.00	R2	0.07TYP	
B2	5.0TYP		θ1	17°TYP	
C	1.30	1.50	θ2	13°TYP	
C1	0.55	0.65	θ3	4°TYP	
C2	0.55	0.65	θ4	12°TYP	

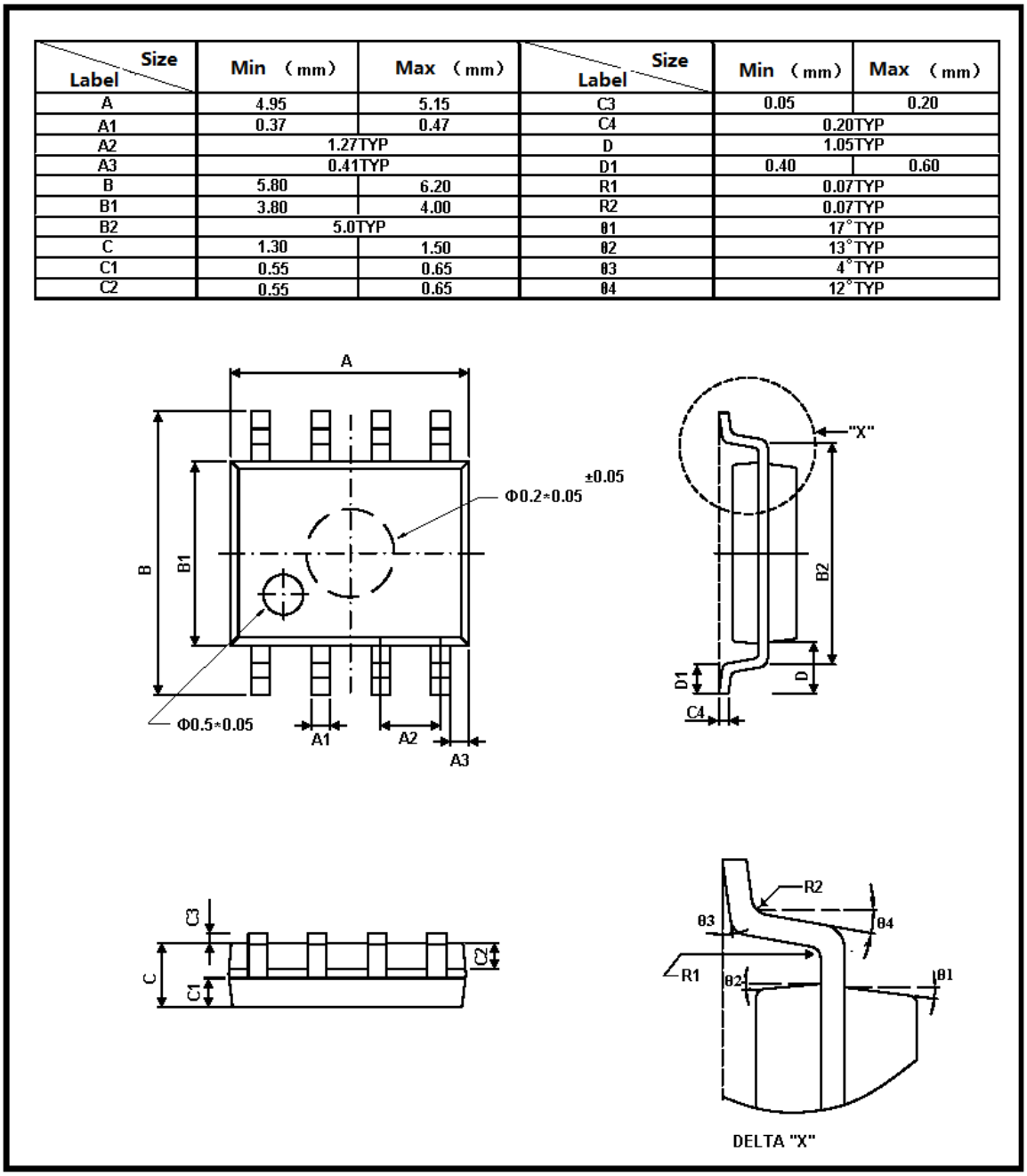

Fig. 5 Packaging size diagram of HLW8032